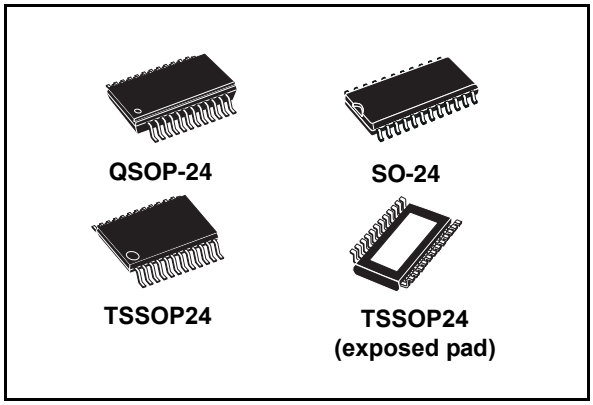
STP16CPP05

Low voltage 16-bit constant current LED sink driver

Features

- 16 constant current output channels
- Adjustable output current through external resistor
- Output current: 3-40 mA
- Serial data in/parallel data ouT
- 3.3 V or 5 V supply voltage
- Max clock frequency 30 MHz
- Schmitt-trigger input
- ESD protection 2 kV HBM
- Thermal shutdown



Description

The STP16CPP05 is a monolithic, low voltage, low current power 16-bit shift register designed for LED panel displays. The STP16CPP05 contains a 16-bit serial-in, parallel-out shift register that feeds a 16-bit, D-type storage register. In the output stage, sixteen regulated current sources provide from 3 mA to 40 mA constant current to drive the LEDs.

The output current setup time is 40 ns (typ), thus improving the system performance.

The LEDs' brightness can be controlled by using an external resistor to adjust the STP16CPP05 output current.

The STP16CPP05 guarantees a 20 V output driving capability, allowing users to connect more LEDs in series.The high clock frequency, 30 MHz, makes the device suitable for high data rate transmission. The 3.3 V voltage supply is useful in applications that interface with a 3.3 V micro controller.

Table 1. Device summary

Order codes	Package	Packaging
STP16CPP05MTR	SO-24	1000 parts per reel
STP16CPP05TTR	TSSOP24	2500 parts per reel
STP16CPP05XTTR	TSSOP24 exposed pad	2500 parts per reel
STP16CPP05PTR	QSOP-24	2500 parts per reel

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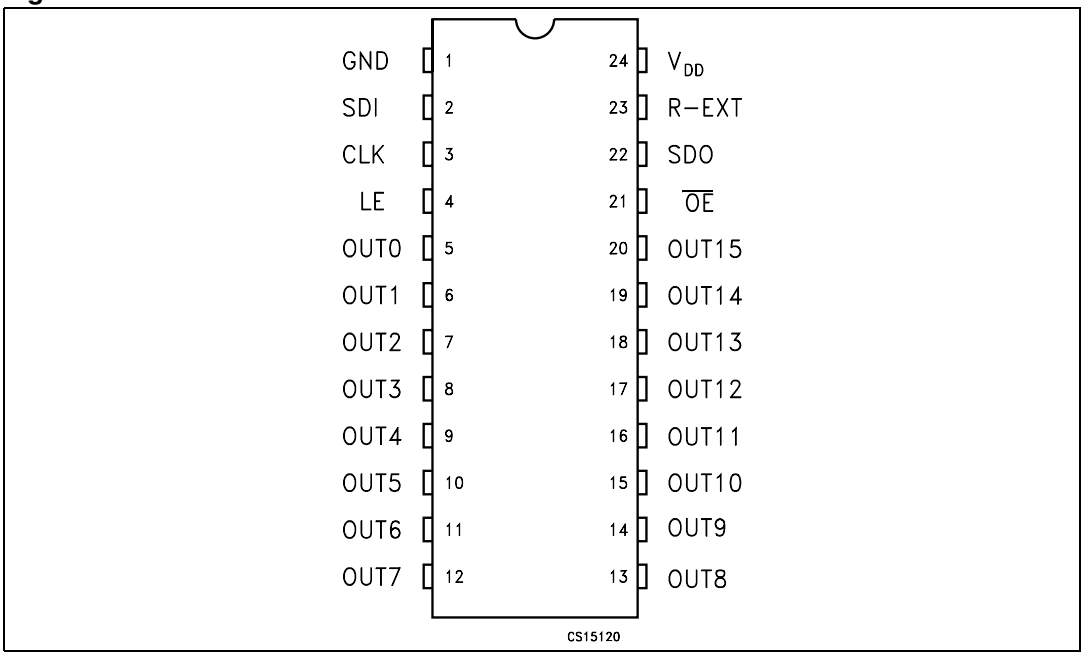
1 Summary description

Table 2. Typical current accuracy

Output voltage	Current accuracy		Output current	V_{DD}	Temperature
	Between bits	Between ICs			
≥ 1.3 V	± 2 %	±5 %	≥ 5 to 40 mA	3.3 V to 5 V	25 °C

1.1 Pin connection and description

Figure 2. Pin connection



Note: The exposed pad is electrically not connected

Table 3. Pin description

Pin N°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE	Latch input terminal
5-20	OUT 0-15	Output terminal
21	$\overline{OE}$	Input terminal of output enable (active low)
22	SDO	Serial data out terminal
23	R-EXT	Input terminal of an external resistor for constant current programing
24	V_{DD}	Supply voltage terminal

2 Electrical ratings

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	0 to 7	V
V_O	Output voltage	-0.5 to 20	V
I_O	Output current	50	mA
V_I	Input voltage	-0.4 to V_{DD}+0.4	V
I_{GND}	GND terminal current	800	mA
f_{CLK}	Clock frequency	50	MHz

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter		Value	Unit
T_{OPR}	Operating temperature range		-40 to +125	°C
T_{STG}	Storage temperature range		-55 to +150	°C
R_{thJC}	Thermal resistance junction-case	SO-24	60	°C/W
		TSSOP24	85	°C/W
		TSSOP24(1) Exposed Pad	37.5	°C/W
		QSOP-24	72	°C/W

1. The exposed pad should be soldered directly to the PCB to realize the thermal benefits.

2.3 Recommended operating conditions

Table 6. Recommended operating conditions at 25 °C

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage		3.0		5.5	V
V_O	Output voltage				20	V
I_O	Output current	OUTn	3		40	mA
I_{OH}	Output current	SERIAL-OUT			+1	mA
I_{OL}	Output current	SERIAL-OUT			-1	mA
V_{IH}	Input voltage		0.7 V_{DD}		V_{DD}+0.3	V
V_{IL}	Input voltage		-0.3		0.3 V_{DD}	V
t_{wLAT}	LE pulse width	V_{DD} = 3.3 V to 5.0 V	20			ns
t_{wCLK}	CLK pulse width		16			ns
t_{wEN}	$\overline{OE}$ pulse width		70			ns
$t_{SETUP(D)}$	Setup time for DATA		5			ns
$t_{HOLD(D)}$	Hold time for DATA		5			ns
$t_{SETUP(L)}$	Setup time for LATCH		15			ns
f_{CLK}	Clock frequency	Cascade operation (1)			30	MHz

1. If the device is connected in cascade, it may not be possible achieve the maximum data transfer. Please considered the timings carefully.

3 Electrical characteristics

Table 7. Electrical characteristics
(V_{DD} = 3.3 V to 5 V, T = 25 °C, unless otherwise specified.)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IH}	Input voltage high level		$0.7V_{DD}$		V_{DD}	V
V_{IL}	Input voltage low level		GND		$0.3V_{DD}$	V
I_{OH}	Output leakage current	V_{OH} = 20 V		0.15	1	µA
V_{OL}	Output voltage (Serial-OUT)	I_{OL} = 1 mA			0.4	V
V_{OH}	Output voltage (Serial-OUT)	I_{OH} = -1 mA	V_{DD}-0.4V			V
I_{OL1}	Output current	V_O = 0.3 V, R_{ext} = 4 kΩ	4.75	5	5.25	mA
I_{OL2}		V_O = 0.3 V, R_{ext} = 980 Ω	19	20	21	
I_{OL3}		V_O = 1.3 V, R_{ext} = 490 Ω	38	40	42	
ΔI_{OL1}	Output current error between bit (All Output ON)	V_O = 0.3 V, I_O = 5 mA R_{EXT} = 4 kΩ		± 2	± 5	%
ΔI_{OL2}		V_O = 0.3 V, I_O = 20 mA R_{EXT} = 980 Ω		± 0.5	± 3	
ΔI_{OL3}		V_O = 1.3 V, I_O = 40 mA R_{EXT} = 490 Ω		± 1.0	± 3	
$R_{SIN(up)}$	Pull-up resistor		150	300	600	kΩ
$R_{SIN(down)}$	Pull-down resistor		100	200	400	kΩ
$I_{DD(OFF1)}$	Supply current (OFF)	R_{EXT} = 980 OUT 0 to 15 = OFF		5.4	7.5	mA
$I_{DD(OFF2)}$		R_{EXT} = 490 OUT 0 to 15 = OFF		8.0	9.5	
$I_{DD(ON1)}$	Supply current (ON)	R_{EXT} = 980 OUT 0 to 15 = ON		5.5	7.5	
$I_{DD(ON2)}$		R_{EXT} = 490 OUT 0 to 15 = ON		8.1	9.5	
Thermal	Thermal protection			170		°C

Table 8. Switching characteristics (V_{DD} = 5 V, T = 25 °C, unless otherwise specified.)

Symbol	Parameter	Test conditions			Min	Typ	Max	Unit
t_{PLH1}	Propagation delay time, CLK-$\overline{OUTn}$, LE = H, $\overline{OE}$ = L	$V_{IH} = V_{DD}$ V_{IL} = GND I_O = 20 mA R_{EXT} = 1 KΩ	C_L = 10 pF V_L = 3.0 V R_L = 60 Ω	V_{DD} = 3.3 V		44	58	ns
				V_{DD} = 5 V		24	32	
t_{PLH2}	Propagation delay time, LE-$\overline{OUTn}$, $\overline{OE}$ = L			V_{DD} = 3.3 V		43	56	ns
				V_{DD} = 5 V		24	32	
t_{PLH3}	Propagation delay time, $\overline{OE}$-$\overline{OUTn}$, LE = H			V_{DD} = 3.3 V		63	82	ns
				V_{DD} = 5 V		37	48	
t_{PLH}	Propagation delay time, CLK-SDO			V_{DD} = 3.3 V		17	22	ns
				V_{DD} = 5 V		11	14	
t_{PHL1}	Propagation delay time, CLK-$\overline{OUTn}$, LE = H, $\overline{OE}$ = L			V_{DD} = 3.3 V		22	28	ns
				V_{DD} = 5 V		16	21	
t_{PHL2}	Propagation delay time, LE-$\overline{OUTn}$, $\overline{OE}$ = L			V_{DD} = 3.3 V		19	25	ns
				V_{DD} = 5 V		15	20	
t_{PHL3}	Propagation delay time, $\overline{OE}$-$\overline{OUTn}$, LE = H			V_{DD} = 3.3 V		16	21	ns
				V_{DD} = 5 V		13	17	
t_{PHL}	Propagation delay time, CLK-SDO			V_{DD} = 3.3 V		21	27	ns
				V_{DD} = 5 V		13	17	
t_{ON}	Output rise time 10~90% of current waveform			V_{DD} = 3.3 V		26	35	ns
				V_{DD} = 5 V		12	16	
t_{OFF}	Output fall time 90~10% of current waveform			V_{DD} = 3.3 V		4	6	ns
				V_{DD} = 5 V		3	5	
t_r	CLK rise time (1)						5000	ns
t_f	CLK fall time (1)						5000	ns

1. In order to achieve high cascade data transfer,please consider tr/tf timings carefully.

4 Equivalent circuit and outputs

Figure 3. $\overline{OE}$ terminal

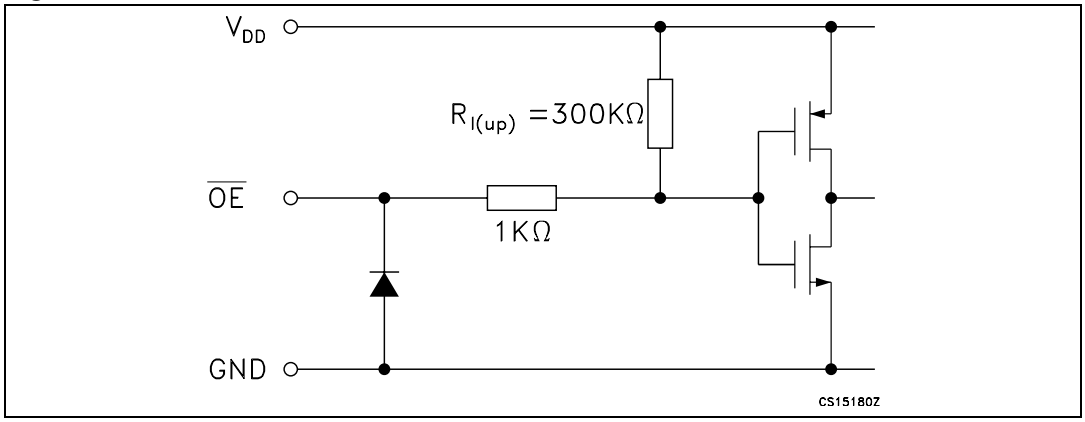


Figure 4. LE terminal

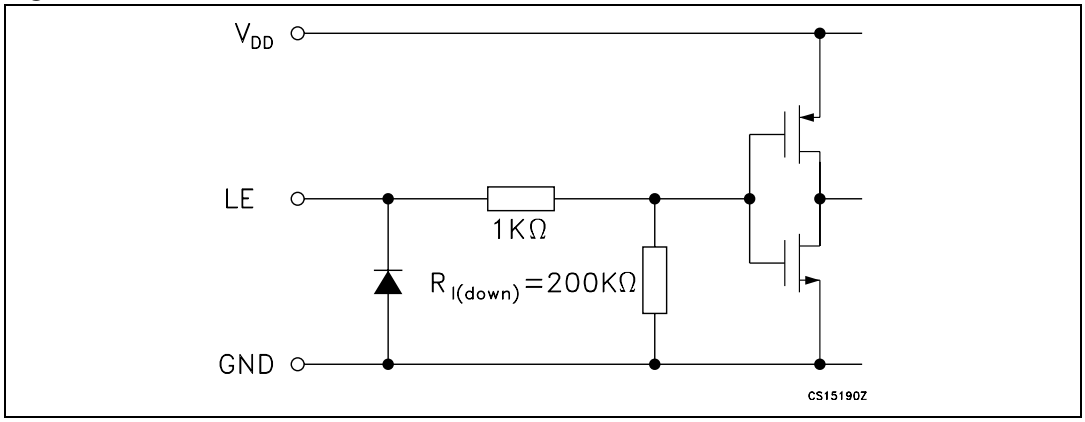


Figure 5. CLK, SDI terminal

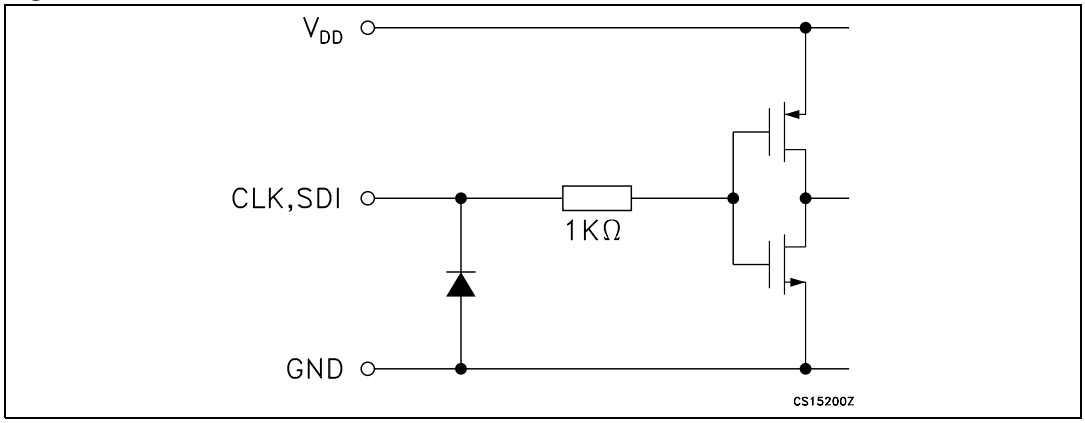


Figure 6. SDO terminal

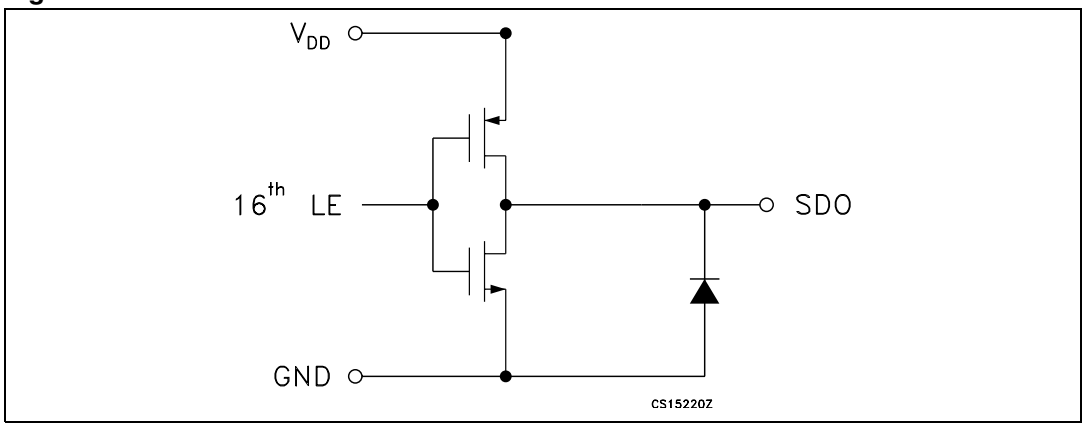
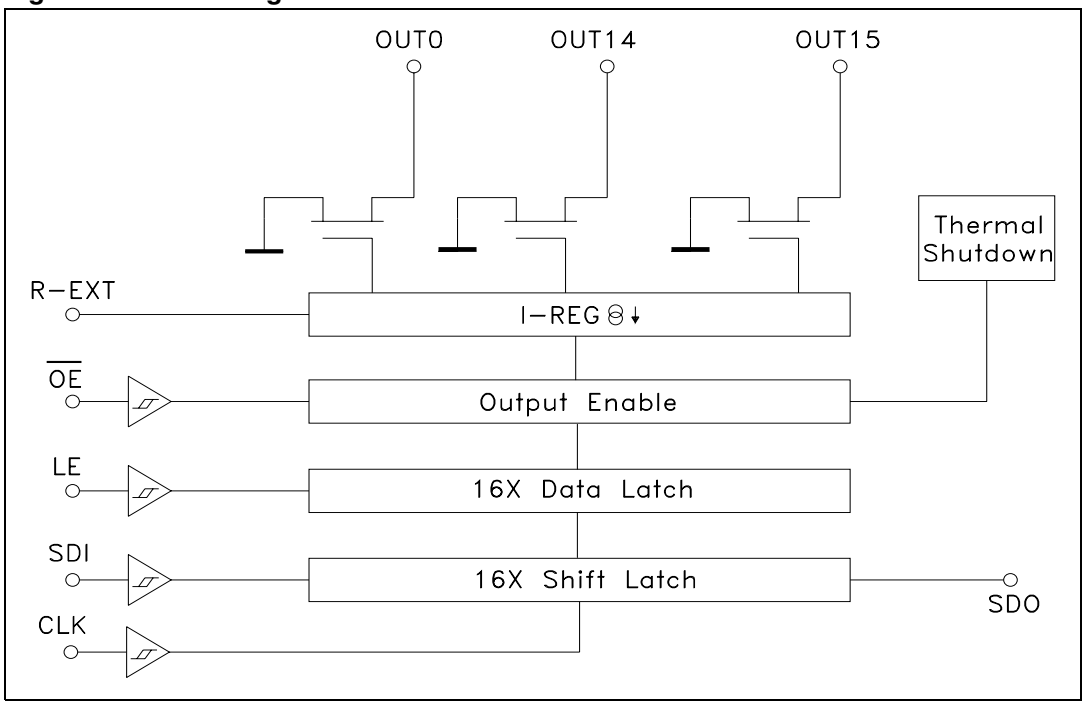


Figure 7. Block diagram



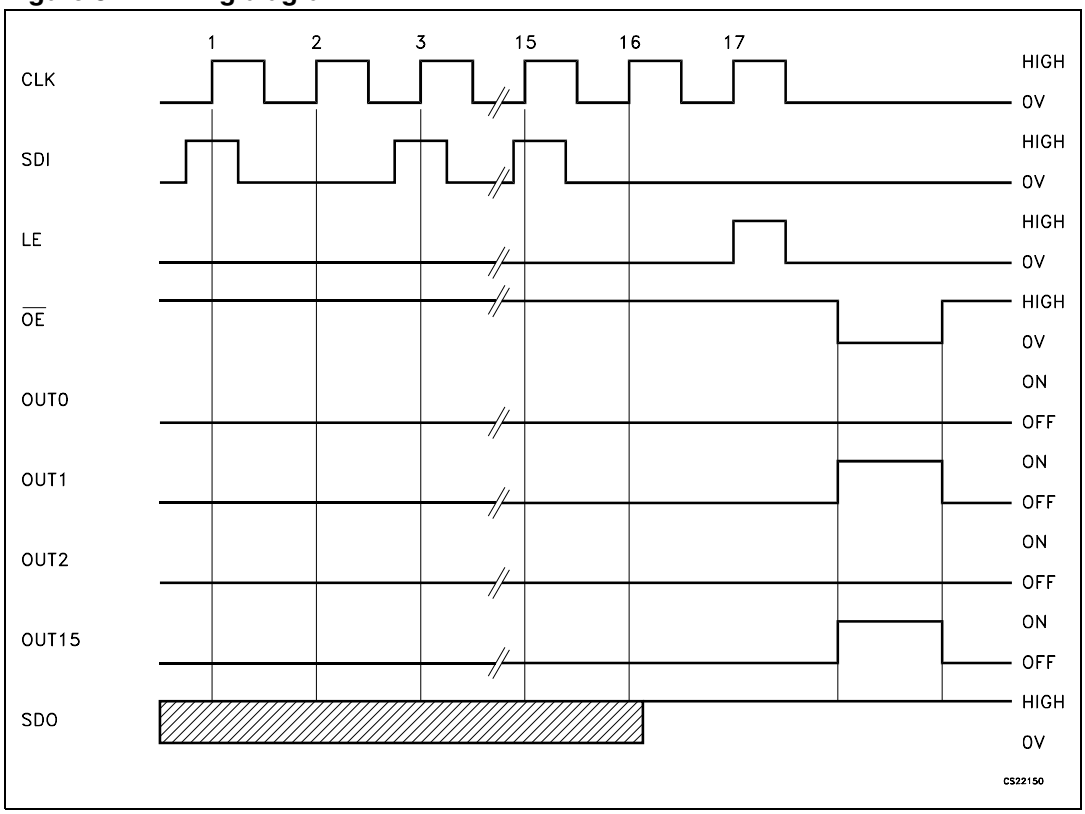
5 Timing diagrams

Table 9. Truth table

CLOCK	LE	$\overline{OE}$	SERIAL-IN	OUT0 ..... OUT7 ..... OUT15	SDO
⎍	H	L	Dn	Dn ..... Dn - 7 ..... Dn -15	Dn - 15
⎍	L	L	Dn + 1	No change	Dn - 14
⎍	H	L	Dn + 2	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
⎎	X	L	Dn + 3	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
⎎	X	H	Dn + 3	OFF	Dn - 13

Note: OUTn = ON when Dn = H OUTn = OFF when Dn = L

Figure 8. Timing diagram



Note: The latches circuit holds data when the LE terminal is Low.

1. *When LE terminal is at high level, latch circuit does not hold the data it passes from the input to the output.*
2. *When $\overline{OE}$ terminal is at low level, output terminals OUT0 to OUT15 respond to the data, either ON or OFF.*
3. *When $\overline{OE}$ terminal is at high level, it switches off all the data on the output terminal.*

Figure 9. Clock, serial-in, serial-out

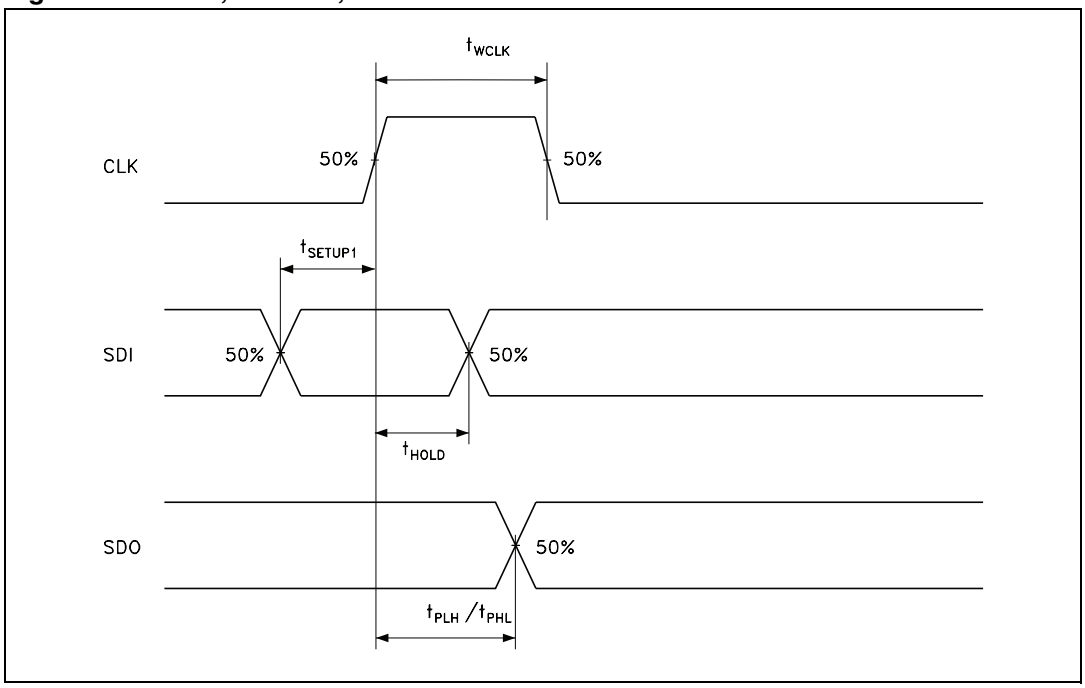


Figure 10. Clock, serial-in, latch, enable, outputs

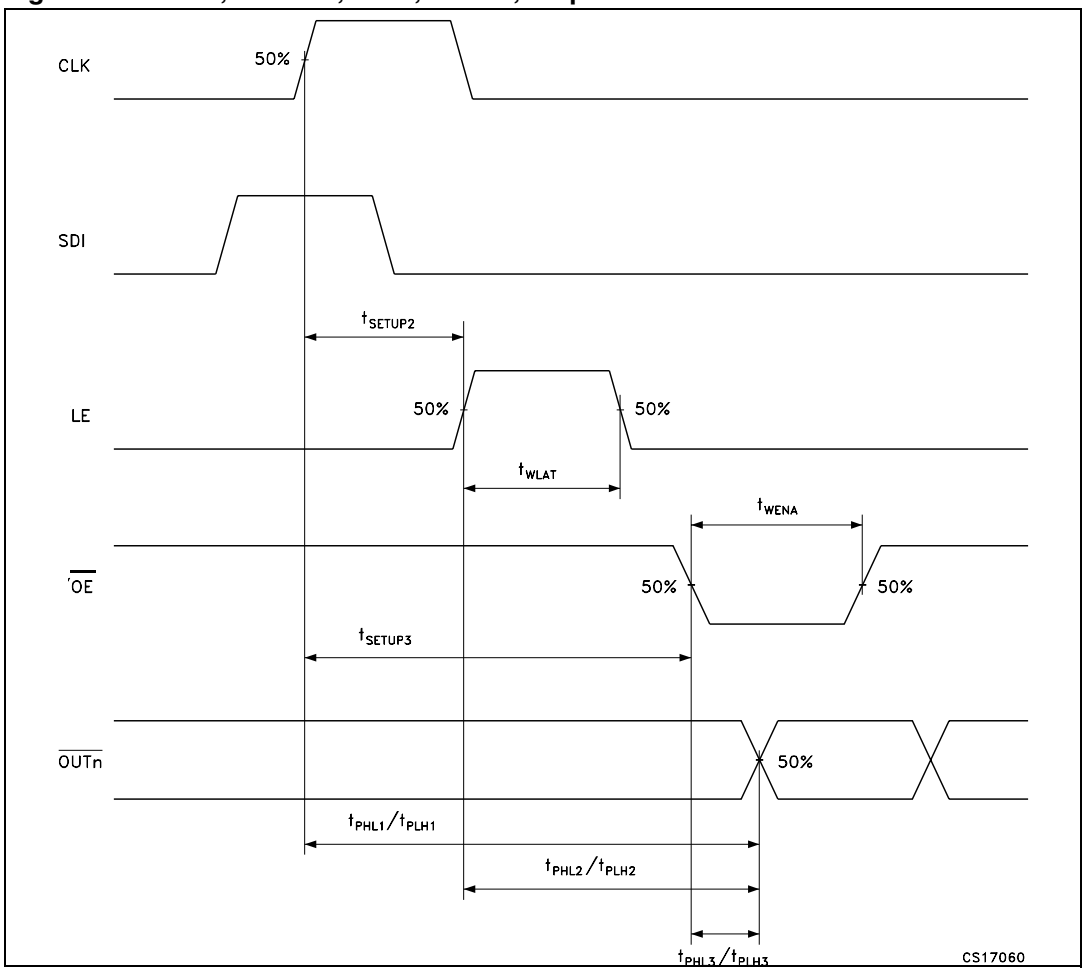
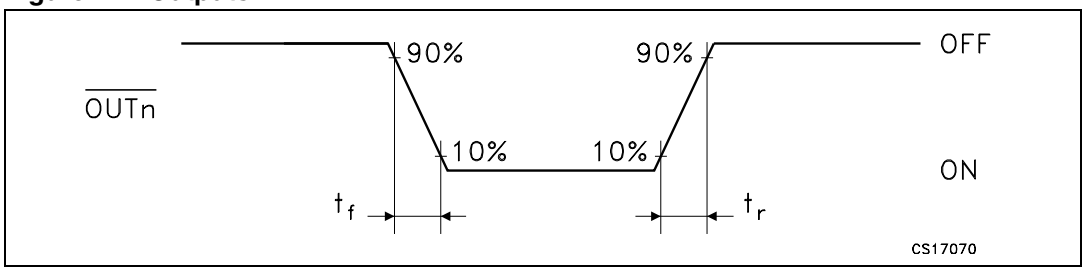


Figure 11. Outputs



6 Typical characteristics

Figure 12. Output current-R_{EXT} resistor

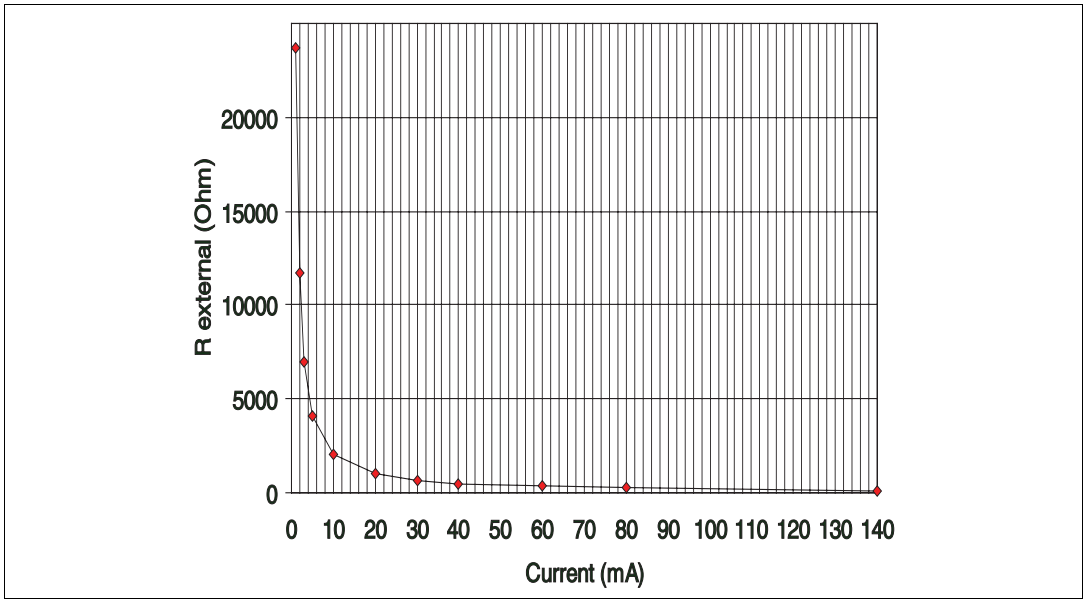


Table 10. Output current-R_{EXT} resistor

R_{EXT} (Ω)	Output current (mA)
2370	1
1173	2
6930	3
4090	5
2025	10
1006	20
667	30
497	40
331	60
245	80
136	140

Figure 13. Output current vs $\pm \Delta I_{OL}$(%) (temp.= 25°, Vdd = 5 V, pin= all outputs)

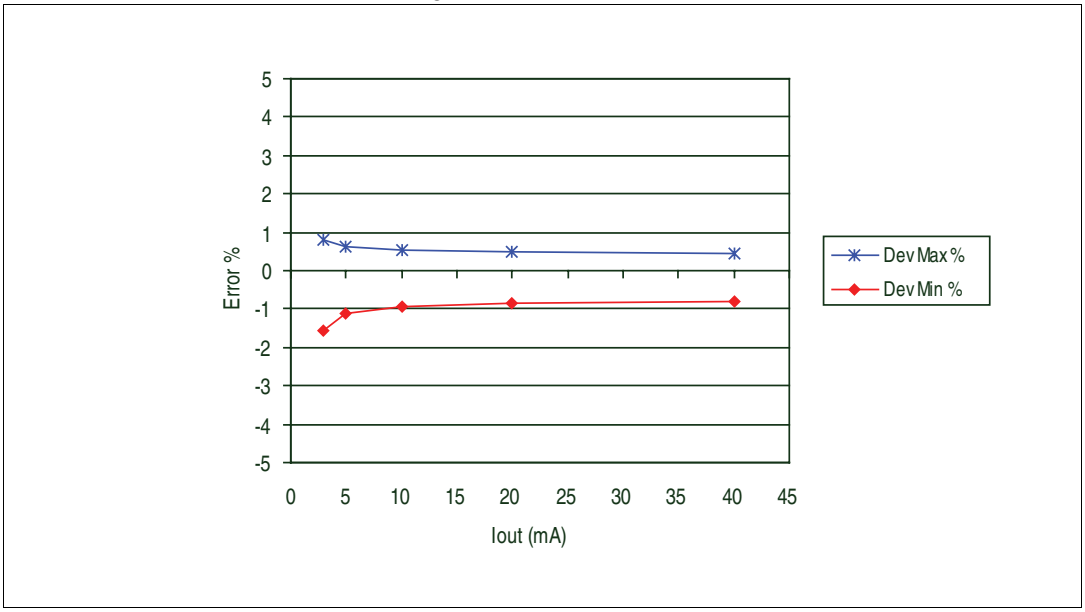


Figure 14. I_{SET} vs drop out voltage (V_{drop})

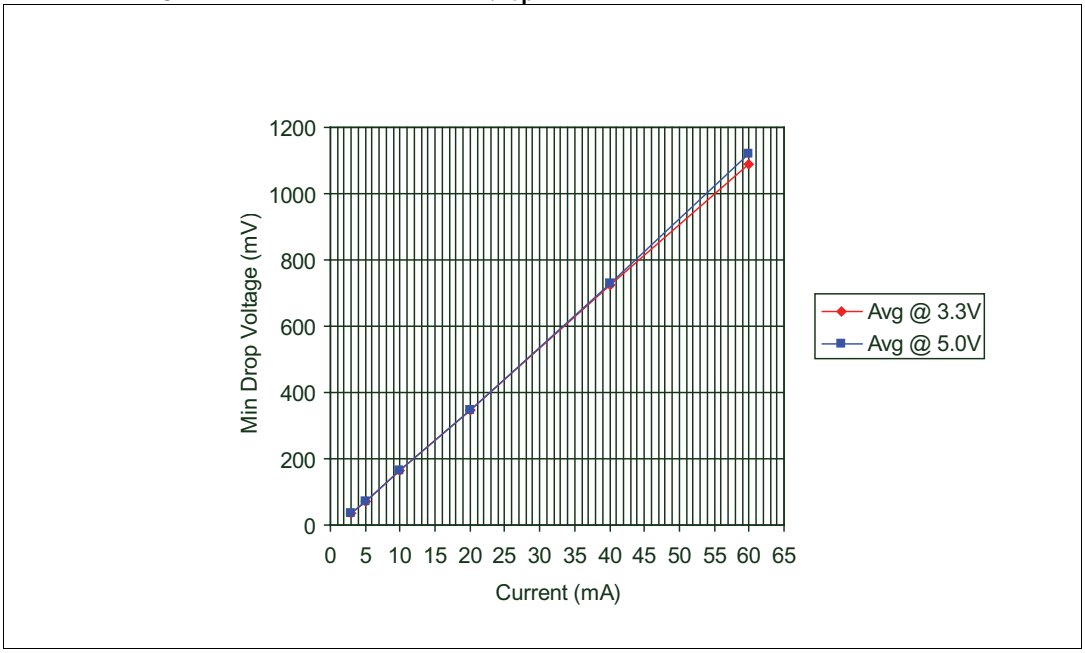


Table 11. I_{SET} vs drop out voltage (V_{drop})

Vdd (V)	Iset (mA)	Min (mV)	Max (mV)	Avg (mV)	Vdd (V)	Iset (mA)	Min (mV)	Max (mV)	Avg (mV)
3.3	3	35	37	36	5.0	3	37	37	37
	5	71	72	71		5	72	73	72
	10	162	165	163		10	162	164	163
	20	347	348	347		20	345	347	346
	40	724	724	724		40	725	728	726
	60	1080	1090	1080		60	1090	1140	1110

7 Test circuit

Figure 15. DC characteristic

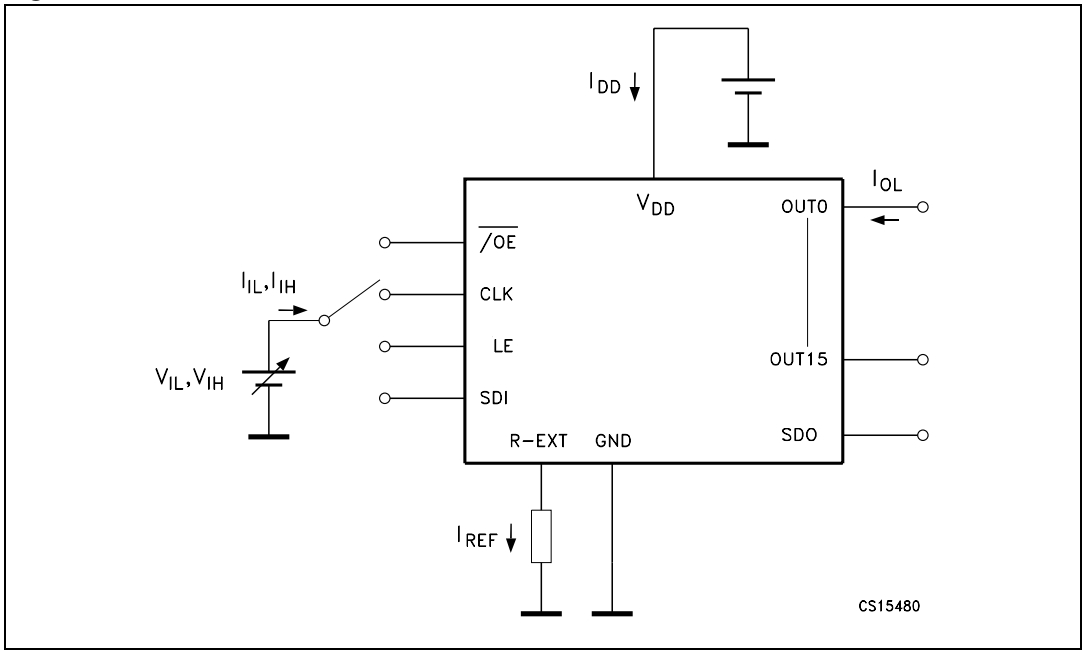


Figure 16. AC characteristic

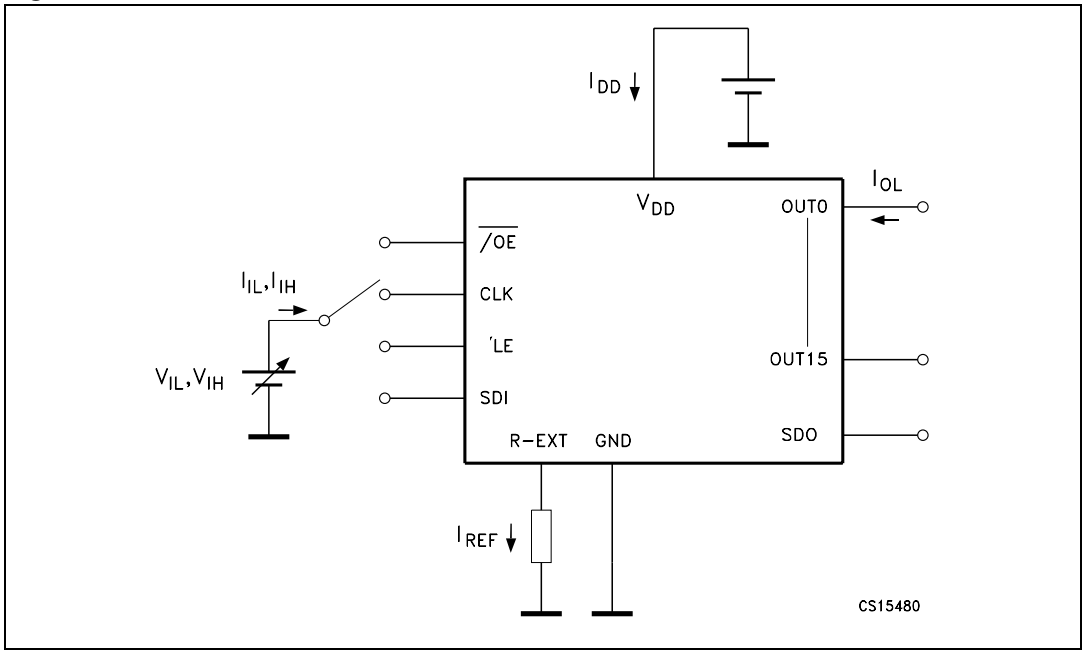
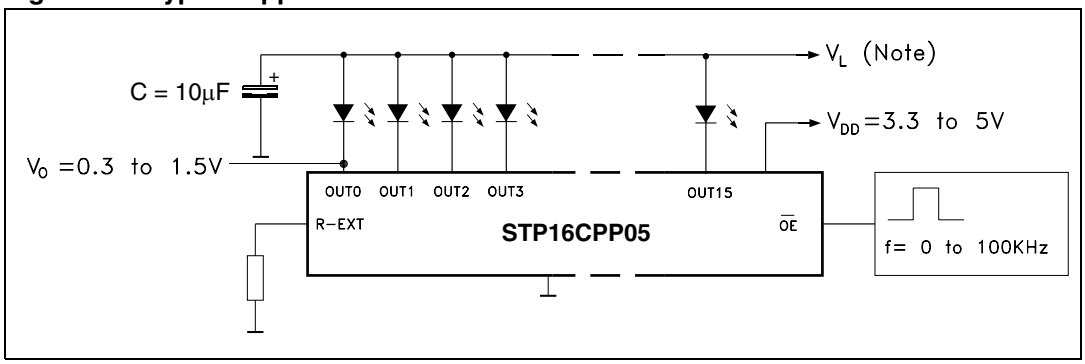


Figure 17. Typical application schematic



Note: *V_L will be determined by the V_F of the LEDs*

Test condition: Temp. = 25 °C, V_{DD} = 3.3 V, V_{IN} = V_{DD}, C_L = 10 pF, Freq. = 1 MHz, Ch1 = CLK, Ch2 = SDI, Ch3 = OUTn , Ch4 = V_{OUT}

Figure 18. Turn ON output current setup

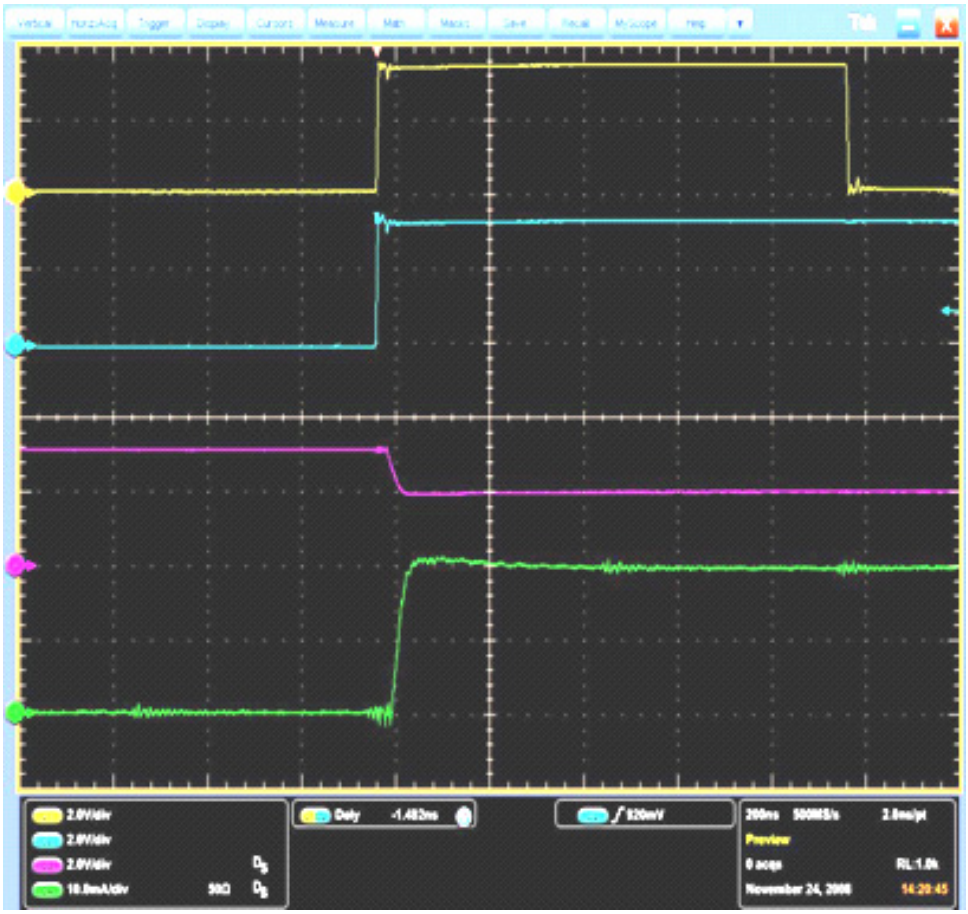
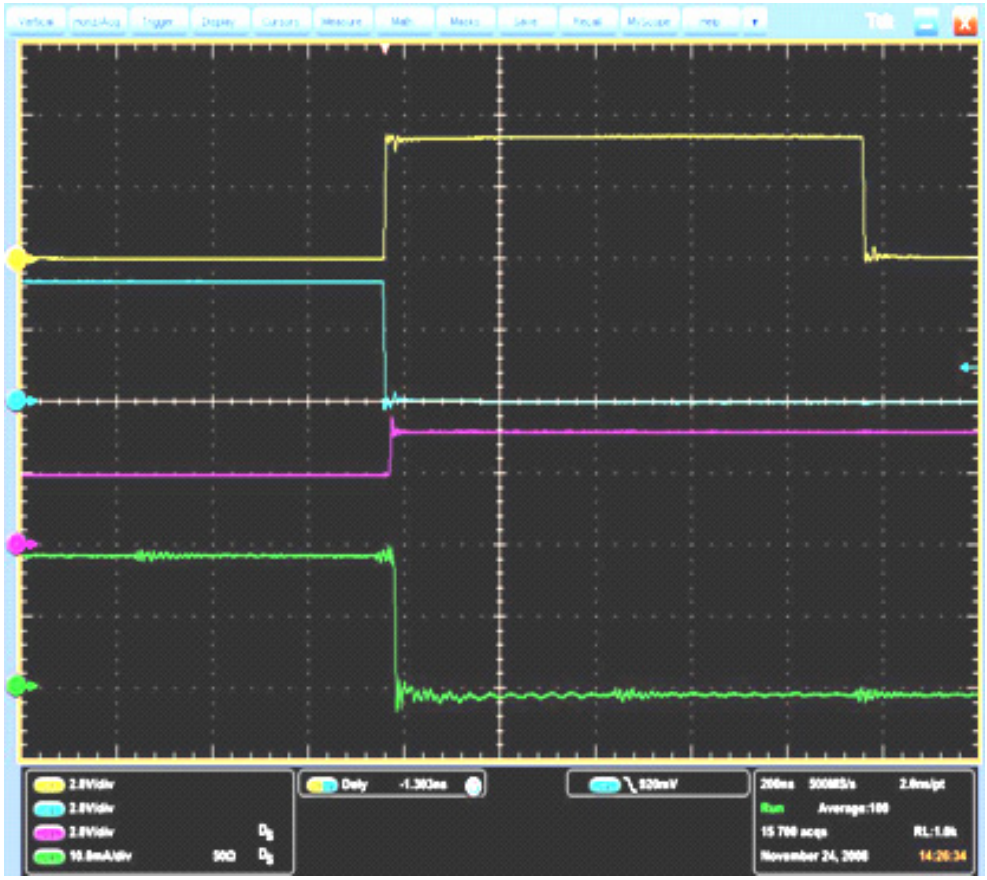


Figure 19. Turn OFF output current setup



8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 12. QSOP-24 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.54	1.62	1.73	0.061	0.064	0.068
A1	0.1	0.15	0.25	0.004	0.006	0.010
A2		1.47			0.058	
b	0.31	0.2		0.012	0.008	
c	0.254	0.17		0.010	0.007	
D	8.56	8.66	8.76	0.337	0.341	0.345
E	5.8	6	6.2	0.228	0.236	0.244
E1	3.8	3.91	4.01	0.150	0.154	0.158
e		0.635			0.025	
L	0.4	0.635	0.89	0.016	0.025	0.035
h	0.25	0.33	0.41	0.010	0.013	0.016
<	8°	0°				

Figure 20. QSOP-24 package dimensions

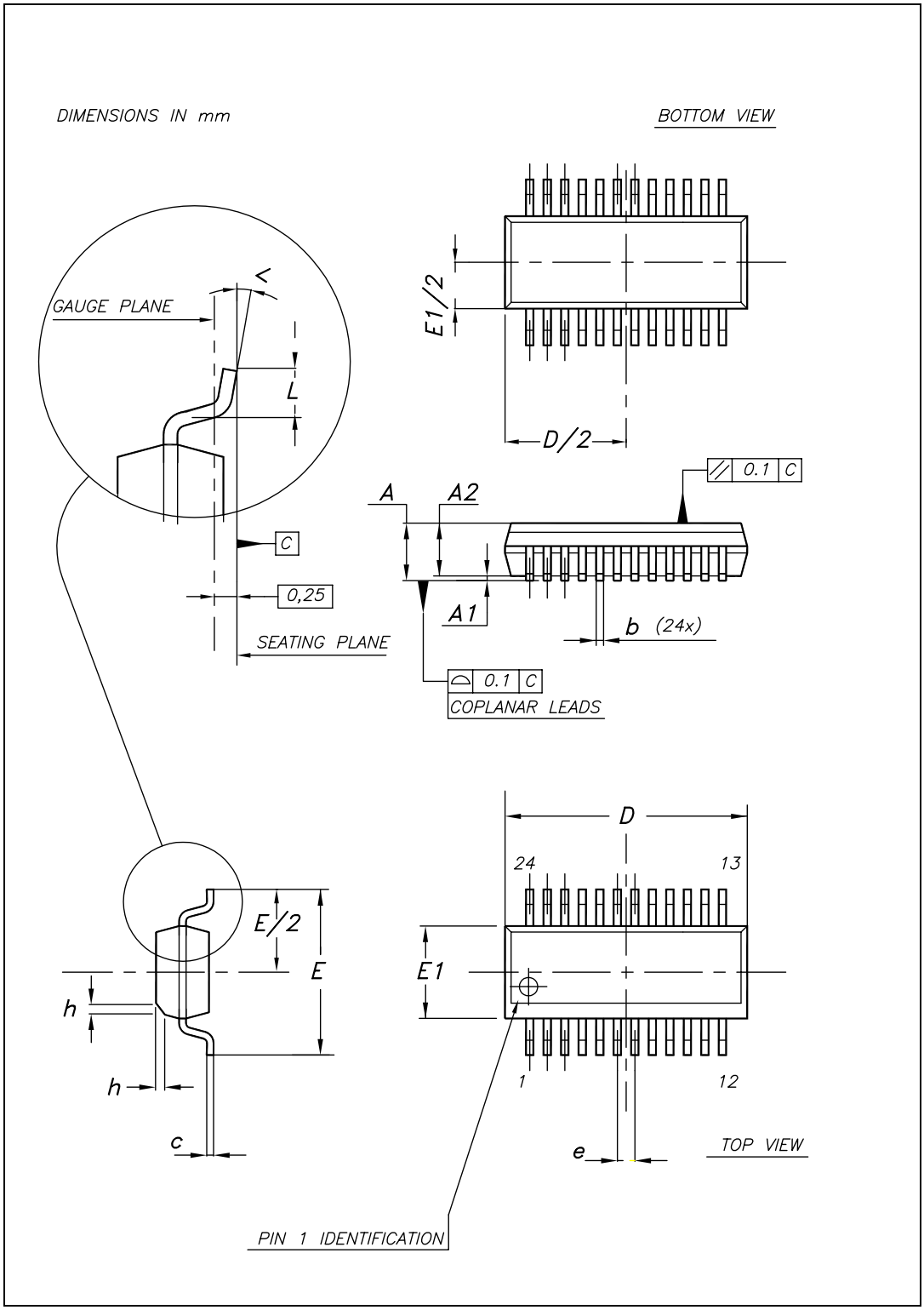


Table 13. TSSOP24 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.1			0.043
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	7.7		7.9	0.303		0.311
E	4.3		4.5	0.169		0.177
e		0.65 BSC			0.0256 BSC	
H	6.25		6.5	0.246		0.256
K	0°		8°	0°		8°
L	0.50		0.70	0.020		0.028

Figure 21. TSSOP24 package dimensions

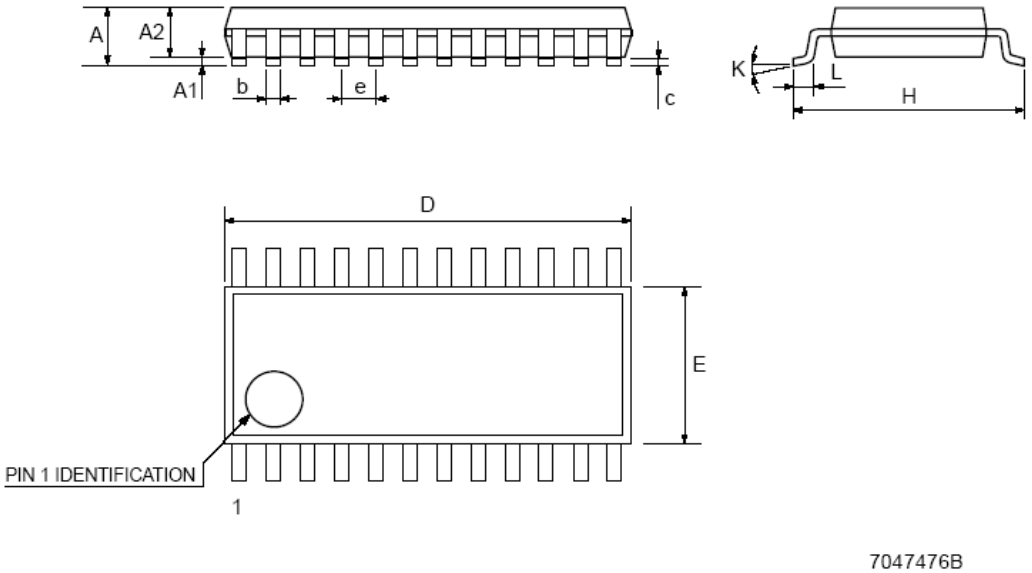


Table 14. Tape and reel TSSOP24

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	8.2		8.4	0.323		0.331
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

Figure 22. Reel dimensions

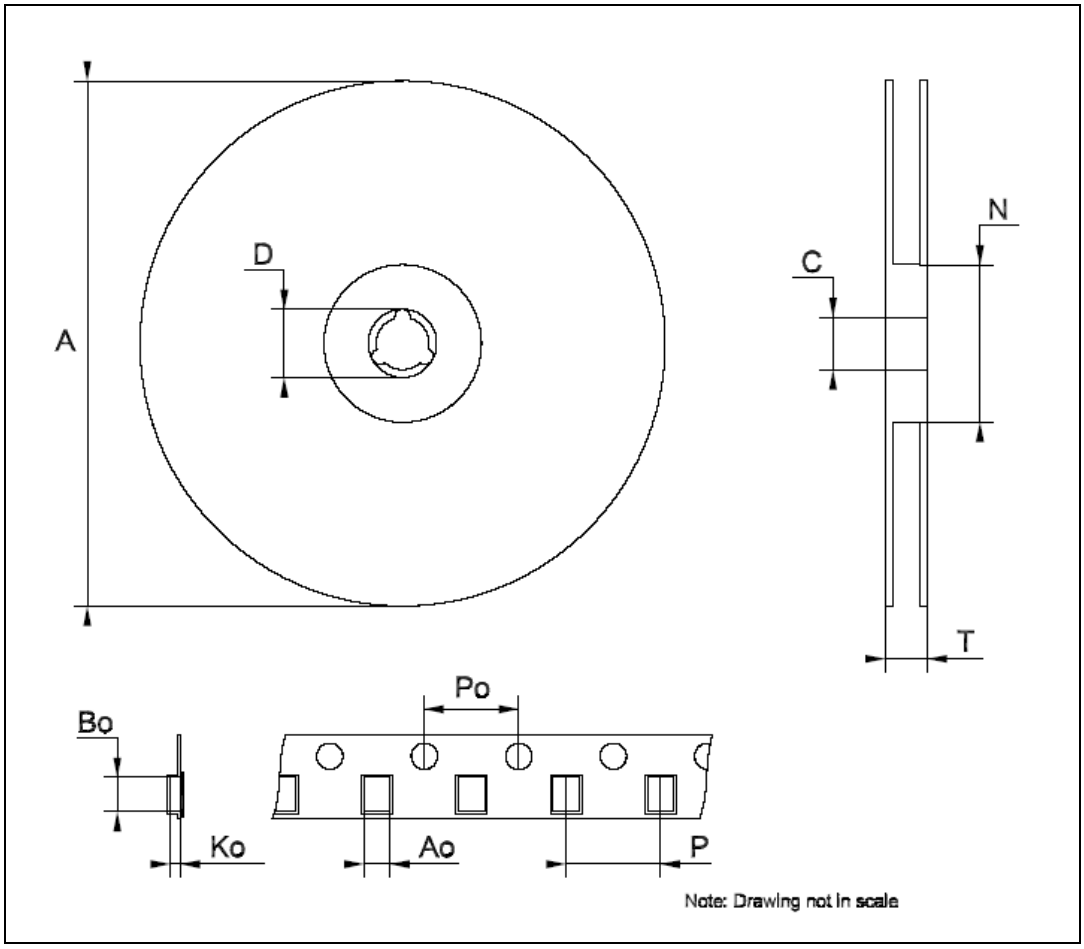


Table 15. SO-24 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45°(typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		13.97			0.550	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
S	°(max.) 8					

Figure 23. SO-24 package dimensions

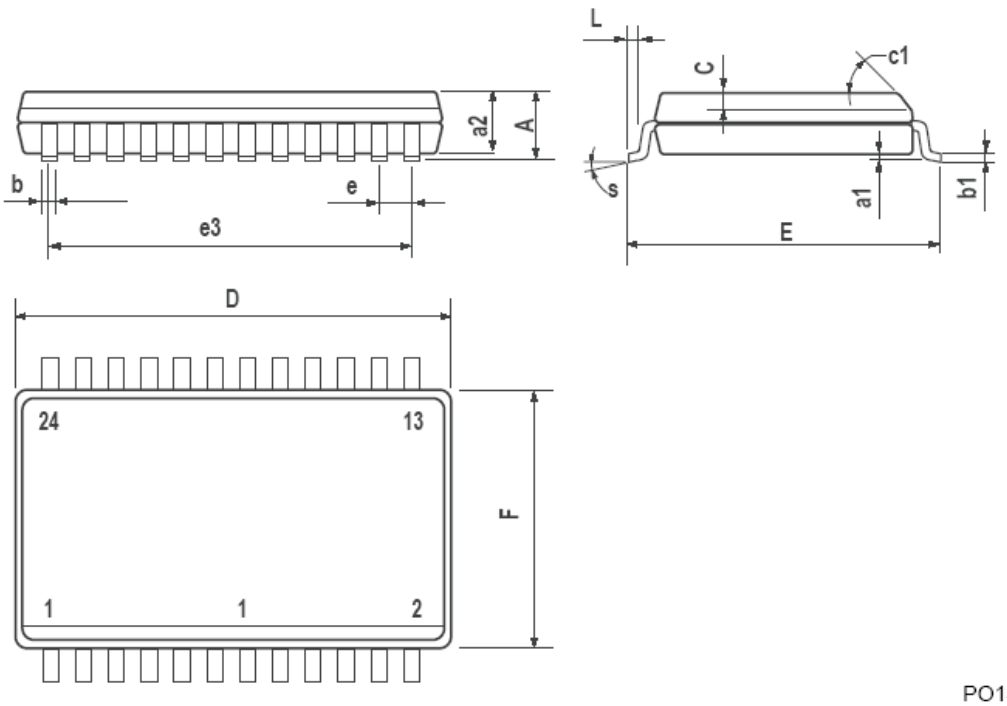


Table 16. Tape and reel SO-24

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	10.8		11.0	0.425		0.433
Bo	15.7		15.9	0.618		0.626
Ko	2.9		3.1	0.114		0.122
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

Figure 24. Reel dimensions

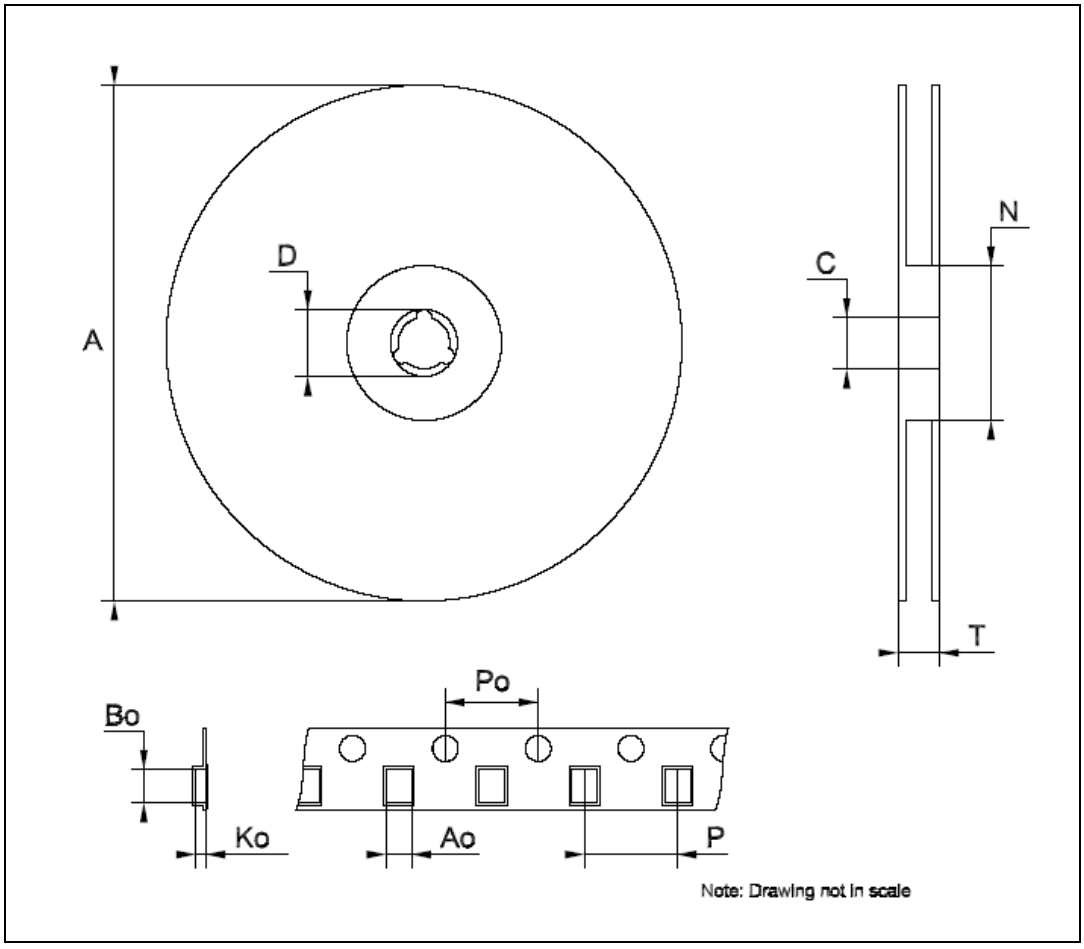
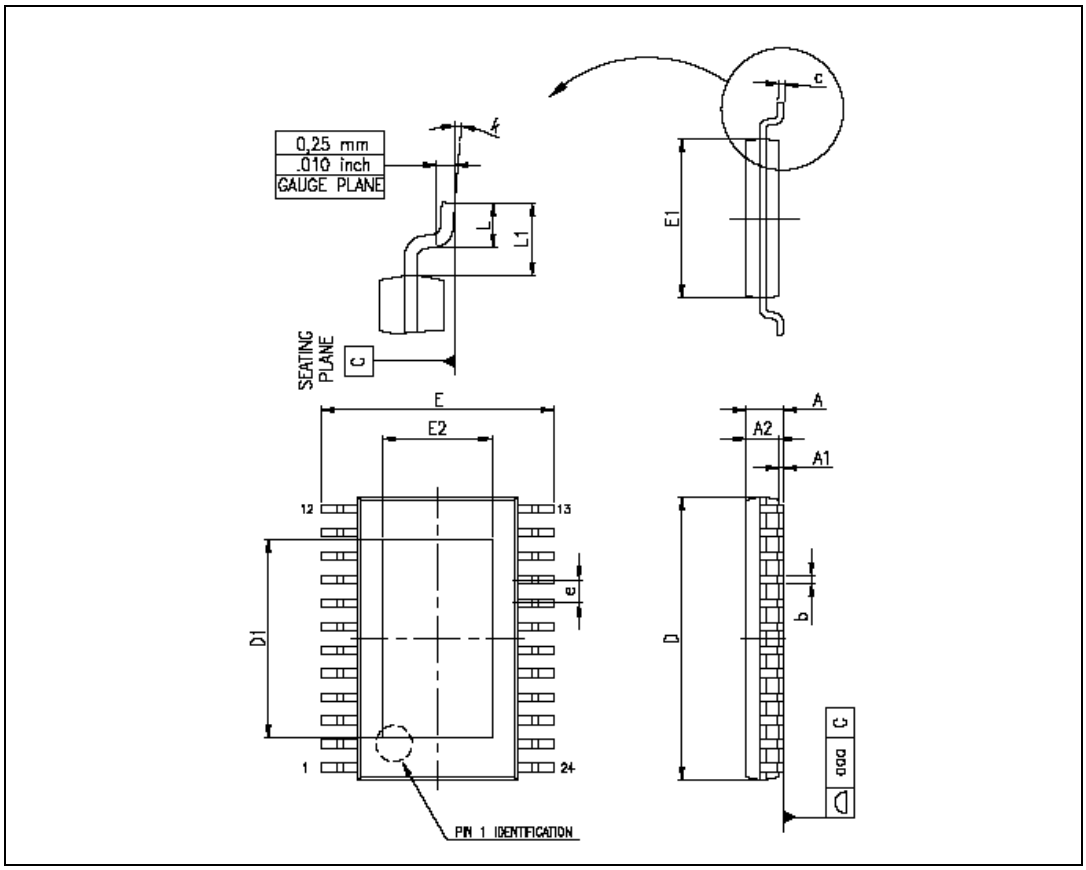


Table 17. TSSOP24 exposed-pad

Dim.	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.2			0.047
A1			0.15		0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	7.7	7.8	7.9	0.303	0.307	0.311
D1	4.7	5.0	5.3	0.185	0.197	0.209
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.5	0.169	0.173	0.177
E2	2.9	3.2	3.5	0.114	0.126	0.138
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

Figure 25. TSSOP24 dimensions



9 Revision history

Table 18. Document revision history

Date	Revision	Changes
11-Feb-2009	1	First release

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