IMP50E10 EPAC

Programmable Analog Signal-Conditioning Circuit

Electrically Programmable Analog Circuit

Introduction

The IMP50E10 EPAC™ is a user-programmable IC offering a variety of features targeted for use in analog signal conditioning applications where channel-dependent gain and offset settings are key system needs.

The IMP50E10 contains several analog and mixed signal functions and EEPROM. These functions are combined into modules with a variety of programmable electrical and functional characteristics such as gain, polarity, speed, power consumption, comparator hysteresis, filter cut-off, interconnect and output drive. (see ***Figure 1***.)

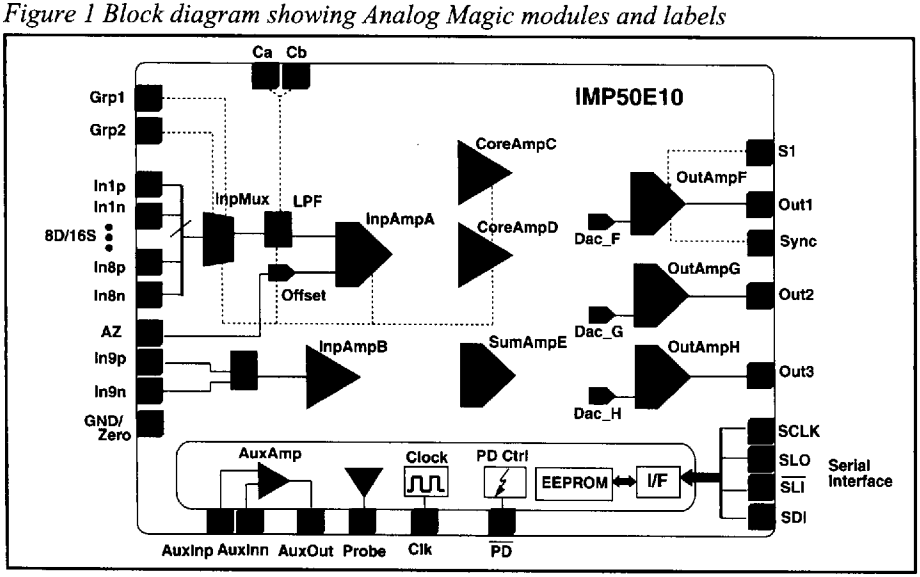
Programming EPAC devices is done via Analog Magic™, the design support software for the EPAC family, which is organized so that a new user can set-up, design and program an EPAC in less than one hour.

The IMP50E10 can simultaneously switch between up to four different gain, filter and offset settings, referred to as the "Group Switching" feature. It allows four different inputs or groups of inputs to each be assigned a different gain, offset, and filter cut-off frequency combination.

IMP50E10 Features

- Unequaled flexibility and ease of use in an analog IC
- Programmable power consumption, signal gains, filter cutoffs, offsets - hundreds of combinations
- Group switching - switch between up to four programmed combinations of gain, filtering and offset voltages (4-in-1)
- 12-bit linearity
- Low-power, switched-capacitor CMOS technology for battery-powered circuits
- Auto-Zero to within ±100μV
- Single-supply 5V operation
- Sleep-mode current under 70μA
- Unconditionally stable, oscillation-free

Figure 1 Block diagram showing Analog Magic modules and labels



IMP50E10 General Description

The user may program each IMP50E10 module according to the design requirements. Input signals pass through three basic sections:

- Input selection and filtering
- Internal Amplification
- Output conditioning

In addition, several modules exist outside of the normal signal flow. The analog modules on the chip are a mix of switched-capacitor and continuous-time circuits. The modules are discussed in detail in the Module section.

Input

Two high-impedance input amplifier modules (***InpAmpA*** and ***InpAmpB***) are available to amplify analog signals, offering gain settings from 0.5 to 10 in eight steps. Up to 16 single-ended or 8 differential input signals can be connected to an 8/16 channel multiplexer (***InpMux*** in ***Figure 1***) which is connected to Input Amplifier A (***InpAmpA***). One single-ended or differential signal can be connected to ***InpAmpB***.

Input signals containing substantial DC offsets are shifted by means of an offset module (***Offset***) in a range of steps up to a maximum voltage of ±2.54V.

System dynamic range is increased by summing the input of ***InpAmpA*** with the ***Offset*** module's output. The offset of the signal source can be eliminated and the remainder amplified and examined in finer detail by less-costly, low-resolution analog-to-digital converters.

Input signals 0.2V beyond zero and VDD are acceptable. An integrated single-pole continuous-time filter can be switched into the signal paths of ***InpAmpA*** and ***InpAmpB*** to limit the signal bandwidth to 15kHz, removing the need for an external anti-alias filter. The filter for ***InpAmpA*** is a separate module (***LPF***) and an optional external capacitor can be added to achieve different corner frequencies.

Internal Amplification

Three core amplifier modules (***CoreAmpC, CoreAmpD*** and ***SumAmpE***) are also available to amplify analog signals, offering gain settings from 1 to 10 in eight steps.

Output Conditioning

Programmable output modules can be used as amplifiers, voltage references, Track & Hold amplifiers, and comparators (with and without hysteresis). All output modules are connected to a 5-bit DAC (***Dac_F, Dac_G, Dac_H***), which can be used to either generate a reference voltage or to program the thresholds when in comparator mode.

OutAmpF can be configured as a track and hold amplifier, and ***OutAmpG***, ***OutAmpH*** can be set up as amplifiers or comparators. Hysteresis can be added in the comparator mode. The output level can also be DC-shifted by a 5-bit DAC. To eliminate offset voltage errors, an Auto-Zero loop can be connected from one of the input modules to any of the output modules.

Other Modules, Functions

The Auxiliary Amplifier module (***AuxAmp***) allows external feedback components to implement functions not found on the IMP50E10.

Even though all analog modules feature local offset cancellation and low-frequency noise suppression, an overall Auto-Zero loop is available which cancels offsets along a path from the multiplexer to any one of the three output modules. A dedicated pin is available to re-trigger the preprogrammed Auto-Zero sequence.

Many options exist to control power consumption of the chip. Unused modules are turned OFF. Either the entire chip or selected portions are temporarily powered-down, depending on commands sent to the chip.

The on-chip ***Clock*** module is used for internal timing control. The output of the clock is available at the Clk pin. The clock also operates in a Slave mode, with the chip clocked by a user-provided signal.

Table 1 IMP50E10 Modules and Programming Options

Module Name		Basic Programmability Overview
Super-Module		(Program Sub-Modules individually)
	InpMux	Group selection (Ext/Int), input mode (S/D)
	LPF	Filter by switching group (Int/Ext/Both/None)
	Offset	Step and Offset by switching group, Auto-Zero (On/Off), Zero reference (Ext/Int)
	InpAmpA	Gain by switching group, power down mode (Global/Selective)
InpAmpB		Gain, input filter (On/Off), power down mode
CoreAmpC		Gain by switching group, power down mode, polarity, connected to
CoreAmpD		Gain by switching group, power down mode, polarity, connected to
SumAmpE		Gain, polarity by input, power down mode, module interconnect by input
Dac_F		Reference voltage
Dac_G		Reference voltage
Dac_H		Reference voltage
OutAmpF		Function (Amp/Comparator), Track/Hold (On/Off), Zero-output (0V/2.5V), Filtering (On/Off), Hysteresis (On/Off), Turbo (On/Off), polarity, power down mode, module interconnect [selections available are function-dependent]
OutAmpF		Function (Amp/Comparator), Zero-output (0V/2.5V), Filtering (On/Off), Hysteresis (On/Off), Turbo (On/Off), polarity, power down mode, module interconnect [selections available are function-dependent]
OutAmpF		Function (Amp/Comparator), Zero-output (0V/2.5V), Filtering (On/Off), Hysteresis (On/Off), Turbo (On/Off), polarity, power down mode, module interconnect [selections available are function-dependent]
AuxAmp		Power down mode, Turbo (On/Off)
Clock		Power mode (Low/Normal), Mode (Master/Slave), divider ratio
Power_Down		Mode control for $\overline{PD}$ pin (Selective/Global)
Security		ReadBack mode (Open/Locked)

For more information on the modules, refer to the Module Section in this document or the EPAC User's Manual (available with the purchase of an EPAC Development System or EPAC Starter Kit).

The 3-wire serial interface consists of a chip select (SLI), data-in (SDI) and clock (SCLK). A fourth output is provided (SLO) which enables "daisy chaining" of multiple EPAC devices.

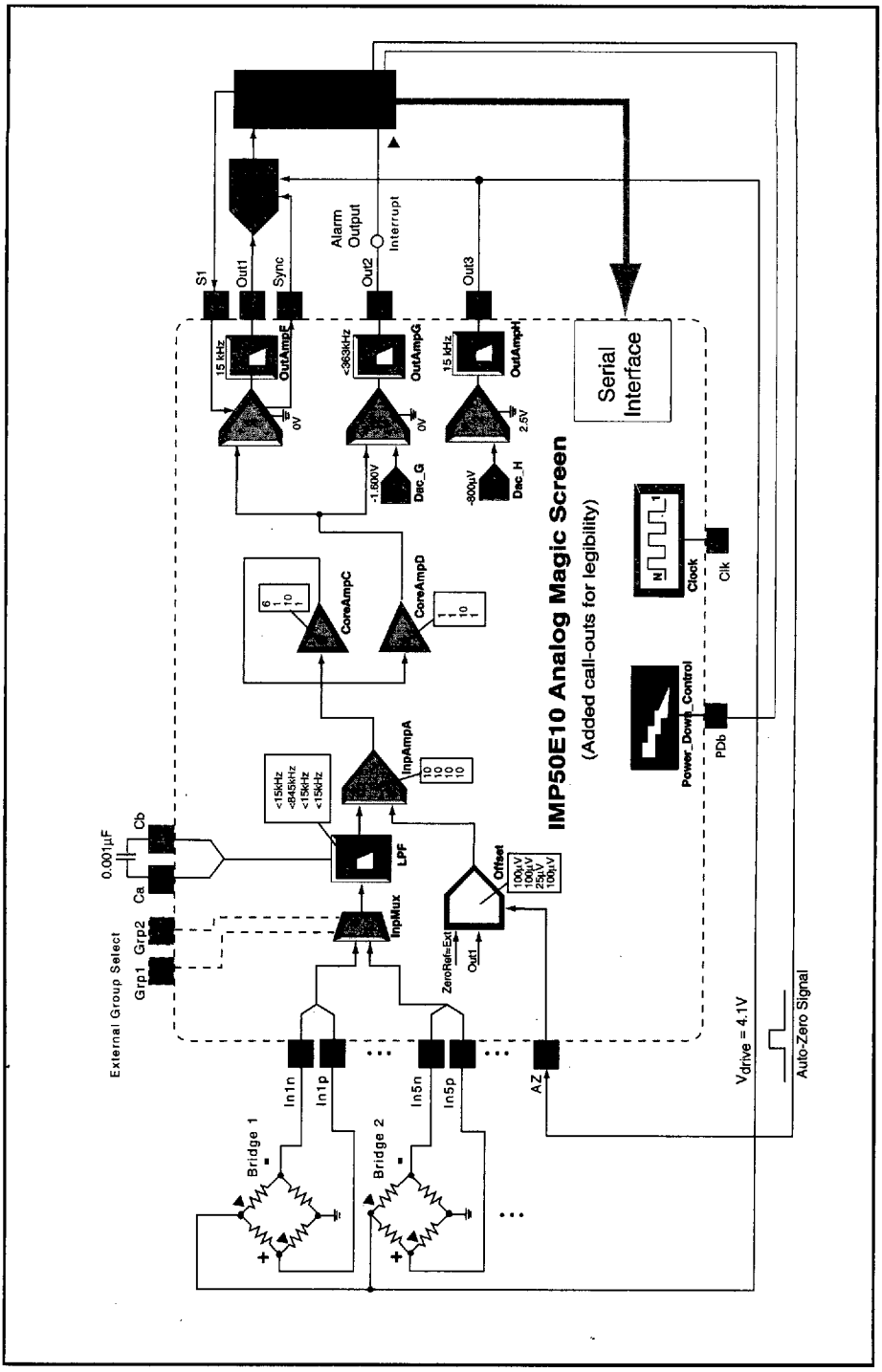
User-Programmable Functions

Hundreds of different gain, offset and filter combinations are available on the IMP50E10. ***Table 1*** lists the programming options.

Module options, such as programmable gain, are specified via pop-up menus in Analog Magic. Each of the available modules used in the design can be activated by a single left mouse button click, and its options programmed by a rapid double-click of the left mouse button to raise the pop-up menu.

Modules can be interconnected in various ways without any impact on performance or stability. Routing of signals is automatic and fully supported by Analog Magic. The user can implement or change an analog function, download it and immediately test it in the system.

Figure 2 Sample application - EPAC connected in a circuit with Analog Magic-type window showing actual interconnection and parametric specification



Applications

- Automotive diagnostic equipment
- Battery chargers
- Data acquisition
- Food processing equipment
- Medical instrumentation
- Non-contact gauging and distance measurement
- Pollution control
- Reconfigurable test equipment
- Remote data logging
- Process control
- Sensor signal conditioning
- UPS control

Application Example

Figure 2 shows a low power, fully programmable analog front end system configured to:

- remove offset and drift voltages
- supply drive to the bridges
- provide filtering and gain
- implement a track and hold circuit
- provide a watchdog output.

Note that input signals with different magnitudes are multiplied by different gains without needing to reprogram the chip. This circuit can be expanded beyond the two inputs shown. For more information, refer to ***Application Brief #1, Connecting the IMP50E10 to Bridge Circuits*** and ***Application Brief #3, IMP50E10 Group Switching Eases Signal Conditioning.***

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IMP50E10 Modules

Input Multiplexer Module

Key features:

- 8 differential or 16 single-ended inputs
- Channels are selected through serial I/O
- Channels are evenly divided into 4 groups
- Groups are selectable through the serial interface or through the Grp select pins
- Built-in zero-reference for Auto-Zero

Description

InpMux selects one of 16 single-ended or 8 differential mode input signals and passes it to the ***LPF*** module.

Input channels are evenly divided into four groups, so there are four channels (input pins) per group in single-ended mode and two channels (two 2-input pin pairs) per group in differential mode. The use of this feature is described in the following modules which support group switching: ***InpAmpA, LPF, Offset, CoreAmpC,*** and ***CoreAmpD***.

Input channels (single-ended or differential mode) can be selected through the serial interface by a simple command. Two external group selection pins, Grp1 and Grp2 (shown in ***Figure 3***), can also be used to select between one of four input channels by switching between the four groups (see ***Table 3***). For more information of group and channel selection, please see ***Application Brief 3, IMP50E10 Group Switching Eases Signal Conditioning,*** and ***Application Note 22, Serial Programming for the IMP50E10.***

InpMux is protected against over-voltages by diode clamps to the supply rails.

The Differential Mode is diagrammed in ***Figure 4.*** When operating in single-ended mode, it is necessary to ground the GND/ Zero pin (***Figure 5***).

Figure 3 Input Multiplexer Module (InpMux)

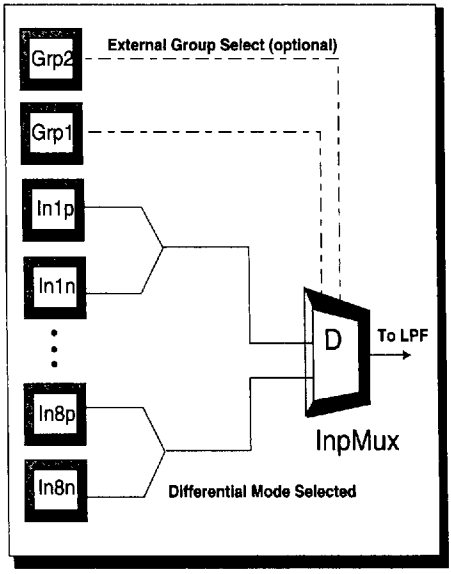


Table 3 Inputs, Channels and Grp1, Grp2

Input Pin Desig. #	MUX Setting: Single-Ended Channel #	MUX Setting: Differential Channel #	Assoc. Group #	External Group-Select Pins: Grp1	Grp2
In1n	1	1	1	0	0
In1p	2				
In2n	3	2			
In2p	4				
In3n	5	3	2	1	0
In3p	6				
In4n	7	4			
In4p	8				
In5n	9	5	3	0	1
In5p	10				
In6n	11	6			
In6p	12				
In7n	13	7	4	1	1
In7p	14				
In8n	15	8			
In8p	16				

Figure 4 Differential Mode Block Diagram

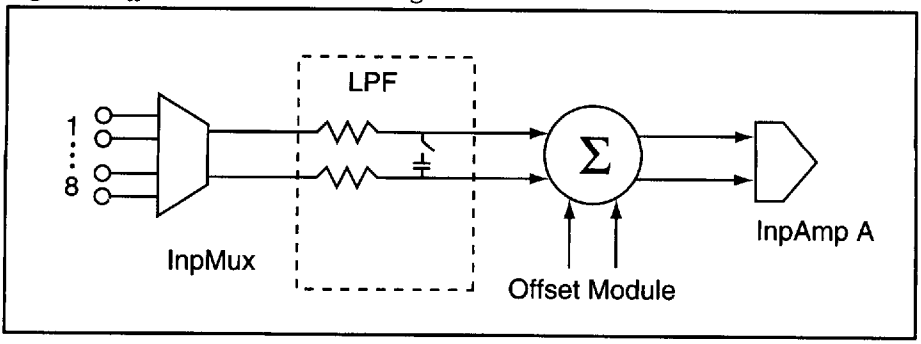
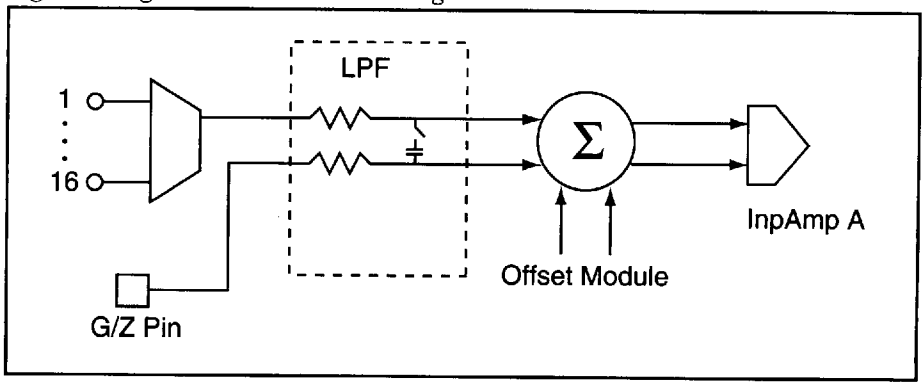


Figure 5 Single-Ended Mode Block Diagram



Low Pass Filter (LPF) Module

Key features:

- Select the internal capacitor (f_c = 15kHz) or provide an external one for lower cutoff frequencies
- Filters both differential and single-ended signals
- Zero DC power consumption (passive filter)
- Single-pole RC filter architecture with 6dB per octave roll-off
- Utilizing group switching, the internal or external capacitor option can be programmed differently depending upon which group is used

Description

This integrated single-pole continuous-time filter can be switched into the signal path to obtain a filter corner frequency of 15kHz, removing the need for an external anti-alias filter. Optionally, an external capacitor can be placed between the Ca and Cb pins to obtain corner frequencies between 845kHz and near zero. The ***LPF*** module (***Figure 6***) is in the path between the ***InpMux*** and ***InpAmpA*** modules.

This module can have the associated internal capacitor switched on or off, in addition to switching the external capacitor option on or off (***Figure 7***).

Group switching allows these options to be changed on the basis of the currently selected input channel. To find the corner frequency when using an external capacitor, apply one of the formulas:

Calculating f_c using an external capacitor:

Internal capacitor on ($C_{internal}$ = ON):

$$C_{external} = \left(\frac{1}{2\pi\,(142 * 10^3) * f_c} \right) - 75pF$$

Internal capacitor off ($C_{internal}$ = OFF):

$$C_{external} = \frac{1}{2\pi\,(142 * 10^3) * f_c}$$

where f_c is the desired corner frequency.

Figure 6 Low Pass Filter Module (LPF)

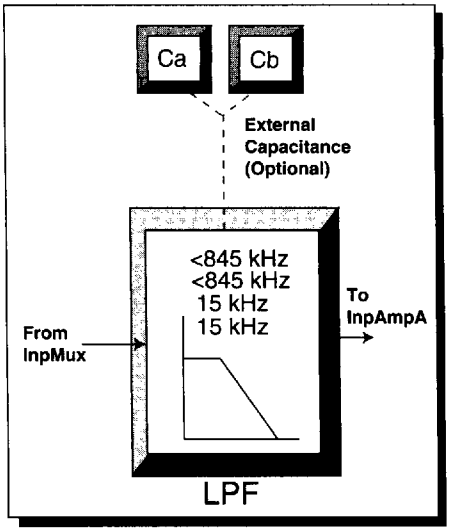
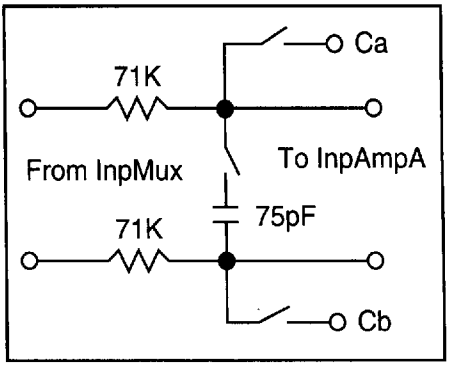


Figure 7 Internal diagram of LPF



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Offset Module

Key features:

- 10 bit DAC (7 for magnitude + 1 for sign + 2 for range)
- 4 step sizes (25µV/100µV/1mV/20mV)
- ±127 steps, true bipolar operation with no missing codes
- Utilizes group switching so that offsets can be programmed to different voltages depending upon which group is used
- Auto-Zero capability between InpMux and any Output Module (F, G, or H)

Description

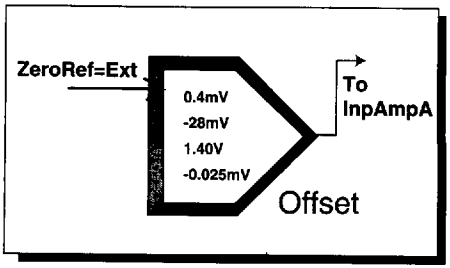
The ***Offset*** module (***Figure 8***) is used for either Auto-Zero or D.C. level shifting of an input signal that is routed through the Input Multiplexer Module. The output of this module is fed to a non-inverting input of ***InpAmpA***. The ***Offset*** module is a 10 bit D/A converter with 7 magnitude bits, 2 range bits, and 1 polarity bit. The heart of the module is a successive approximation register. It shares the same internal reference as the output DACs. For an explanation of the Auto-Zero function, see the Auto-Zero feature description below.

The two range bits allow four different ranges:

Range	LSB
±3.125mV	25µV
±12.7mV	100µV
±127mV	1mV
±2.54V	20mV

The ***Offset*** module supports the group switching feature. As a DAC, this allows four different voltage levels to be set. In Auto-Zero mode, this allows different sensitivities to be set for different groups of input channels.

Figure 8 Offset module (Offset)



Auto-Zero

The Auto-Zero capability is used to eliminate offset errors that originate from either internal or external sources. After an Auto-Zero sequence, typical input referred offset levels are 100µV.

Referring to ***Figure 9***, notice the modules named Auto-Zero Comparator and SAR. ***These modules reside on chip, but are not shown in diagrams of the IMP50E10*** because the user does not interact with these modules directly. They are only used for the Auto-Zero function.

First, the chip sets the output module being Auto-Zeroed to a zero reference level of 2.5V (see description of the output modules for an explanation). This occurs even if the user has selected a zero reference of 0V. So, an offset free system would have a 2.5V output at this point. After the Auto-Zero sequence, the zero reference level reverts to what was programmed by the user.

Next, this signal is routed to the comparator. One input of the comparator is tied to the 2.5V on-chip reference. The output of the comparator signals the Successive Approximation Register (SAR) if the signal being monitored from the output module is higher or lower than the zero reference of 2.5V. The SAR then increments or decrements the voltage being output by the ***Offset*** module. This voltage propagates through the chip, where eventually this new voltage is again compared to the zero reference level.

There are a number of additional options with the Auto-Zero feature. The Input Multiplexer Module (***InpMux***) can be set to use the currently selected channel as the input signal source. This effectively removes this signal, which, for example, could be the output of an unbalanced Wheatstone Bridge. ***InpMux*** can also be set for an internal signal source, in which case the input is switched so that only internal offsets are removed.

The input to the Auto-Zero Comparator (Out1, Out2, Out3 or Out2-Out3) can also be selected. Out2-Out3 Auto-Zeros to the difference between ***OutAmpG*** and ***OutAmpH***. This is useful if these two modules are set up as a differential output.

An Auto-Zero sequence can be initiated through either the serial interface or by applying a positive going, return to zero pulse of at least 5µs duration to the external pin named AZ. At the clock rate of 500kHz, an Auto-Zero takes approximately 21ms to complete. When initiating an Auto-Zero through the serial interface, the external AZ pin must be grounded. The sequence stops automatically upon finding the minimum offset or reaching the end of the offset-module's range.

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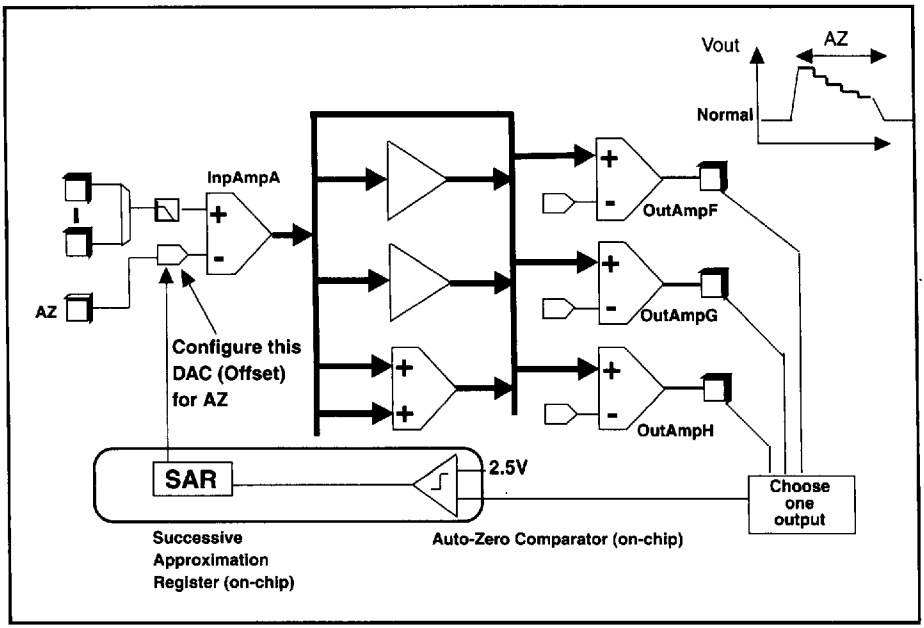
Figure 9 Automatic Offset Calibration (Auto-Zero)



Input Amplifier Module A

Key features:

- Accepts single-ended and differential input signals
- Local auto-zero and 1/f noise cancellation
- Gain choices available: 0.5, 1, 2, 3, 4, 6, 8, 10
- Utilizes group switching so that up to four different gain settings can be programmed, with the amplification level depending upon which group is selected.

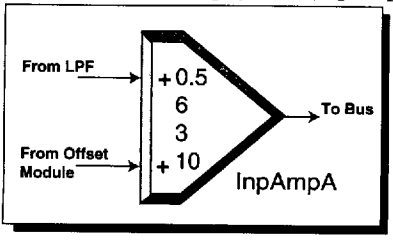
Description

InpAmpA is one of two input paths into the IMP50E10, with the other path going through ***InpAmpB***. This module (***Figure 10***) is essentially an instrumentation amplifier with programmable gain. Gain settings include 0.5, 1, 2, 3, 4, 6, 8, and 10. ***InpAmpA*** also supports the group switching feature, so different gains can be applied to signals which are in different groups. This does not require re-programming. Once the chip is orginally programmed, it automatically switches to the gain which is programmed for that group.

A second non-inverting terminal is provided which sums the output of the ***Offset*** module with the input signal. This summing is performed before any amplification is done. With the ***Offset*** module suitably programmed, this allows the IMP50E10 to automatically eliminate offset errors. (Refer to the previous section on Auto-Zero).

Low-power mode is supported, as described in the clock module section. This is a switched capacitor module; in normal power mode there is a propagation delay of 4µs, while in low power mode there is a 32µs delay. Global and selective power down options are supported. (See Power Management.)

Figure 10 Input Amplifier A (InpAmpA)

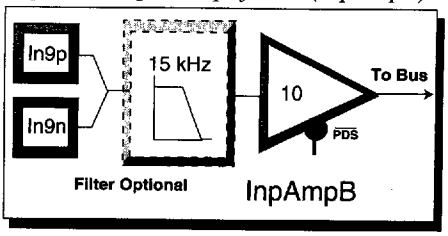


Input Amplifier Module B

InpAmpB is physically identical to ***InpAmpA***, except that group switching is not supported. The optional low-pass filter is integrated into the amplifier, rather than specified as a separate module (***Figure 11***). The corner frequency is fixed at 15kHz when the filter is on.

This module has a dedicated differential input, channels In9p (9 positive) and In9n (9 negative). If a single-ended input of inverting or non-inverting polarity is desired, ground the unused pin of this differential pair.

Figure 11 Input Amplifier B (InpAmpB)



Core Modules
- Core Amplifier Modules C & D

Key features:

- Programmable gain settings of 1, 1.5, 2, 3, 4, 6, 8, 10
- Choose inverting or non-inverting configurations
- Utilizes group switching so that up to four different gain settings can be programmed, with the amplification level depending upon which group is selected
- Cascadable to increase total gain
- Local offset and 1/f noise cancellation

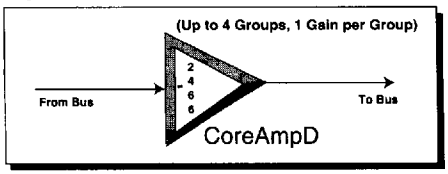
Description

The core amplifiers (***CoreAmpC*** and ***CoreAmpD, Figure 12***) feature programmable gain, power-down mode, signal polarity, and input signal source. Typically, these modules are used to supply more gain to a signal. Gain settings include 1, 1.5, 2, 3, 4, 6, 8, and 10.

When these low power CMOS switched-capacitor modules are operated in normal power mode (this setting is controlled by the clock module), it requires 4µs to clock a signal through from input to output. Low power mode requires 32µs. Global and selective power down options are supported, as described in the description of power management.

These modules support the powerful group switching feature, which allows different gain options to be used depending upon which input channel is selected. The signal polarity is programmed to be either inverting or non-inverting. The input signal source can be ***InpAmpA*** or ***InpAmpB***, ***SumAmpE***, or another core amplifier.

Figure 12 Core Amplifier (CoreAmpD)



Core Modules
- Summing Amplifier Module E

Key features:

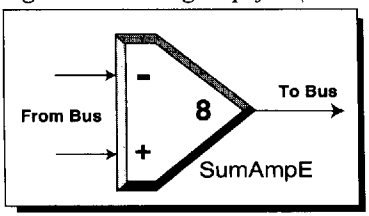
- Programmable gain settings of 1, 1.5, 2, 3, 4, 6, 8, 10
- Choose to utilize one or two inputs and inverting or non-inverting configurations
- Cascadable with other core amplifiers to increase total gain
- Local offset and 1/f noise cancellation

Description

Summing Amplifier ***SumAmpE*** is similar to modules ***CoreAmpC*** and ***CoreAmpD***, except that this module can accept either one or two input signals (***Figure 13***). Typically, this module is used to supply gain to the sum or difference of two signals. An example of an application requiring this would be subtracting the cold-junction compensation voltage from a thermocouple.

Each input signal can be connected to other module outputs, and each input has its own polarity option. Programmable options include: gain, power-down mode, signal polarity, and input signal source. Please note that with the default sampling clock frequency of 250kHz, it requires 4 microseconds to clock a signal through from input to output. Also, this module can be utilized in low-power mode.

Figure 13 Summing Amplifier (SumAmpE)



Output Modules F, G, H

Key features:

- Use as an amplifier, Track and Hold, comparator, or reference
- Fixed ±2 gain amplifier
- Single-ended output to VSS or 2.5V
- Optional LP-filtered output (15kHz)
- Track&Hold mode with dedicated control pins (***OutAmpF*** only)
- Comparator with optional 75mV hysteresis
- Optional enhanced slew rate capability (Turbo mode)

Description

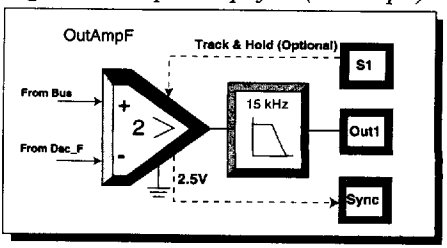
Programmable output modules ***OutAmpG*** and ***OutAmpH*** can be used as amplifiers, voltage references, and comparators. In addition to these features, Output Module ***OutAmpF*** (***Figure 14***) can also be set up as a Track & Hold amplifier. The output modules have second inputs, which are tied to 5 bit Digital-to-Analog converters (DACs).

In amplifier mode, the output modules have a fixed gain of two. Also, there is a 4µs propagation delay in normal power mode (see the clock module) through these modules, which are a mix of a switched-capacitor input stage followed by a continuous time output stage. In low power mode, there is a 32µs delay.

Amplifier programmable features include output signal reference level and filtering. The output signal reference level is the ability of these modules to shift their ground reference level. They can be set to function as "zero in, zero out" type amplifiers or "zero in, 2.5V out". The nominal 2.5V ground reference is the same reference used in the ***Offset*** Module and output ***DAC*** modules. The optional filter (on or off) is a single pole low-pass filter with a corner frequency of 15kHz.

In comparator mode, an optional 75mV level of hysteresis may be programmed. The amount of hysteresis is set to approximately 75 mV. Hysteresis is used to keep a comparator circuit from oscillating back and forth when the input signal is very close to the trip point.

Figure 14 Output Amplifier (OutAmpF)



Other programmable features include signal polarity, input signal source, turbo and power-down modes. Signal polarity can be inverting or non-inverting. For the input signal source, these modules may be connected to ***InpAmpA*** or ***InpAmpB***, ***CoreAmpC*** or ***CoreAmpD***, and ***SumAmpE***. Turbo mode increases slew rate and power consumption. Global and Selective power-down are also supported. When these modules are off, either not used or powered down, their outputs are high impedance.

To use the module as a voltage reference set the dedicated DAC to -1/2 the desired output voltage. The other input to the module may be left off by using "None" as the "connect input to" choice.

The Track & Hold feature of ***OutAmpF*** is useful for capturing a signal so that an Analog-to-Digital converter can convert it. With a Track & Hold circuit, the analog output can be in tracking or hold mode.

In tracking mode, the output of the circuit "tracks" the input. When placed in hold mode, the analog output is held (i.e., frozen) to the level that is present at the time the hold signal is received. Both the S1 and Sync pins are used to implement the Track and Hold feature.

The module is set to tracking mode whenever external pin S1 is set to a TTL level high, and hold mode when S1 is low. The output is held until S1 returns high. Because the IMP50E10 is clock driven, the output is not actually held the instant S1 is low, but rather when the proper clock phase is valid. A TTL level high voltage on the external Sync pin alerts the user when the signal is actually held.

The Sync pin is useful for feeding to a convert pin in the A/D. The maximum delay between the "requested" hold and the "actual" hold is 2µs for normal-power mode and 16µs for low-power mode.

DAC Modules F, G, & H

Key features:

- 32 voltage settings (= 4 bit + sign).
- One DAC for each Output Module, which is useful for setting thresholds, level-shifting and supplying reference voltages.

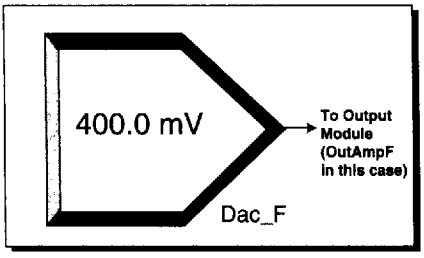
Description

There are three DACs (***Dac_F, Dac_G*** and ***Dac_H***., see ***Figure 15***) which are connected to the inverting input of all three output modules, ***OutAmpF, OutAmpG*** and ***OutAmpH***. The three DACs share a common resistor ladder network, allowing for excellent matching. Likewise, the DACs use the same internal chip reference.

The DAC output voltage is programmable in 133.3mV increments over a range of ±2.0V. The voltage range of the DAC can be extended by changing the Zero-output option of the output module to 2.5V. The DAC module can be used to: level-shift a signal when the output module is in amplifier mode, set the comparator trip point, or set a voltage reference.

Since the DACs share resources, if any one DAC is turned on, all three DACs are considered on for power consumption purposes. Low power mode does not affect current consumption of these modules.

Figure 15 DAC Modules (Dac_F)



Auxiliary Amplifier Module

Key features:

- Inputs/Output externally accessible for adding external feedback
- Optional enhanced drive capability ("Turbo" Mode)
- Low power consumption

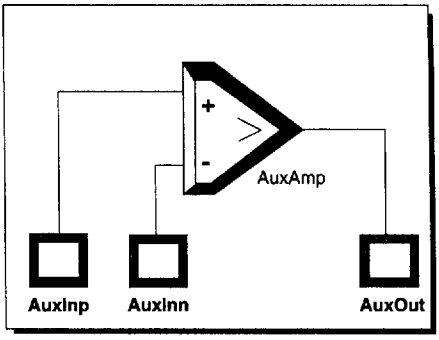
Description

One uncommitted low voltage, low power operational amplifier (***AuxAmp***) is available which can be used with externally supplied feedback components. This module is not connected to the internal signal paths of the chip, therefore, connections to or from this module are done externally (***Figure 16***).

Typical applications include non-linear feedback, voltage to current conversion, and precision gain adjustment using an external potentiometer.

Programmable features include Turbo and power-down modes. Power-down can be either global or selective. Turbo Power, which increases slew rate and power consumption, can be on or off.

Figure 16 Auxiliary Amplifier (AuxAmp)



Clock Module

Key features:

- Master mode (On-chip oscillator), can drive off-chip logic
- Generates output frequencies from 62kHz to 500kHz
- Slave mode (follows external clock)
- Accepts external clock frequencies from 500kHz to 4MHz
- Programmable input/output divider (N = 1,2,4,8)
- No external components

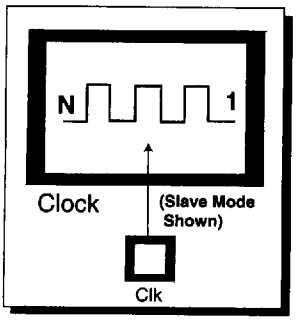
Description

The ***Clock*** module supplies control signals to the switched capacitor modules inside the chip. The master clock runs at approximately 500kHz. Two main analog sampling clocks run at half the frequency of the master clock, and thereby control the Nyquist rate of the chip.

The clock module has the capability to operate in either master or slave mode (***Figure 17***). A programmable divider resides between the clock and the external Clk pin. In master mode, clock frequencies of 500kHz, 250kHz, 125kHz, or 62.5kHz are supplied to external circuits. In slave mode, an externally generated clock signal can be supplied to the Clk pin.

The IMP50E10 can be put into a low power mode by changing the clock frequency and the internal bias circuits. This can be accomplished by switching from 500kHz (normal power mode) to 62.5kHz (low power mode).

Figure 17 Clock Module



Power Management Features

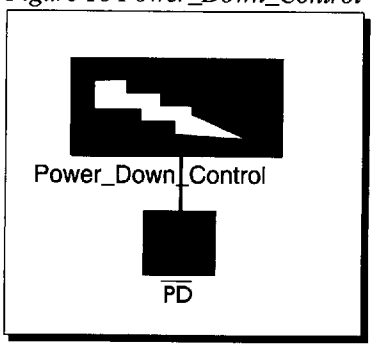
Power_Down_Control

The IMP50E10 is highly programmable for power control characteristics. The first option is whether or not to use a particular module for a given design. Unused modules draw no power. Once a module is used, it can be turned off through either the selective or global power down command.

Global, Selective Power Down: A global power down puts all modules inside the chip, even those with the selective power down option enabled, into a sleep mode. Typical power consumption is under 40µA for the entire chip. A selective power down is utilized to put only those modules specified as having selective power down enabled to sleep. The assignment of selective power down is done for each individual module with this feature. Selective power down allows some modules to remain fully functional, while other modules in the chip are put to sleep.

Either global or selective power down commands can be issued through the serial interface. In addition, a TTL zero voltage level on the external pin named $\overline{PD}$ (***Figure 18***) sends the chip into either the global or selective type of power down. Which type of power down depends on how the pin is programmed.

Figure 18 Power_Down_Control



Low Power Mode

In addition to power down, the chip can be operated in one of two power modes, normal and low. The power mode is controlled by the clock module on the chip. Many of the modules inside the chip are switched-capacitor, and their power consumption is related to the frequency at which they are clocked.

In low power mode, the nominal 500kHz master clock signal and some internal bias currents are divided by eight, which reduces power consumption and signal bandwidth by the same factor. Some modules inside the chip, such as the reference, and not affected by low power mode.

This feature is controlled individually for each output module, and is not part of the Power_Down_Control or Clock modules.

Turbo Power

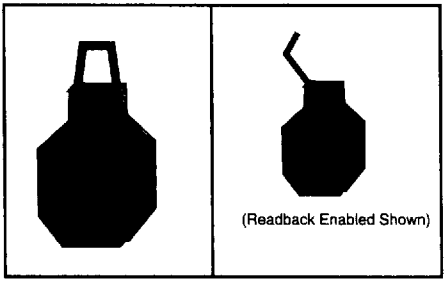
Output modules can be configured to have increased slew rate capability by enabling the Turbo Power option. When this feature is enabled, increased bias current is supplied to the module.

Security

Proprietary circuit configuration data is hidden from users and competitors through a security bit (***Figure 19***) which prevents reading back the stored configuration data.

The MagicProbe will not function if the security bit is enabled (i.e., locked).

Figure 19 Security ((A) Locked, (B) Unlocked)



A *B*

3

MagicProbe

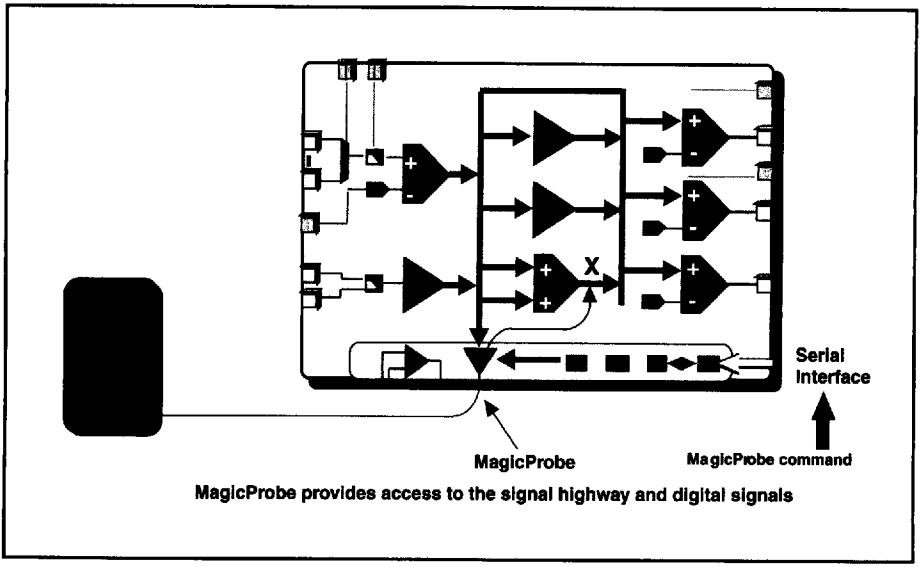
The IMP50E10 is very easy to use, with most design sessions taking less than half an hour. However, an on-chip debugging facility exists for situations when unexpected signal outputs occur. The MagicProbe™ feature allows the user to probe internal digital and analog signals inside the chip without disturbing the original signal. This module features high input and low output impedances. (See ***Figure 20***.)

In analog mode, it has a fixed gain of two, signal inversion capability, zero reference level control, and an optional single pole 15kHz low pass filter. These capabilities are the same as described in the Output module description.

The digital mode of the MagicProbe allows viewing of the two main analog sampling clocks, which run at half the frequency of the master clock.

The MagicProbe configuration register is not mapped into the EEPROM memory, consequently when power is first applied to the chip this module is not connected and powered off.

Figure 20 MagicProbe Concept



IMP50E10
Electrical Characteristics

Absolute Maximum Ratings[1]

Parameter	Range
V_{DD} to V_{SS}	0V to 7V
Voltage at Any Pin[2]	V_{SS} -0.3V to V_{DD} +0.3V
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10sec)	300°C
ESD Rating (max)[3]	1.5kV
Input Current at Any Pin	100mA

[1] Stresses beyond those specified in the "Absolute Maximum Ratings" may cause damage to the device. The ratings are for stress only, and the functional operation of the device at these levels is not implied.
[2] Transients to 0.6V above or below the power supply rails are permissable.
[3] Human body model, 100pF discharged through a 1.5kΩ resistor

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Recommended Operating Conditions

Part No.	Operating Temperature Range	Operating Voltage Range
IMP50E10-C	0°C to 70°C	4.5V to 5.5V

General Electrical Characteristics

(Unless otherwise specified, 4.5V<V_{DD}<5.5, T_A = 0-70°C, 500kHz Master Clock Rate)

Parameter	Condition	Min	Typ	Max	Units
Power Supply Voltage		4.5	5	5.5	V
Quiescent Supply Current	Sleep Mode		55	70	µA
	Low Power, all modules active		3.8	5.1	mA
	Normal Power, all modules active		7.5	10	mA
	Normal power, no modules active [1]		3.4	4.5	mA
Programming Time (Full configuration)	To EEPROM, f_{clock} = 800Hz	285			ms
	To Configuration Register, f_{clock} = 1.5MHz	150			µs
EEPROM Download Time	To Configuration Register			1	ms
Wake-up Time[2]	Time from receiving SLI high or $\overline{PD}$ voltage input			5	µs
Auto-Zero Time	Normal power			20.5	ms
	Low power			163	ms
Channel Scan Rate	Channels selected with external Grp select pins, modules A & F in series[3], no filters, normal power	8			µs/ch
	Channels selected through serial interface, modules A & F in series[3], no filters, normal power	26			µs/ch
EEPROM Endurance	T_A = 25°C	10,000	100,000		cycles
EEPROM Data Retention	T_A = 70°C	10			years
System Clock	Master mode, T_A = 25°C	450	500	550	kHz
Internal Sampling Rate	Normal power	225	250	275	kHz
	Low power	28.1	31.3	34.4	kHz
System Bandwidth	Input filter ON, normal or low power	12.5	15	18.5	kHz
	Input and output filters OFF, normal power (limited by Nyquist rate)	112	125	138	kHz
	Input and output filters ON, normal or low power	8.8	10.6	13.1	kHz
	Input and output filters OFF, low power (limited by Nyquist rate)	14	15.5	17	kHz

[1] Active circuitry includes voltage reference, bias and clock circuitry

[2] Time does not include propagation delay through switch-capacitor modules or settling times for the LPF and output filters

[3] A = InpAmpA, C = CoreAmpC, F = OutAmpF

General Electrical Characteristics (continued)

(Unless otherwise specified, 4.5V<V_{DD}<5.5, T_A = 0-70°C, 500kHz Master Clock Rate)

Parameter	Condition	Min	Typ	Max	Units
Input Signal Range		V_{SS}-0.2		V_{DD}+0.2	V
Input Common-Mode Voltage Range		V_{SS}		V_{DD}	V
Output Signal Range	R_L = 1kΩ to V_{SS}	V_{SS}+0.05		V_{DD}-0.5	V
Minimum Gain	All modules in series		1		V/V
Maximum Gain	All modules in series		20,000		V/V
Absolute Gain Error	Modules A, C, & F in series[3], gains = 6,4,2,T_A = 25°C	1.2		2.1	%
Gain Drift	Modules A, C, & F in series[3], gains = 6,4,2		-60		ppm/°C
Input Offset Voltage	Modules A, C, & F in series[3], gains = 6,4,2,V_{CM} = 2.5V	-27.5		17.5	mV
	With Auto-Zero		100	1000	µV
Input Offset Voltage Drift	Modules A, C, & F in series[3], gains = 6,4,2		-15		µV/°C
Input Noise Voltage Spectral Density	Modules A, C, & F in series[3], gains = 10, 10, 2, f = 1kHz		0.5		µV/√Hz
Total Harmonic Distortion	Sum of 2nd, 3rd harmonic, modules A, C, & F in series[3], gains = 10, 1, 2, V_{out} = $2V_{PP}$, f = 5kHz		-65		dB

[3] A=InpAmpA, C=CoreAmpC, F=OutAmpF

Digital DC Characteristics

(Unless otherwise specified, 4.5V < V_{DD} < 5.5V, T_A = 0-70°C)

Parameter	Condition	Min	Typ	Max	Units
Input High Voltage		2.0			V
Input Low Voltage				0.8	V
Input Capacitance				10	pF
Output Low Voltage	I_{OL} = 3.2mA			0.4	V
Output High Voltage	I_{OH} = -2mA	2.4			V

3

Analog Characteristics

(Unless otherwise specified, 4.5V<V_{DD}<5.5, T_A = 0-70°C, 500kHz Master Clock Rate)

Input Multiplexer Module (InpMux)

Parameter	Condition	Min	Typ	Max	Units
Number of Channels	Differential mode			8	
	Single-ended mode			16	
Quiescent Supply Current				0.1	µA
Input Voltage Range		V_{SS}-0.2		V_{DD}+0.2	V
Channel Offset Matching (Input Referred)	Between any two grounded input channels		100		µV

Low Pass Filter Module (LPF)

Parameter	Condition	Min	Typ	Max	Units
Quiescent Supply Current				0.1	µA
Settling Time	5 time constants (99.3%) Low-pass filter resistor ≈ 144kΩ Multiplexer ON resistance ≈ 0.1kΩ On-chip low-pass filter ON		52		µs
Cutoff Frequency	$C_{internal}$ = ON	12.5	15	18.5	kHz
	$C_{internal}$ = OFF		845		kHz
Low Pass Resistor and Multiplexer ON Switch Resistance			144		kΩ

Offset Module (Offset)

Parameter	Condition	Min	Typ	Max	Units
Resolution	Including sign bit	8		8	Bits
Quiescent Supply Current	Normal power		380	500	µA
	Low power		50	65	µA
Integral Non-Linearity [1,4]	All ranges			±0.5	LSB
Differential Non-Linearity [1,4]	All ranges			±0.5	LSB
Full-scale Range Error [2,4]	20mV step	-1.5		2	%
	1mV step	-2.5		2.5	%
	100µV step	-5		5	%
	25µV step	-6		18	%
DAC Offset Error [1]	All ranges			±1	mV
Analog Settling Time	Normal power			8	µs
PSRR	At DC		50		dB
Voltage Reference					
Absolute Error [2]	All ranges	-5		5	%
Temperature Drift [3]			-25		ppm/°C
PSRR[3]	At DC		50		dB

[1] Ranges are ±3.175mV, ±12.7mV, ±127mV and ±2.54V
[2] The total Offset Module scale error is arrived at by adding the Offset Module Full-Scale Range Error to the Voltage Reference Absolute Error.
[3] Temperature Drift and PSRR are dominated by the voltage reference.
[4] $T_A = 25^{\circ}C$

3

Input Modules [1] (InpAmpA, InpAmpB)

Parameter	Condition	Min	Typ	Max	Units
Quiescent Supply Current	Normal power		380	500	µA
	Low power		50	65	µA
Common Mode Voltage Input Range		V_{SS}		V_{DD}	V
Input Impedance	Differential mode, normal power, gain = 4, V_{CM} = 2.5V		20		MΩ
	Differential mode, low power, V_{CM} = 2.5V		160		MΩ
	Common mode, normal power, V_{CM} = 2.5V		2		MΩ
	Common mode, low power, V_{CM} = 2.5V		16		MΩ
Input Referred Offset Voltage	All gains, Auto-Zero set to 100µV range, external mode			100	µV
	Gain = 1 to 10, V_{CM}=2.5V[2]	-12.5		12.5	mV
	Gain = 0.5, V_{CM} = 2.5V[2]	-20		20	mV
Absolute Gain Error	Gain = 0.5, V_{CM} = 2.5V	-1	0	4	%
	Gain = 1,2,3, V_{CM} = 2.5V	-0.7	0.8	2.3	%
	Gain = 4,6,8, V_{CM} = 2.5V	-1	0	1	%
	Gain = 10, V_{CM} = 2.5V	-2.1	-1.1	0.1	%
Gain Matching Error	Between two adjacent gains		0.5		%
PSRR	At DC		50		dB
CMRR	At DC		55		dB
Total Harmonic Distortion	Sum of 2nd, 3rd harmonic, f = 5kHz, V_{out} = 2.5V_{P-P}, R_L = 100kΩ, gain = 10		-68		dB
Linearity	A-F[4] (8-2), R_L=100kΩ, 0.5V ≤V_{OUT}≤4.5V		12		Bits
Input Noise Voltage [3] Spectral Density	Normal power, gain = 200, f = 1kHz, A-C-F[4] (10-10-2)		0.5		µV/√Hz
Input Noise Voltage	Normal power, gain = 200, 0< f<15kHz, A-C-F[4] (10-10-2)		61		$µV_{RMS}$
Propagation Delay	Normal power		4		µs

[1] Input modules cover specifications for any input module (A or B) when connected to any output module (F, G or H). Gains are shown for Input Modules only.
[2] T_A = 25 °C
[3] Noise is dominated by input modules
[4] A = InpAmpA, B=InpAmpB, C = CoreAmpC, F = OutAmpF, G=OutAmpG, H=OutAmpH

Core Modules[1] (CoreAmpC, CoreAmpD, SumAmpE)

Parameter	Condition	Min	Typ	Max	Units
Quiescent Supply Current	Normal power		250	330	µA
	Low power		32	42	µA
Input Referred Offset Voltage[2]	All gains, V_{CM}=2.5V, T_A=25°C	-15		5	mV
Absolute Gain Error	Gain = 1 to 3	0.1	0.8	1.7	%
	Gain = 4 to 8	-0.2	0.5	1.1	%
	Gain = 10	-0.6	0	0.6	%
Gain matching error	Between two adjacent gains		0.2		%
PSRR	At DC		65		dB
Total Harmonic Distortion	Sum of 2nd, 3rd harmonic, f = 1kHz, V_{out} = 2Vpp, gain = 4		-75		dB
Propagation Delay	Normal power		4		µs

[1] Parameters measured by inserting core modules in series with an input/output pair. Parameters are derived by subtracting result of an input/core/output module connection sequence with an input/output module connection.

[2] Referred to the input of the core module

3

Output Modules (OutAmpF, OutAmpG, OutAmpH)

Parameter	Condition	Min	Typ	Max	Units
Quiescent Supply Current	Normal power		590	770	µA
	Turbo power		1.1	1.45	mA
Output Impedance	Normal power at DC		3		Ω
	Turbo power at DC		1		Ω
Short Circuit Output Current			40		mA
Slew Rate	Normal power, C_L= 50pF		1.5		V/µs
	Turbo power, C_L= 50pF		3		V/µs
Output Voltage Range	I_{OUT} = ±50µA	V_{SS}+0.05		V_{DD}-0.05	V
	I_{OUT} = ±5mA	V_{SS}+0.5		V_{DD}-0.5	V
Zero Output Reference Level	Analog Magic Zero Output set to 2.5V	2.35	2.5	2.65	V
Propagation Delay	Normal power		4		µs
Amplifier Mode					
Output Filter Cut-off Frequency	Filter = ON	12.5	15	18.5	kHz
	Filter = OFF		363		kHz
Droop Rate	Track&Hold mode, T_A=25°C		10		nV/ms
	Track&Hold mode, T_A=70°C			450	nV/ms
Acquisition Time	To 0.1%, Track&Hold mode, after sync pulse			4	µs
Sync Delay				2	µs
Comparator Mode					
Hysteresis	Hysteresis = ON		75		mV
Delay	C_L = 50pF, normal power, 10mV overdrive			5	µs
Resolution		1			mV

DAC Modules (DAC_F, DAC_G, DAC_H)

Parameter	Condition	Min	Typ	Max	Units
Quiescent Supply Current	Total for three DACs		300	430	µA
Resolution (4-bits)			133		mV
Output Voltage			±2.0		V
Voltage Gain Errors[1]	T_A = 25°C	-7		7	%
Voltage Offset Error	T_A = 25°C	-10		10	mV
PSRR	At DC, V_{DAC} = 1.067V		55		dB

[1] Error includes contributions from internal reference and output modules OutAmpF, OutAmpG or OutAmpH.

MagicProbe (T_A = 25°C)

Parameter	Condition	Min	Typ	Max	Units
Quiescent Supply Current			590	770	µA
Gain			2.0		V/V
Output Voltage Range	Iout = ±50µA	V_{SS} + 0.05		V_{DD} - 0.05	V
	Iout = ±5mA	V_{SS} + 0.5		V_{DD} - 0.5	V

Auxiliary Amplifier (AuxAmp)

Parameter	Condition	Min	Typ	Max	Units
Quiescent Supply Current	Normal power		350	460	µA
	Turbo power		700	920	µA
Input Referred Offset Voltage	V_{CM} = 2.5V	-8		8	mV
Short Circuit Output Current			40		mA
Input Noise Voltage Spectral Density	f = 10kHz		30		nV/√Hz
Input Offset Drift			2.5		µV/ °C
Output Impedance	Normal power at DC		3		Ω
	Turbo power at DC		1		Ω
Open Loop Gain	Turbo OFF	82	88		dB
Unity-Gain Bandwidth	Turbo ON, C_L = 100pF		2.0		MHz
	Turbo OFF, C_L = 100pF		1.4		MHz
Phase Margin	C_L=100pF, Normal or Turbo power		60		Degrees
CMRR	At DC		60		dB
PSRR	At DC		74		dB
Common-Mode Input Voltage Range	V_{DD} = 5V	0		3	V
Output Voltage Range	I_{out} = ±50µA	V_{SS}+0.05		V_{DD}-0.05	V
	I_{out} = ±5mA	V_{SS}+0.5		V_{DD}-0.5	V
Slew Rate	Normal power, C_L = 50pF		1.5		V/µs
	Turbo power, C_L = 50pF		3		V/µs
Input Bias Current		-15		15	nA

Clock

Parameter	Condition	Min	Typ	Max	Units
Output Frequency [1]	Normal power, divider = 1	450	500	550	kHz
	Normal power, divider = 8	56	62	69	kHz
Duty Cycle [1]	Master mode	47.5	50	52.5	%
Power Supply Sensitivity			1		kHz/V
Frequency Drift			350		Hz/°C
Rise Time	C_L = 50pF		25		ns
Fall Time	C_L = 50pF		10		ns

[1] T_A = 25 °C

Typical Characteristic Curves ($T_A = 25°C$, $V_{CM} = 2.5V$, $V_{DD} = 5V$)

Figure 21 Temperature Drift of Gain - Modules Used: (A or B) to (F or G or H)

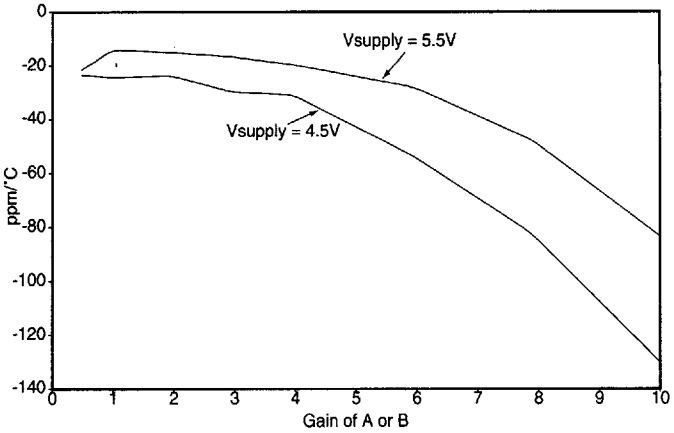


Figure 22 Temperature Drift of Gain - Modules Used: C or D

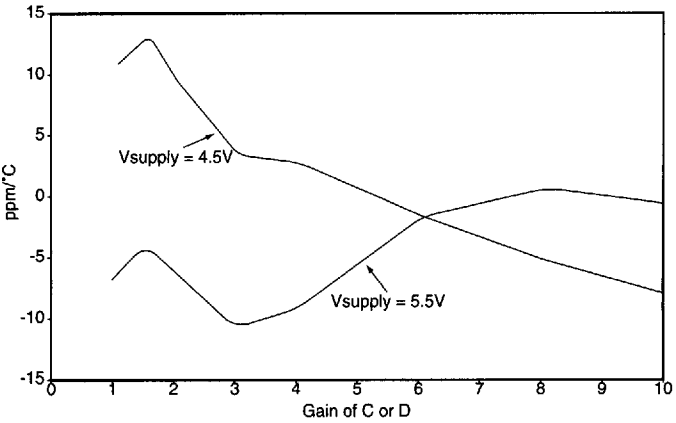
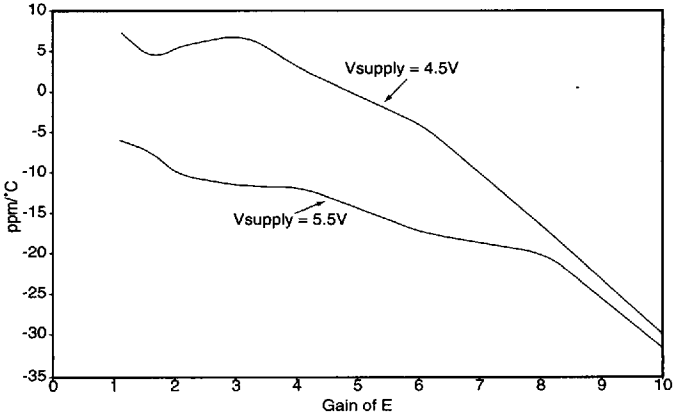


Figure 23 Temperature Drift of Gain - Module Used: E



Typical Characteristic Curves $(T_A = 25°C, V_{CM} = 2.5V, V_{DD} = 5V)$

Figure 24 Temperature Drift of Offset - Modules Used: (A or B) to (F or G or H)

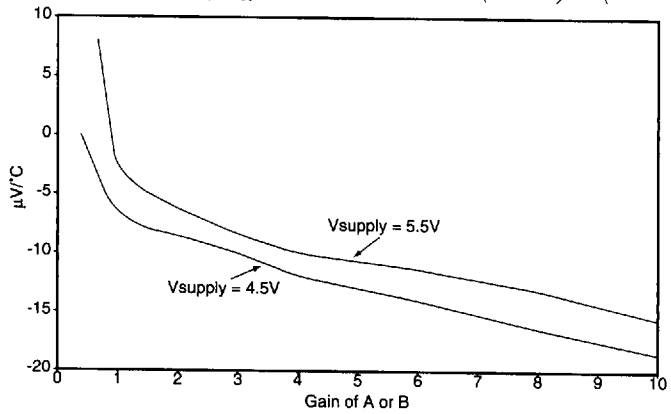


Figure 25 Temperature Drift of Offset - Modules Used:C or D or E

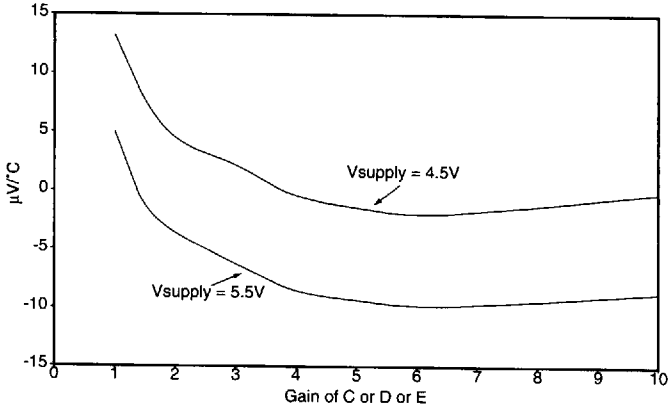
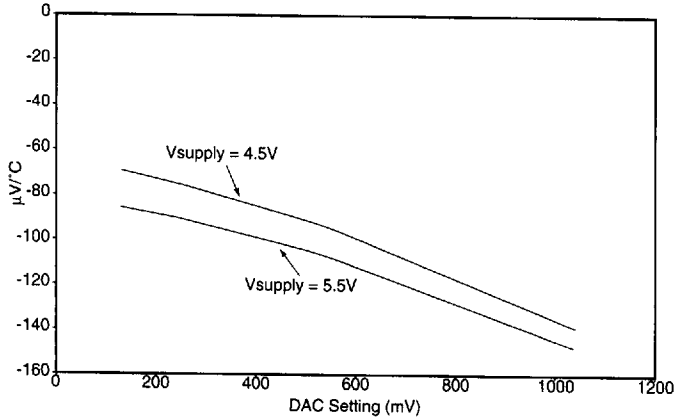


Figure 26 Temperature Drift of Output DAC & Amplifier- Modules Used: F or G or H



Typical Characteristic Curves $(T_A = 25°C, V_{CM} = 2.5V, V_{DD} = 5V)$

Figure 27 IMP50E10 Frequency Response[1], Filters[2] OFF

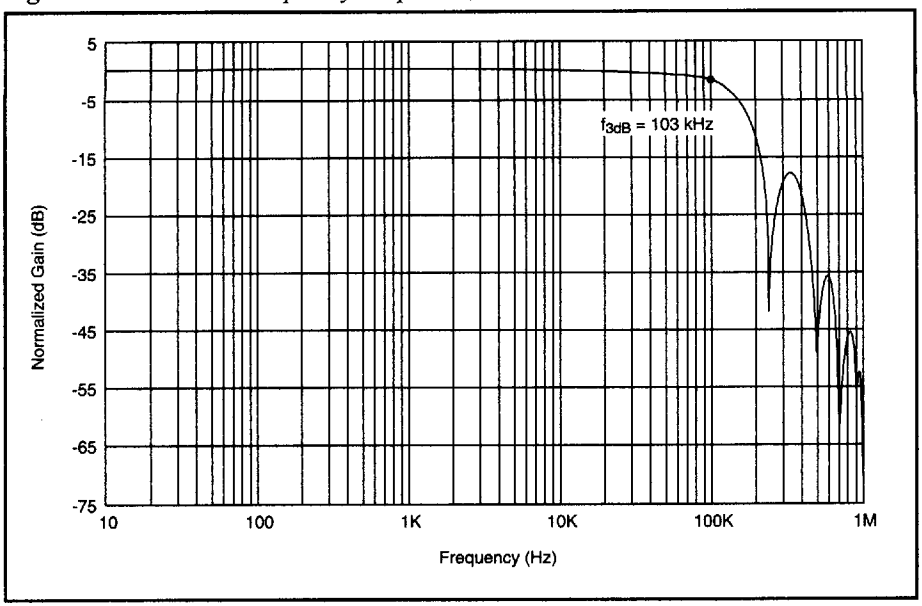
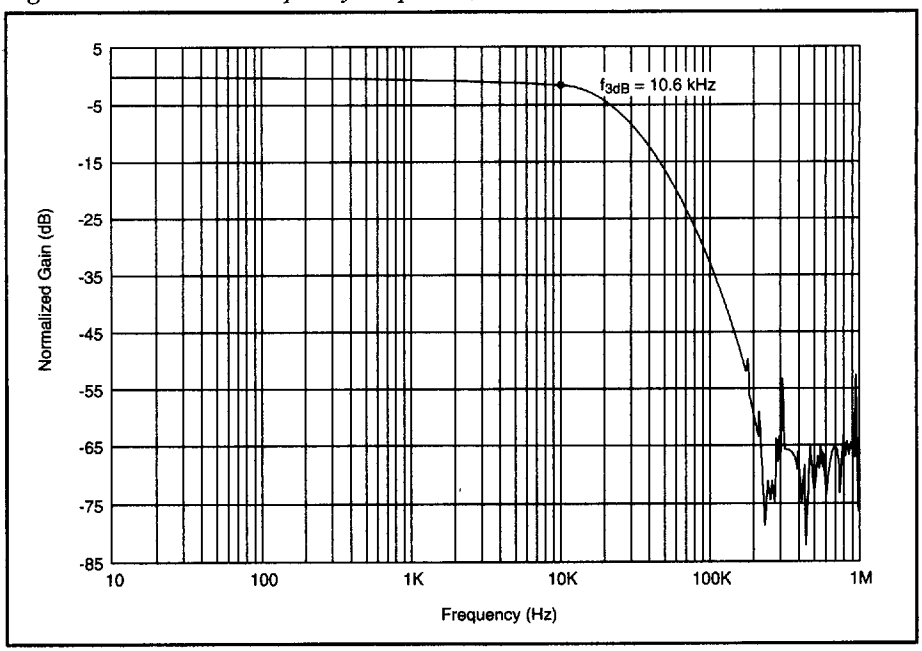


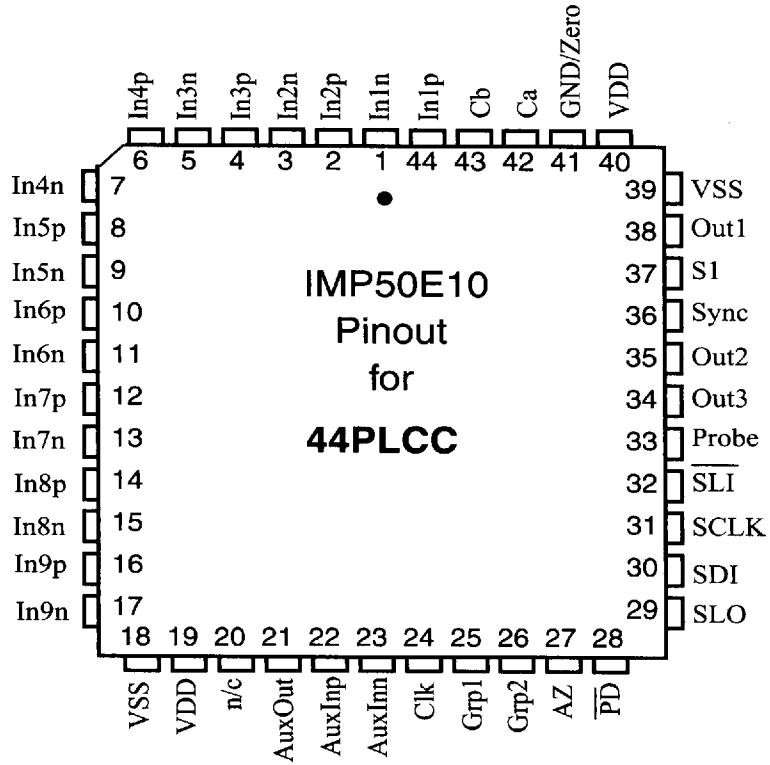
Figure 28 IMP50E10 Frequency Response[1], Filters[2] ON



[1] Gain vs. frequency exhibits the same 3dB points for any gain (1, ..., 20,000) because of the switched-capacitor module implementation inside the IMP50E10. Gain roll-off is due to the $\frac{\sin x}{x}$ term in the sampling theorem.

[2] Filters refers to the input and output filters.

Pin Assignments



Ordering Information	Package	Temperature Range
IMP50E10C-018AC	44-pin PLCC	0°C to 70°C

IMP50E10 Pin Descriptions (Pin Type: (P)ower, (D)igital, (A)nalog)

PIN #	Name	Type	Description
44	In1p	A	Analog Inputs to Multiplexer and InpAmpA.
1	In1n	A	Configurable as 16 single-ended inputs or 8 differential inputs.
2	In2p	A	
3	In2n	A	
4	In3p	A	Pin name definition: Pins are named as differential channels,
5	In3n	A	the channel number and polarity of the pin [(p)ositive or
6	In4p	A	(n)egative] are part of the pin name.
7	In4n	A	In single-ended mode, In1n is channel 1, In2p
8	In5p	A	is channel 2, etc.
9	In5n	A	
10	In6p	A	
11	In6n	A	
12	In7p	A	
13	In7n	A	
14	In8p	A	
15	In8n	A	
16	In9p	A	Analog Inputs to InpAmpB. Configurable as 1 differential-pair
17	In9n	A	input or one single-ended input.
18, 39	VSS	P	Negative Power Supply (0V)
19, 40	VDD	P	Positive Power Supply (+5V)
21	AuxOut	A	Output of Auxiliary Amplifier
22	AuxInp	A	Non-inverting input of Auxiliary Amplifier
23	AuxInn	A	Inverting input of Auxiliary Amplifier
24	Clk	D	Clock input or output
25	Grp1	D	Group Selection Pins: Pin combination selects 1 of 4 Groupings of
26	Grp2	D	gain, filter setting and offset to be applied to a selected input channel.
27	AZ	D	Auto-Zero trigger. Must be low if unused.
28	$\overline{PD}$	D	Active-low Power-Down pin. Can be programmed to act as a selective or global power-down pin.
29	SLO	D	Serial Load Output. Provides input to next cascaded EPAC's SLI pin.
30	SDI	D	Serial Data Input. "0"=low. Data sampled on SCLK low-to-high transition.
31	SCLK	D	Serial Interface Clock.
32	$\overline{SLI}$	D	Serial Load Input. Chip-Select for Serial Interface. Data is shifted into registers while $\overline{SLI}$ is low and is latched when $\overline{SLI}$ goes high.
33	Probe	A/D	PROBE output. Internal analog or digital signals can be routed to this test pin. High-Impedance mode if unused.
34	Out3	A	Output of OutAmpH. High-Impedance mode is unused.
35	Out2	A	Output of OutAmpG. High-Impedance mode if unused.
36	Sync	D	Output flag indicates that OutAmpF is holding a signal.
37	S1	D	TTL input to OutAmpF to control Track (high) and Hold (low).
38	Out1	A	Output of OutAmpF. High-Impedance mode if unused.
41	GND/Zero	A	GND/Zero pin. In single-ended mode, this pin is used as signal ground. In differential mode, always tie to Vss.
42	Ca	A	Connections for external capacitor to change LPF corner
43	Cb	A	frequency. High-Impedance mode when unused.

44-pin Plastic LCC Package

Package Description

44-pin Plastic Leaded Chip Carrier
JEDEC Part Number MS-018AC

Package Outline

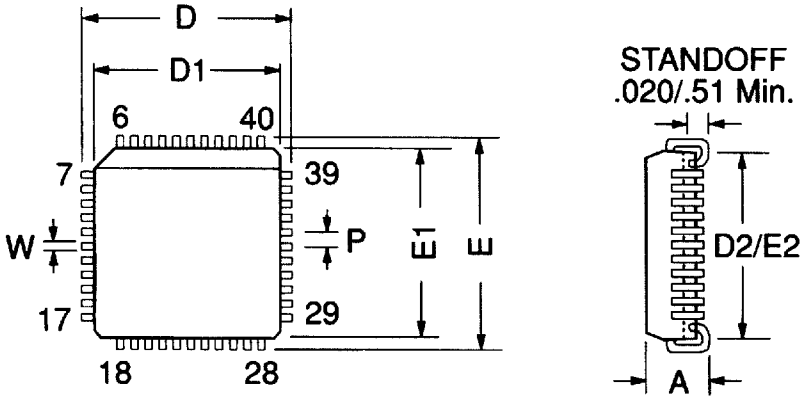


Table 1 Package Outline - Dimensions in Inches

Description	Symbol	Min.	Max.
Package Height	A	.165	.180
Standoff	A1	.090	.120
Max Width	D	.685	.695
Body Width	D1	.650	.656
Footprint Width	D2	.590	.630
Max Length	E	.685	.695
Body Length	E1	.650	.656
Footprint Length	E2	.590	.630

Table 2 Package Outline - Dimensions in Metric

Description	Symbol	Min.	Max.
Package Height	A	4.20	4.57
Standoff	A1	2.29	3.04
Max Width	D	17.40	17.65
Body Width	D1	16.510	16.662
Footprint Width	D2	14.99	16.00
Max Length	E	17.40	17.65
Body Length	E1	16.510	16.662
Footprint Length	E2	14.99	16.00

Recommended Connection Diagram