2.5 V 184-pin Unbuffered DDR-I SDRAM Modules

256MB & 512MB Modules

Preliminary Datasheet Rev. 0.9

- 184-pin Unbuffered 8-Byte Dual-In-Line DDR-I SDRAM non-parity and ECC-Modules for PC and Server main memory applications
- One bank 32M × 64, 32M x 72 and two bank 64M x 64, 64M × 72 organization
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR-I SDRAM) Single + 2.5 V (± 0.2 V) power supply
- Built with 256Mbit DDR-I SDRAMs in 66-Lead TSOPII package
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- Serial Presence Detect with E^2PROM
- Jedec standard MO-206a form factor: 133.35 mm × 31.75 mm × 4.00 mm
- Jedec standard reference layout
- Gold plated contacts

- Performance:

		-7	-7.5	-8	Unit
	Component Speed Grade	PC266A	PC266B	PC200	
	Module Speed Grade	PC2100	PC2100	PC1600	
f_{CK}	Clock Frequency (max.) @ CL = 2.5	143	133	125	MHz
f_{CK}	Clock Frequency (max.) @ CL = 2	133	100	100	MHz

The HYS64/72D000GU are industry standard 184-pin 8-byte Dual in-line Memory Modules (DIMMs) organized as 32M × 64 and 64M × 64 for non-parity and 32M x 72 and 64M x 72 for ECC main memory applications. The memory array is designed with Double Data Rate Synchronous DRAMs (2.5V DDR-I). A variety of decoupling capacitors are mounted on the PC board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

Ordering Information

Type	Compliance Code	Description	SDRAM Technology
PC266A:			
HYS64D32000GU-7	PC266A-20330-B1	one bank 256 MB Reg. DIMM	256 MBit
HYS72D32000GU-7	PC266A-20330-B1	one bank 256 MB Reg. ECC-DIMM	256 Mbit
HYS64D64020GU-7	PC266A-20330-A1	two banks 512 MB Reg. DIMM	256 MBit
HYS72D64020GU-7	PC266A-20330-A1	two banks 512 MB Reg. ECC-DIMM	256 MBit
PC266B:			
HYS64D32000GU-7.5	PC266B-25330-B1	one bank 256 MB Reg. DIMM	256 MBit
HYS72D32000GU-7.5	PC266B-25330-B1	one bank 256 MB Reg. ECC-DIMM	256 Mbit
HYS64D64020GU-7.5	PC266B-25330-A1	two banks 512 MB Reg. DIMM	256 MBit
HYS72D64020GU-7.5	PC266B-25330-A1	two banks 512 MB Reg. ECC-DIMM	256 MBit
PC200R:			
HYS64D32000GU-8	PC200-20220-B1	one bank 256 MB Reg. DIMM	256 MBit
HYS72D32000GU-8	PC200-20220-B1	one bank 256 MB Reg. ECC-DIMM	256 Mbit
HYS64D64020GU-8	PC200-20220-A1	two banks 512 MB Reg. DIMM	256 MBit
HYS72D64020GU-8	PC200-20220-A1	two banks 512 MB Reg. ECC-DIMM	256 MBit

Note: All part numbers end with a place code (not shown), designating the silicon-die revision. Reference information available on request.
Example: HYS 72D32000GU-8-A, indicating Rev.A die are used for SDRAM components.

Pin Definitions and Functions

A0 - A12	Address Inputs	$\overline{S0}$, $\overline{S1}$	Chip Selects
BA0, BA1	Bank Selects	V_{DD}	Power (+ 2.5 V)
DQ0 - DQ63	Data Input/Output	V_{SS}	Ground
CB0 - CB7	Check Bits (x72 organization only)	V_{DDQ}	I/O Driver power supply
$\overline{RAS}$	Row Address Strobe	V_{DDID}	VDD Indentification flag
$\overline{CAS}$	Column Address Strobe	V_{REF}	I/O reference supply
$\overline{WE}$	Read/Write Input	V_{DDSPD}	Serial EEPROM power supply
CKE0 - CKE1	Clock Enable	SCL	Serial bus clock
DQS0 - DQS8	SDRAM low data strobes	SDA	Serial bus data line
CLK0 - CLK2,	SDRAM clock (positive lines)	SA0 - SA2	slave address select
$\overline{CLK0}$ - $\overline{CLK2}$	SDRAM clock (negative lines)	NC	no connect
DM0 - DM8 DQS9 - DQS17	SDRAM low data mask/ high data strobes		

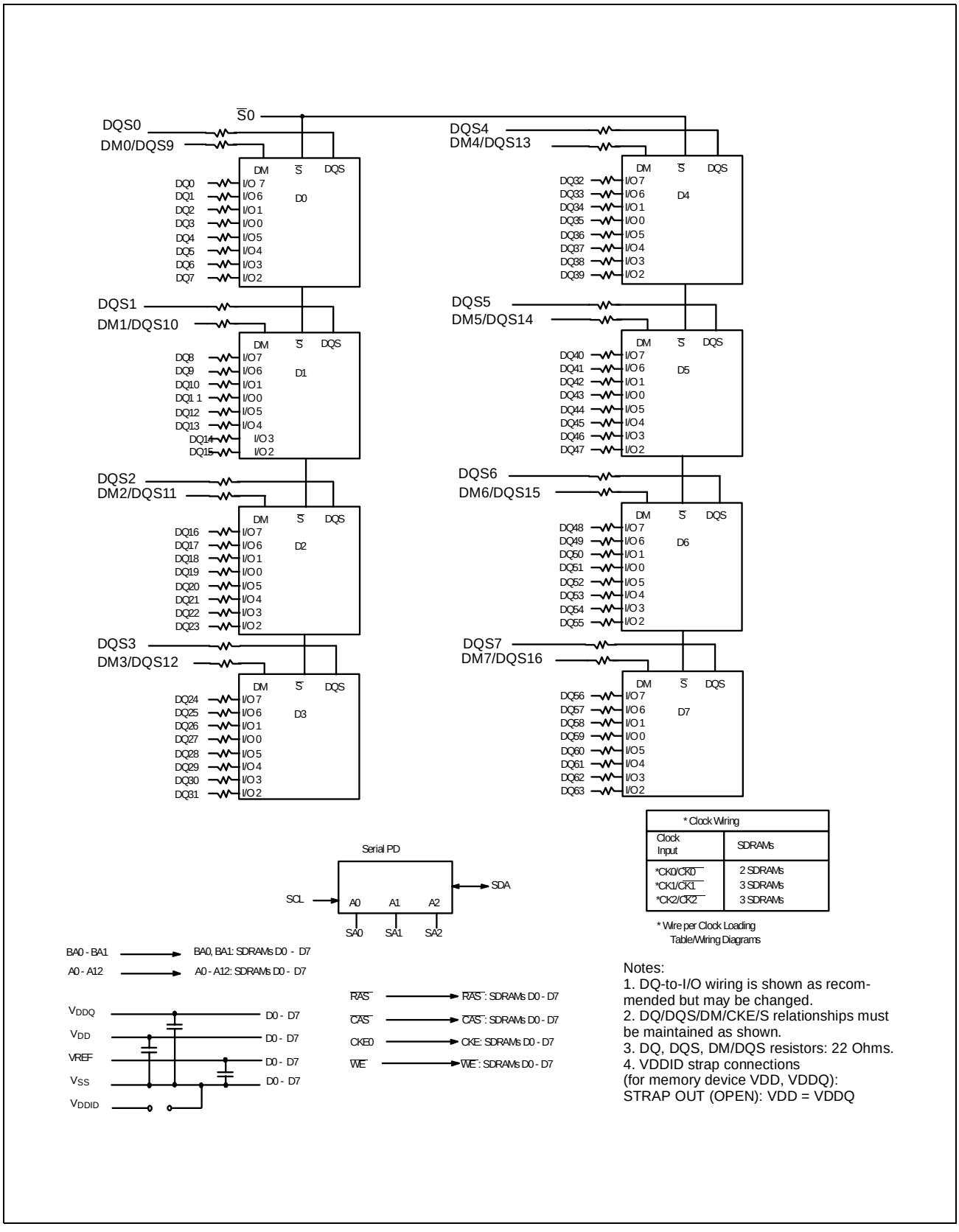
Address Format

Density	Organization	Memory Banks	SDRAMs	# of SDRAMs	# of row/bank/ columns bits	Refresh	Period	Interval
256 MB	32M x 64	1	32M x 8	8	13/2/10	8k	64 ms	7.8 µs
256 MB	32M x 72	1	32M x 8	9	13/2/10	8k	64 ms	7.8 µs
512 MB	64M × 64	2	32M x 8	16	13/2/10	8k	64 ms	7.8 µs
512 MB	64M × 72	2	32M x 8	18	13/2/10	8k	64 ms	7.8 µs

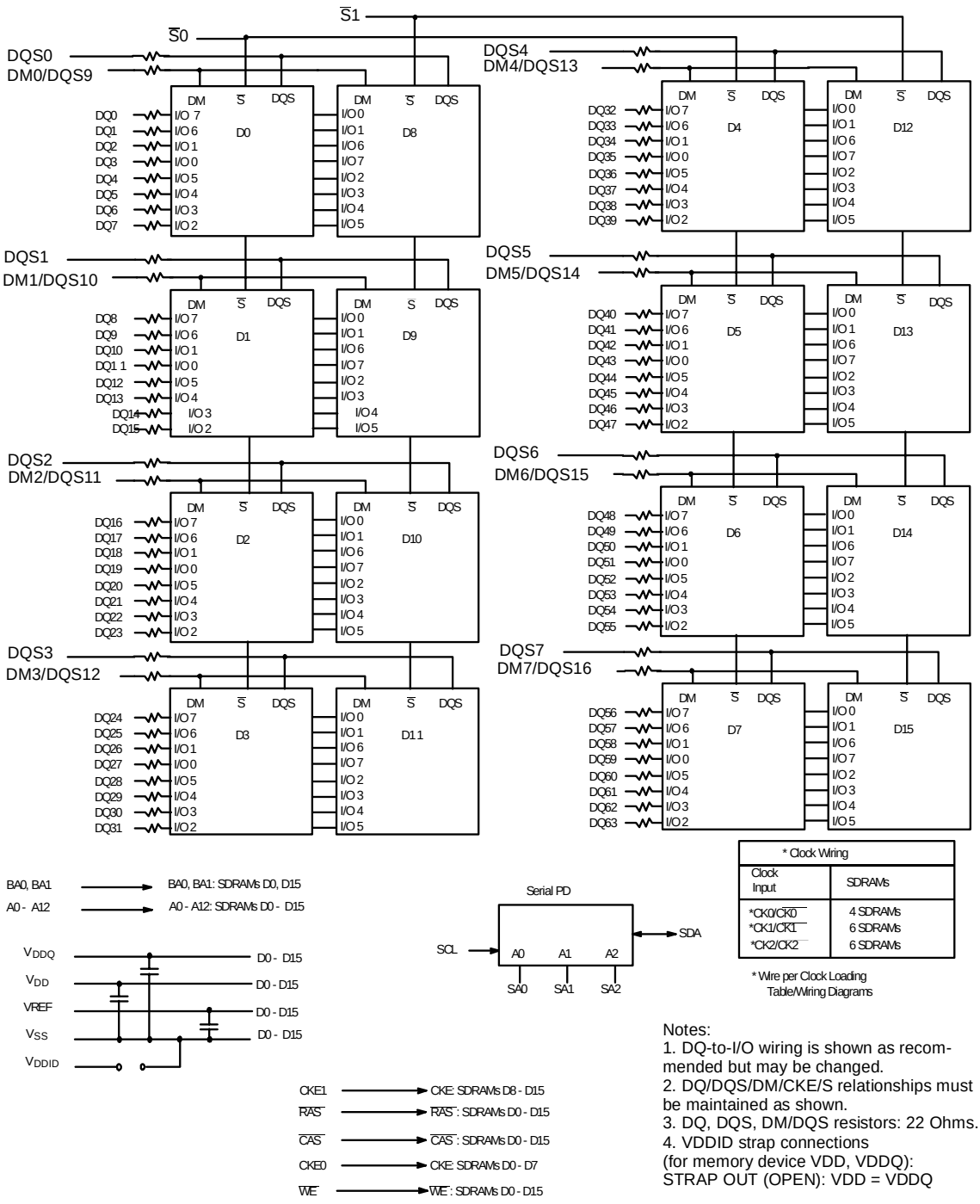
Pin Configuration

Frontside		Frontside		Backside		Backside	
PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
1	VREF	48	A0	93	VSS	140	NC / DM8/DQS17
2	DQ0	49	NC / CB2	94	DQ4	141	A10
3	VSS	50	VSS	95	DQ5	142	NC / CB6
4	DQ1	51	NC / CB3	96	VDDQ	143	VDDQ
5	DQS0	52	BA1	97	DM0/DQS9	144	NC / CB7
6	DQ2	KEY		98	DQ6	KEY	
7	VDD	53	DQ32	99	DQ7	145	VSS
8	DQ3	54	VDDQ	100	VSS	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	NC	56	DQS4	102	NC	148	VDD
11	VSS	57	DQ34	103	A13	149	DM4/DQS13
12	DQ8	58	VSS	104	VDDQ	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	VSS
15	VDDQ	61	DQ40	107	DM1/DQS10	153	DQ44
16	CLK1	62	VDDQ	108	VDD	154	$\overline{RAS}$
17	$\overline{CLK1}$	63	$\overline{WE}$	109	DQ14	155	DQ45
18	VSS	64	DQ41	110	DQ15	156	VDDQ
19	DQ10	65	$\overline{CAS}$	111	CKE1	157	$\overline{S0}$
20	DQ11	66	VSS	112	VDDQ	158	$\overline{S1}$
21	CKE0	67	DQS5	113	NC (BA2)	159	DM5/DQS14
22	VDDQ	68	DQ42	114	DQ20	160	VSS
23	DQ16	69	DQ43	115	A12	161	DQ46
24	DQ17	70	VDD	116	VSS	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC
26	VSS	72	DQ48	118	A11	164	VDDQ
27	A9	73	DQ49	119	DM2/DQS11	165	DQ52
28	DQ18	74	VSS	120	VDD	166	DQ53
29	A7	75	CLK2	121	DQ22	167	NC
30	VDDQ	76	$\overline{CLK2}$	122	A8	168	VDD
31	DQ19	77	VDDQ	123	DQ23	169	DM6/DQS15
32	A5	78	DQS6	124	VSS	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	VSS	80	DQ51	126	DQ28	172	VDDQ
35	DQ25	81	VSS	127	DQ29	173	NC
36	DQS3	82	VDDID	128	VDDQ	174	DQ60
37	A4	83	DQ56	129	DM3/DQS12	175	DQ61
38	VDD	84	DQ57	130	A3	176	VSS
39	DQ26	85	VDD	131	DQ30	177	DM7/DQS16
40	DQ27	86	DQS7	132	VSS	178	DQ62
41	A2	87	DQS8	133	DQ31	179	DQ63
42	VSS	88	DQ59	134	NC / CB4	180	VDDQ
43	A1	89	VSS	135	NC / CB5	181	SA0
44	NC / CB0	90	NC	136	VDDQ	182	SA1
45	NC / CB1	91	SDA	137	CK0	183	SA2
46	VDD	92	SCL	138	$\overline{CK0}$	184	VDDSPD
47	NC / DQS8			139	VSS		

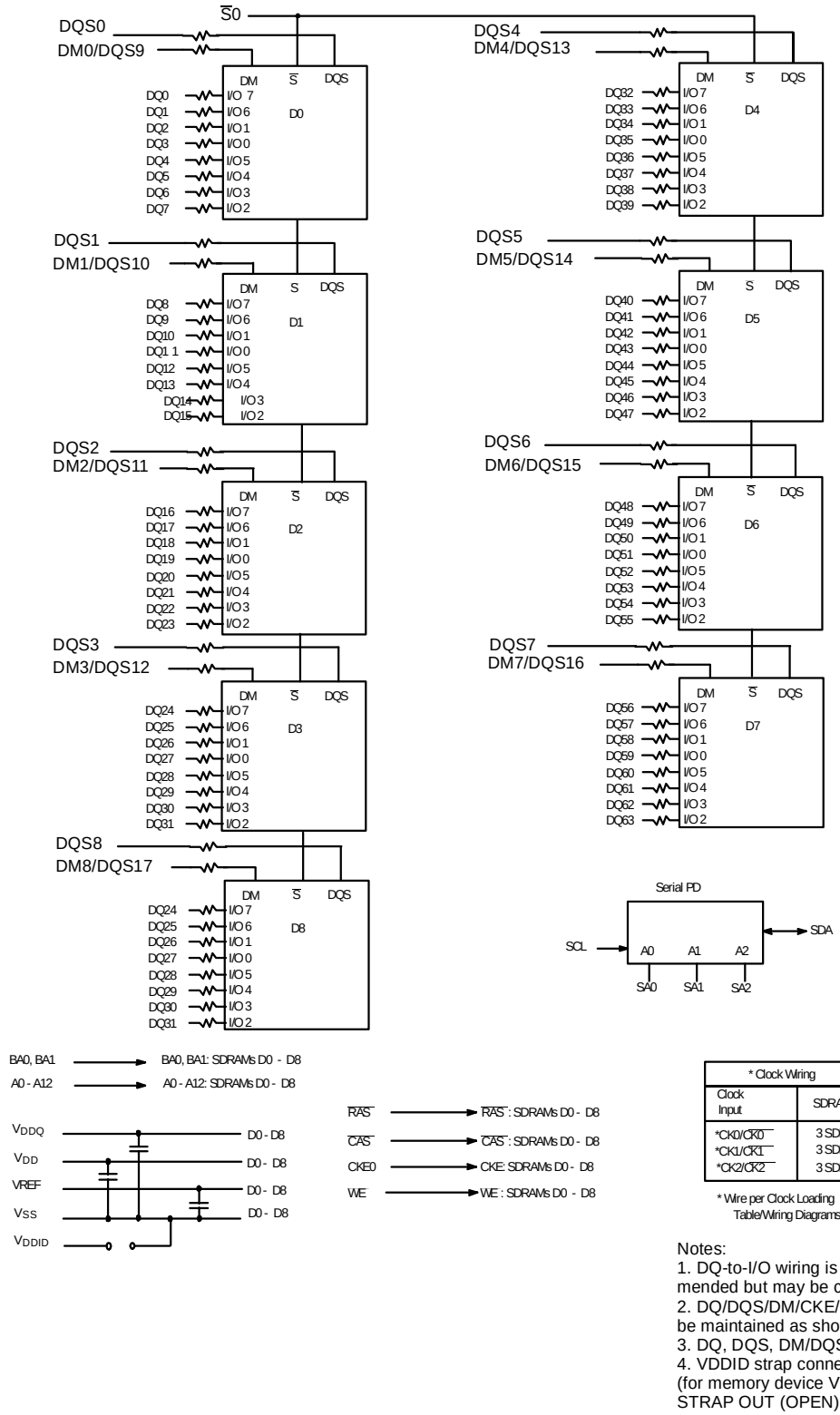
Note: Pins 44, 45, 47, 49, 51, 134, 135, 140 and 144 are NC (“no-connects”) on x64 organised non-ECC modules



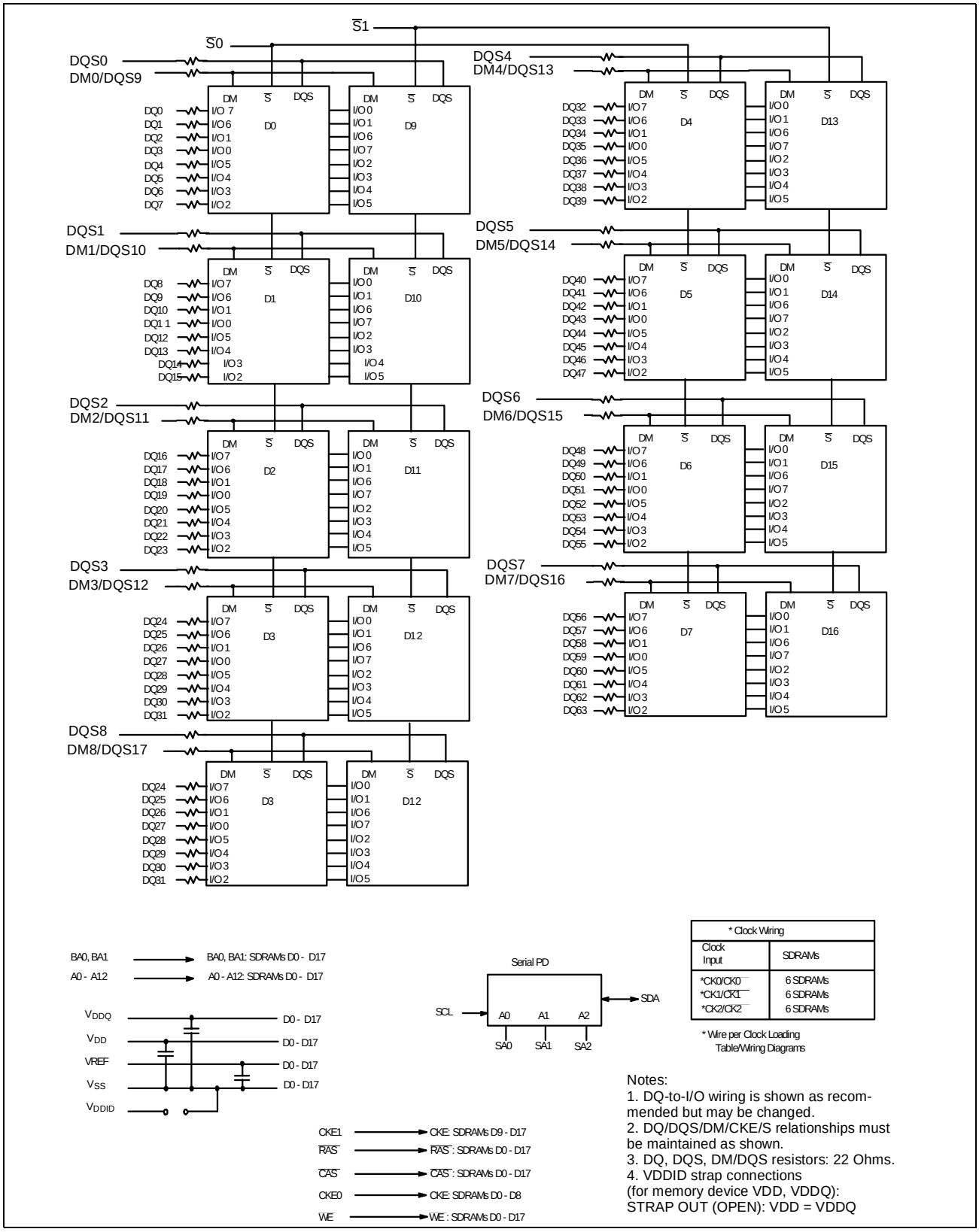
Block Diagram: One Bank 32M × 64 DDR-I SDRAM DIMM Module
HYS64D32000GU using x8 organized SDRAMs on Raw Card Version B



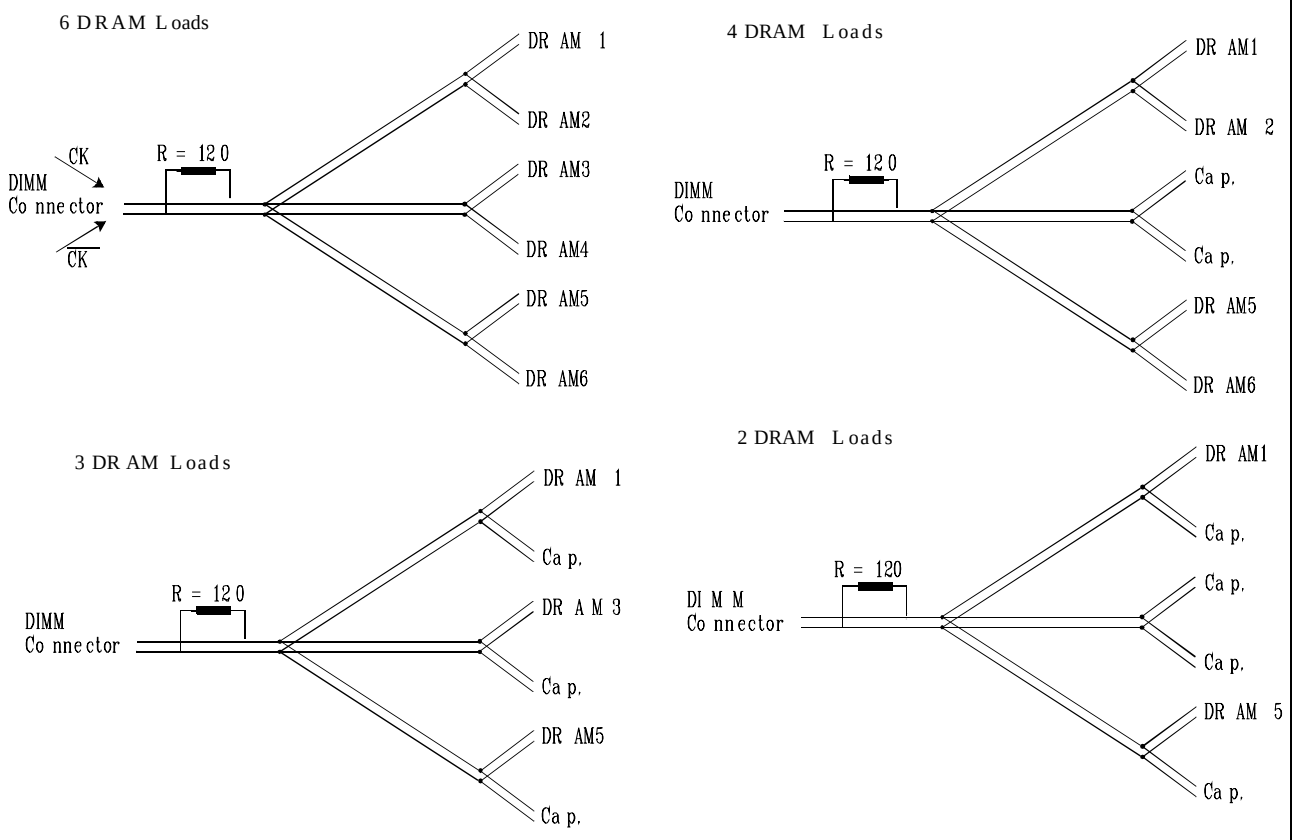
Block Diagram: Two Bank 64M × 64 DDR-I SDRAM DIMM Modules
HYS64D64020GU using x8 Organized SDRAMs on Raw Card Version A



Block Diagram: One Bank 32M × 72 DDR-I SDRAM DIMM Module HYS72D32000GU using x8 organized SDRAMs on Raw Card Version B



Block Diagram: Two Bank 64M × 72 DDR-I SDRAM DIMM Modules
HYS72D64020GU using x8 Organized SDRAMs on Raw Card Version A



Clock Net Wiring

Capacitance (target, not verified)
T_A = 0 to 70 °C; V_{DD} = 2.5 V ± 0.2 V, f = 1 MHz

Parameter	Symbol	Limit Values (max.)		Unit
		One Bank modules	Two Bank Modules	
Input Capacitance (all inputs except CLK,$\overline{\text{CLK}}$ & CKE)	C_{IN}	tbd.	tbd.	pF
Input Capacitance (CLK, $\overline{\text{CLK}}$)	C_{CLK}	tbd.	tbd.	pF
Input Capacitance (CKE)	C_{CKE}	tbd.	tbd.	pF
Input/Output Capacitance (DQ0 - DQ63, CB0 - CB7)	C_{IO}	tbd.	tbd.	pF
Input Capacitance (SCL, SA0 - 2)	C_{SC}	8	8	pF
Input/Output Capacitance (SDA)	C_{SD}	8	8	pF

Supply Voltage Levels

Parameter	Symbol	Limit Values			Unit	Notes
		min.	nom.	max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	–
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	1)
Input Reference Voltage	V_{REF}	1.15	1.25	1.35	V	2)
Termination Voltage	V_{TT}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V	3)

1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.

2) Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\ (DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ}.

3) V_{TT} of the transmitting device must track V_{REF} of the receiving device.

DC Operating Conditions (SSTL_2 Inputs)

(V_{DDQ} = 2.5 V, T_A = 70 °C, Voltage Referenced to V_{SS})

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
DC Input Logic High	$V_{IH\ (DC)}$	V_{REF} + 0.18	V_{DDQ} + 0.3	V	1)
DC Input Logic Low	$V_{IL\ (DC)}$	– 0.30	V_{REF} – 0.18	V	–
Input Leakage Current	I_{IL}	– 5	5	µA	2)
Output Leakage Current	I_{OL}	– 5	5	µA	2)

1) The relationship between the V_{DDQ} of the driving device and the V_{REF} of the receiving device is what determines noise margins. However, in the case of $V_{IH\ (max)}$ (input overdrive), it is the V_{DDQ} of the receiving device that is referenced. In the case where a device is implemented such that it supports SSTL_2 inputs but has no SSTL_2 outputs (such as a translator), and therefore no V_{DDQ} supply voltage connection, inputs must tolerate input overdrive to 3.0 V (High corner V_{DDQ} + 300 mV).

2) For any pin under test input of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V.

Operating, Standby and Refresh Currents (for reference only)
(values apply to one SDRAM component and do not include register and PLL)

(T_A = 0 to +70 °C, V_{DD} = 2.5 V ± 0.2 V)

Parameter	Symbol	Test Condition	Speed			Unit	Notes
			– 7	– 7.5	– 8		
Operating Current t_{RC} = $t_{RC(min)}$, t_{CK} = min. Active-Precharge command without burst operation	I_{CC1}	1 bank operation $\overline{CAS}$ Latency = 2	100	90	70	mA	1), 2), 3)
Precharge Standby Current in Power Down Mode	I_{CC2P}	CKE ≤ $V_{IL(max)}$, t_{CK} = min., $\overline{CS}$ = $V_{IH(min)}$	20	20	20	mA	1)

Operating, Standby and Refresh Currents (cont'd)**(for reference only)**
(values apply to one SDRAM component and do not include register and PLL)

(T_A = 0 to +70 °C, V_{DD} = 2.5 V ± 0.2 V)

Parameter	Symbol	Test Condition	Speed			Unit	Notes
			– 7	– 7.5	– 8		
Precharge Standby Current in Non-Power Down Mode	I_{CC2N}	CKE ≥ $V_{IH(min)}$, t_{CK} = min., $\overline{CS}$ = $V_{IH\ (min)}$	50	45	40	mA	1), 3)
No Operating Current (Active state: 4 bank)	I_{CC3P}	CKE ≤ $V_{IL(max)}$, t_{CK} = min.	30	30	30	mA	1)
	I_{CC3N}	CKE ≥ $V_{IH(min)}$, t_{CK} = min., $\overline{CS}$ = $V_{IH\ (min)}$	65	60	55	mA	1), 3)
Operating Current (Burst Mode)	I_{CC4}	t_{CK} = min., Read/Write command cycling, Multiple banks active, gapless data, BL = 4	140	120	100	mA	1), 2), 3)
Auto (CBR) Refresh Current	I_{CC5}	t_{CK} = min., t_{RC} = $t_{RFC(min)}$ CBR command cycling	155	135	110	mA	1), 4), 5)
Self Refresh Current	I_{CC6}	CKE ≤ 0.2 V	1	1	1	mA	1), 4)

1) These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of t_{CK} and t_{RC}.

2) The specified values are obtained with the output open.

3) Input signals are changed once during three clock cycles.

4) 8192 refresh cycles in 64 ms.

5) Minimum cycle time during Auto Refresh operation (t_{REF}) is greater than minimum cycle time for Read/Write operation.

AC Characteristics (for reference only)
(values apply to the SDRAM component and do not include register, PLL, or card wiring)

(T_A = 0 to + 70 °C, V_{DD} = 2.5 V ± 0.2 V)

Parameter		Symbol	-7 PC266A		-7.5 PC266B		-8 PC200		Unit	Notes
			min.	max.	min.	max.	min.	max.		
DQ Output Access Time from CK/ $\overline{CK}$		t_{AC}	– 0.75	+ 0.75	– 0.75	+ 0.75	– 0.8	+ 0.8	ns	–
DQS Output access Time from CK/ $\overline{CK}$		t_{DQSCK}	– 0.75	+ 0.75	– 0.75	+ 0.75	– 0.8	+ 0.8	ns	–
CLK High Level Width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	*tCK	–
CLK Low Level Width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	*tCK	–
Clock Period	CL = 2	t_{CK}	7.5	20	10	20	10	20	ns	1)
	CL = 2.5		7	20	7.5	20	8	20	ns	–
	CL = 3		7	20	7.5	20	8	20	ns	–
DQ and DM Input Hold Time		t_{DH}	0.5	–	0.5	–	0.6	–	ns	–
DQ and DM Input Setup Time		t_{DS}	0.5	–	0.5	–	0.6	–	ns	–
DQ and DM Input Pulse Width (for each input)		t_{DIPW}	1.75	–	1.75	–	2	–	ns	–
Data-Out High-impedance from CK/ $\overline{CK}$		t_{HZ}	– 0.75	+ 0.75	– 0.75	+ 0.75	– 0.8	+ 0.8	ns	–
Data-Out Low-impedance from CK/ $\overline{CK}$		t_{LZ}	– 0.75	+ 0.75	– 0.75	+ 0.75	– 0.8	+ 0.8	ns	–
DQS-DQ Skew		t_{DQSQ}	–	+ 0.5	–	+ 0.5	–	+ 0.6	ns	–
QH Data-Out Hold Time from DQS		t_{QH}	tHP-0.75	–	tHP-0.75	–	tHP-1.0	–	ns	2)
Write Command to First DQS Latching Transition		t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	*t_{CK}	–
DQS Input Valid Time		$t_{DSL,H}$	0.4	0.6	0.4	0.6	0.4	0.6	*t_{CK}	–
Mode Register/Extended Mode Register Set Cycle Time		t_{MRD}	15	–	15	–	16	–	ns	–
Write Preamble Setup Time		t_{WPRES}	0	–	0	–	0	–	ns	–
DQS Hold Time from CK/$\overline{CK}$		t_{WPREH}	0.25	–	0.25	–	0.25	–	*t_{CK}	–
Write Postamble		t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	*t_{CK}	–
Input Setup Time (LVTTL inputs)		t_{IS}	0.9	–	0.9	–	1.2	–	ns	3)
Input Hold Time (LVTTL inputs)		t_{IH}	0.9	–	0.9	–	1.2	–	ns	3)
Read Preamble		t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	*t_{CK}	–
Read Postamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	*t_{CK}	–
Row Active Time		t_{RAS}	45	120K	45	120k	50	120K	ns	–
Row Cycle Time	R/W Operation	t_{RC}	65	–	65	–	70	–	ns	–
	Auto Refresh	t_{RFC}	75	–	75	–	80	–	ns	1)
$\overline{RAS}$ to $\overline{CAS}$ Delay		t_{RCD}	20	–	20	–	20	–	ns	–
Row Precharge Time		t_{RP}	20	–	20	–	20	–	ns	–
Row Activate to Row Activate Delay		t_{RRD}	15	–	15	–	15	–	ns	–
Write Recovery Time		t_{WR}	15	–	15	–	15	–	ns	–

AC Characteristics (cont'd)**(for reference only)**
(values apply to the SDRAM component and do not include register, PLL, or card wiring)
(T_A = 0 to + 70 °C, V_{DD} = 2.5 V ± 0.2 V)

Parameter	Symbol	-7 PC266A		-7.5 PC266B		-8 PC200		Unit	Notes
		min.	max.	min.	max.	min.	max.		
Auto Precharge Write Recovery + Precharge Time	t_{DAL}	35	–	35	–	35	–	ns	–
Internal Write to Read Command Delay	t_{WTR}	1	–	1	–	1	–	*t_{CK}	–
Power Down Entry Time	t_{PDENT}	t_{IS} + 1 CLK	2 CLK + t_{IS}	–	–	t_{IS} + 1 CLK	2 CLK + t_{IS}	ns	–
Power Down Exit Time	t_{PDEX}	t_{IS} + 1 CLK	2 CLK + t_{IS}	–	–	t_{IS} + 1 CLK	2 CLK + t_{IS}	ns	–
Self Refresh Exit Time	t_{SREX}	200	–	200	–	200	–	Cycles	–
Average Periodic Refresh Intercal	t_{REF}	–	7.8	–	7.8	–	7.8	µs	–
CLK Transition Time	t_T	0.5	–	–	–	0.5	–	ns	–

1) Minimum Auto Refresh cycle time is greater than minimum cycle time during normal Read or Write operation.

2) t_{HP} is the lesser of t_{CL} and T_{CH}

3) These parameters guarantee device timing, but they are not necessarily tested on each device
they may be guaranteed by design or tester correlation
t_{IS} / t_{IH} =0.9ns for PC266 are measured with command / address input slew rate of $\geq$ 1.0V/ns
for command / address input slew rate of $\geq$ 0.5V/ns and < 1.0V/ns t_{IS} / t_{IH} = 1.0ns should be guaranteed by design
for PC200 t_{IS} / t_{IH} = 1.2ns command / address input slew rate of 1.0V/ns is assumed
slew rate is measured between V_{OH}(AC) and V_{OL}(AC)
CK / CK slew rates are assumed to be $\geq$ 1.0V/ns
Pulse width for command / address signals to be properly sampled at rising edges of clock shall be a minimum of 2.2ns

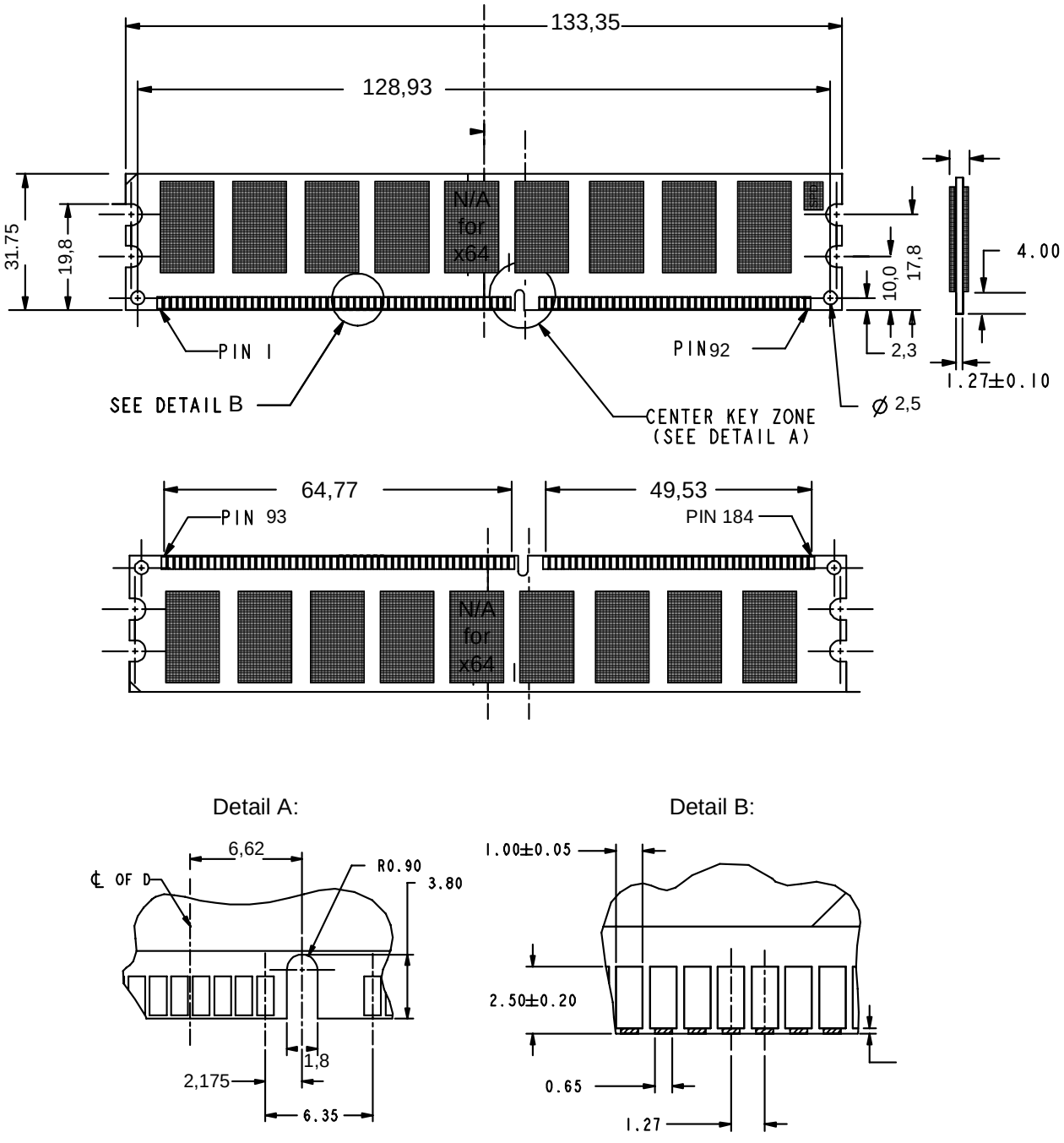
Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	0 to +55	°C	
H_{OPR}	Operating Humidity (relative)	10 to 90	%	
T_{STG}	Storage Temperature	-50 to +100	°C	1)
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1)
	Barometric Pressure (operating and storage)	105 to 69	K Pascal	2)

1) stresses greater than those listed may cause permanent damage to the device. Device functional operation at or above these conditions is not implied.
2) up to 3000 m (9850 ft)

Package Outlines

Simplified Mechanical Drawing
(for details see JEDEC document MO-206a)
DDR-I Unbuffered DIMM Modules



Change List

9.5.2000	Rev.0.9	First target revision