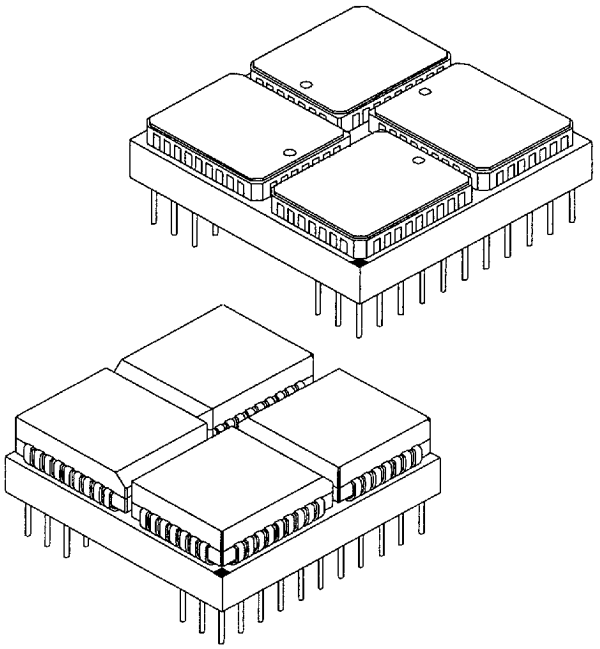
4 MEGABIT FLASH EEPROM

DPZ128X32VI/DPZ128X32VIP

DESCRIPTION:

The DPZ128X32VI/VIP is a 4 megabit CMOS FLASH Electrically Erasable and Programmable nonvolatile memory module. The module is built with four 128K x 8 FLASH memory devices. The DPZ128X32VI/VIP can be user configurable as 512K x 8, 256K x 16 or 128K x 32 bits.

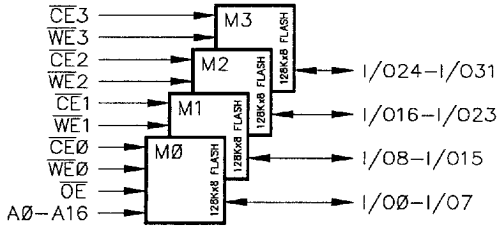
The DPZ128X32VI/VIP is ideal for use in systems that require periodic code updates, or for use as a high speed nonvolatile storage medium.



FEATURES:

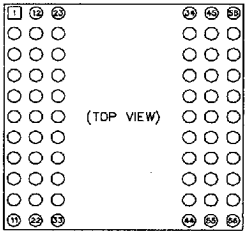
- User Definable Configuration:
  512K x 8, 256K x 16 or 128K x 32
- Fast Read Access Times: 120, 150, 170, 200, 250ns
- Low Power:
  120mA Maximum Active (32 bit Mode)
  400µA Maximum Standby (CMOS)
- 10,000 Erase/Program Cycles Minimum
- Command Register Architecture for Microprocessor Compatible Write Interface.
- 12.0V ±5% V_{PP}
- TTL-Compatible Inputs and Outputs
- Military Versions Available with All Devices used to Construct the Module Compliant to MIL-STD-883; Class B
- 66-Pin Ceramic PGA "VERSAPAC" Package

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O31	Data In/Out
$\overline{CE0}$ - $\overline{CE3}$	Chip Enables
$\overline{WE0}$ - $\overline{WE3}$	Write Enables
$\overline{OE}$	Output Enable
V_{PP}	Programming Voltage
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

PIN-OUT DIAGRAM



1	I/O8	12	$\overline{WE1}$	23	I/O15	34	I/O24	45	VDD	56	I/O31
2	I/O9	13	$\overline{CE1}$	24	I/O14	35	I/O25	46	$\overline{CE3}$	57	I/O3Ø
3	I/O1Ø	14	VSS	25	I/O13	36	I/O26	47	$\overline{WE3}$	58	I/O29
4	A9	15	I/O11	26	I/O12	37	A7	48	I/O27	59	I/O28
5	A16	16	A1Ø	27	$\overline{OE}$	38	A12	49	A4	6Ø	AØ
6	A2	17	A8	28	N.C.	39	VPP	5Ø	A5	61	A1
7	A11	18	A15	29	$\overline{WEØ}$	4Ø	A14	51	A6	62	A3
8	N.C.	19	VDD	3Ø	I/O7	41	A13	52	$\overline{WE2}$	63	I/O23
9	I/OØ	2Ø	$\overline{CEØ}$	31	I/O6	42	I/O16	53	$\overline{CE2}$	64	I/O22
1Ø	I/O1	21	N.C.	32	I/O5	43	I/O17	54	VSS	65	I/O21
11	I/O2	22	I/O3	33	I/O4	44	I/O18	55	I/O19	66	I/O2Ø

DEVICE OPERATION:

The DPZ128X32VI/VIP is an electrically erasable and programmable memory that functions similar to an EPROM type device, but can be erased without removing it from the system and exposing it to ultraviolet light. Each 128K x 8 device on the module can be erased individually eliminating the need to re-program the entire module when partial code changes are required.

READ:

With V_{PP} = 0V to V_{DD}+2.0V *(V_{PPLO})*, the DPZ128X32VI/VIP is a read-only memory and can be read like a standard EPROM. The module can be read as a 32 bit, 16 bit or an 8 bit device. $\overline{CE0}$ through $\overline{CE3}$ select the device to be read. After a device is selected, $\overline{OE}$ is set to a logic-low level to enable the outputs of the module.

When V_{PP} = 12.0V±0.6V *(V_{PPHI})*, reads can be accomplished in the same manner as described above but must be preceded by writing 00H to the command register prior to reading the device. When V_{PP} is raised to V_{PPHI} the contents of the command register default to 00H and remain that way until the command register is altered.

STANDBY:

When $\overline{CE0}$ through $\overline{CE3}$ are raised to a logic-high level, the standby operation disables the DPZ128X32VI/VIP reducing the power consumption substantially. The outputs are placed in a high-impedance state, independent of the $\overline{OE}$ input. If the module is deselected during programming, erasure, or program/erase verification, the device upon which the operation was being performed will continue to draw active current until the operation is completed.

PROGRAM:

The DPZ128X32VI/VIP programming and erasing functions are accessed via the command register when high voltage is applied to V_{PP}. The contents of the command register control the functions of the memory device *(see Command Definition Table)*.

The command register is not an addressable memory location. The register stores the address, data, and command information required to execute the command. When V_{PP} = V_{PPLO} the command register is reset to 00H returning the device to the read-only mode.

The command register is written by enabling the device upon which the operation is to be performed *(see Truth Table)*. While the device is enabled bring $\overline{WE}$ to a logic-low (V_{IL}), the address is latched on the falling edge of $\overline{WE}$ and data is latched on the rising edge of $\overline{WE}$. Programming is initiated by writing 40H *(program setup command)* to the command register. On the next falling edge of $\overline{WE}$ the address to be programmed will be latched followed by the data being latched on the rising edge of $\overline{WE}$ *(see AC Operating and Characteristics Table)*.

PROGRAM VERIFY:

The DPZ128X32VI/VIP is programmed one byte at a time. Each byte may be programmed sequentially or at random. Following each programming operation, the byte must be verified.

To initiate the program-verify mode, C0H must be written to the command register of the device just programmed. The programming operation is terminated on the rising edge of $\overline{WE}$ the program-verify command is written to the command register.

After the program-verify command is written to the command register, the memory device applies an internally generated margin voltage to the byte just written. After waiting t_{WHGL}, the byte can be verified by doing a read. If true data is read from the device, the byte write was successful and the next byte may be programmed.

If the device fails to verify, the program/verify operation is repeated up to 25 times. Failure to verify after 25 program/verify operations indicates a failed device. Most bytes will program on the first or second write.

ERASE:

The DPZ128X32VI/VIP can be erased one 128K x 8 device at a time or two devices can be erased if using the module as a x16 or x32 bit device. The erase function is a command-only operation and can only be executed while V_{PP} = V_{PPHI}.

To setup the chip-erase, 20H must be written to the command register. The chip-erase is then executed by once again writing 20H to the command register *(see AC Operating and Characteristics Table)*.

To ensure a reliable erasure, all bits in the device to be erased should be programmed to their charged state *(data = 00H)* prior to starting the erase operation. With the algorithm provided, this operation should take approximately 2 minutes.

HIGH PERFORMANCE PARALLEL ERASURE:

Dense-Pac recommends that all users implement the following Intel High Performance Parallel Erase algorithm in order to avoid the possibility of over erasing these parts.

In applications containing more than one FLASH memory, you can erase each device serially or you can reduce total erase time by implementing a parallel erase algorithm. You may save time by erasing all devices at the same time. However, since FLASH memories may erase at different rates, you must verify each device separately. This can be done in a word-wise fashion with the Command Register Reset Command and a special masking algorithm.

Take for example the case of two-device (parallel) erasure. The CPU first writes the data word erase command 2020H twice in succession. This starts erasure. After 10ms, the CPU writes the data word verify command A0A0H to stop erasure and setup erase verification. If both one or both bytes are not erased at the given address, the CPU implements the erase sequence again without incrementing the address.

Suppose at the given address only the low byte verifies FFH data? Could the whole chip be erased? The answer is yes. Rather than check the rest of the low byte addresses independently of the high byte, simply use the reset command to mask the low byte from erasure and erase verification on the next erase loop. In this example the erase command would be 20FFH and the verify command would be A0FFH. Once the high byte verifies at the address, the CPU modifies the command back to the default 2020H and A0A0H, increments to the next address, and then writes the verify command.

See Figure 4 for a conceptual view of the parallel erase flow chart and Figure 4 for the detailed version. These flow charts are for the 16-bit systems and can be expanded for 32-bit designs.

ERASE VERIFY:

The erase operation erases all bytes in the device selected in parallel. Upon completion of the erase operation, each byte

must be verified. This operation is initiated by writing A0H to the command register. The address to be verified must be supplied because it is latched on the falling edge of $\overline{WE}$.

The memory device internally generates a margin voltage and applies it to the addressed byte. If FFH is read from the device, it indicates the byte is erased. The erase/verify command is issued prior to each byte verification to latch the address of the byte to be verified. This continues until FFH is not read from the device or the last address for the device being erased is read.

If FFH is not read from the byte being verified, an additional erase operation is performed. Verification then resumes from the last byte verified. Once all bytes in the device being erased are verified, the erase operation is complete. The verify operation should now be terminated by writing a valid command such as program set-up to the command register.

RESET:

The reset command is provided as a way to safely abort a program or erase command operation. Following either the program setup command *(40H)* or the set-up erase command *(20H)*, two consecutive writes of FFH will safely abort either operation. If the reset command is issued prior to the program command or the erase command, the memory contents will not be altered. A valid command must then be written to put the device in another mode.

DESIGN CONSIDERATIONS:

V_{PP} traces should use similar trace widths and layout considerations as the V_{DD} power bus. The V_{PP} supply traces should also be decoupled to help decrease voltage spikes.

Power-up sequencing should be such that V_{PP} doesn't go above $V_{DD}+2.0V$ before V_{DD} reaches a steady state voltage, while on power-down V_{PP} should be below $V_{DD}+2.0V$ before V_{DD} is lowered.

While the DPZ128X32VI/VIP memory module has high-frequency, low-inductance decoupling capacitors mounted on the substrate connected to V_{DD} and V_{SS}, it is recommended that a 4.7µF to 10µF electrolytic capacitor be placed near the memory module connected across V_{DD} and V_{SS} for bulk storage.

TRUTH TABLE

Mode	Description	$\overline{CE}$n	$\overline{WE}$	$\overline{OE}$	V_{PP}	Data I/O
READ - ONLY	Not Selected	H	X	X	V_{PPLO}	HIGH-Z
	Output Disable	L	H	H	V_{PPLO}	HIGH-Z
	Read	L	H	L	V_{PPLO}	DOUT
READ/WRITE	Not Selected	H	X	X	V_{PPHI}	HIGH-Z
	Output Disable	L	H	H	V_{PPHI}	HIGH-Z
	Read	L	H	L	V_{PPHI}	DOUT
	Write	L	L	H	V_{PPHI}	DIN

L = LOW, H = HIGH, X = Don't Care

COMMAND DEFINITION TABLE

Command	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Operation	Address	Data	Operation	Address	Data
Read Memory	1	Write	X	00H	-	-	-
Setup Erase / Erase	2	Write	X	20H	Write	X	20H
Erase Verify	2	Write	EA	A0H	Read	X	EVD
Setup Program / Program	2	Write	X	40H	Write	PA	PD
Program Verify	2	Write	X	C0H	Read	X	PVD
Reset	2	Write	X	FFH	Write	X	FFH

EA = Address to Verify
EVD = Data Read from Location EA
PVA = Data to be Read from Location PA at Program Verify

PA = Address to Program
PD = Data to be Programmed at Location PA

ABSOLUTE MAXIMUM RATINGS [1]			
Symbol	**Parameter**	**Value**	**Unit**
T_{STC}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
$V_{I/O}$	Voltage on any Pin	-0.5 to +7.0 [2]	V
V_{PP}	V_{PP} Supply Voltage During Erase/Program	-0.5 to +14.0 [3]	V
V_{DD}	Supply Voltage	-0.6 to +7.0 [2]	V
I_{OUT}	Output Current	100 [4]	mA

RECOMMENDED OPERATING RANGE[5]						
Symbol	**Characteristic**		**Min.**	**Typ.**	**Max.**	**Unit**
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{IL}	Input LOW Voltage		-0.5		0.8	V
V_{IH}	Input HIGH Voltage		2.0		V_{DD}+0.5	V
T_A	Operating Temperature	C	0	+25	+70	°C
		I	-40	+25	+85	
		M/B	-55	+25	+125	

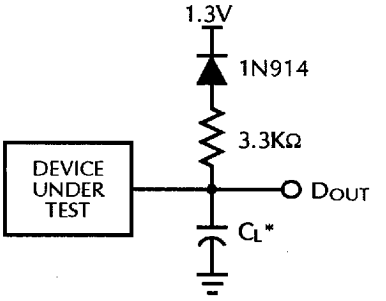
CAPACITANCE [6]: T_A = 25°C, F = 1.0MHz				
Symbol	**Parameter**	**Max.**	**Unit**	**Condition**
C_{ADR}	Address Input	100	pF	V_{IN} [3] = 0V
C_{CE}	Chip Enable	15		
C_{WE}	Write Enable	50		
C_{OE}	Output Enable	100		
$C_{I/O}$	Data Input/Output	100		

DC OPERATING CHARACTERISTICS: Over operating ranges									
Symbol	**Characteristics**	**Conditions**	**X8**		**X16**		**X32**		**Unit**
			Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} to V_{SS}	-5	+5	-5	+5	-5	+5	µA
I_{OL}	Output Leakage Current	V_{OUT} = V_{DD} or V_{SS}	-40	+40	-20	+20	-10	+10	µA
I_{CC1}	V_{DD} Active Read Current	$\overline{CE}$ = V_{IL}, f = 6MHz, I_{OUT} = 0mA		30		60		120	mA
I_{CC2}	V_{DD} Programming Current	Programming in Progress		30		60		120	mA
I_{CC3}	V_{DD} Erase Current	Erasure in Progress		30		60		120	mA
I_{SB1}	VDD Supply Standby Current (CMOS)	$\overline{CE}$ = V_{DD} -0.2V, V_{IN} ≥ V_{DD} -0.2V or V_{IN} ≤ 0.2V		400		400		400	µA
I_{SB2}	V_{DD} Standby Supply Current (TTL)	$\overline{CE}$ = V_{IH}, V_{IN} = V_{IH} or V_{IN} - V_{IL}		4		4		4	mA
I_{PPS}	V_{PP} Leakage Current	V_{PP} = V_{PPLO}		4		4		4	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPHI}		200		200		200	µA
		V_{PP} = V_{PPLO}		4		4		4	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPHI}, Programming in Progress		30		60		120	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPHI}, Erasure in Progress		30		60		120	mA
V_{IL}	Input LOW Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
V_{IH}	Input HIGH Voltage		2.2	V_{DD}+0.5	2.2	V_{DD}+0.5	2.2	V_{DD}+0.5	V
V_{OL}	Output LOW Voltage	I_{OL} = 5.8mA		0.45		0.45		0.45	V
V_{OH}	Output HIGH Voltage	I_{OH} = -2.5mA	2.4		2.4		2.4		V
V_{PPLO}	V_{PP} During Read-Only Operations		0	V_{DD}+2.0	0	V_{DD}+2.0	0	V_{DD}+2.0	V
V_{PPLH}	V_{PP} During Read/Write Operations		11.4	12.6	11.4	12.6	11.4	12.6	V

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Timing Reference Levels During Verify	0.8V and +2.4V

OUTPUT LOAD		
Load	**C_L**	**Parameters Measured**
1	100 pF	except t_{DF}, t_{LZ} and t_{OLZ}
2	30pF	t_{DF}, t_{LZ} and t_{OLZ}

Figure 1. Output Load
* Including Probe and Jig Capacitance.

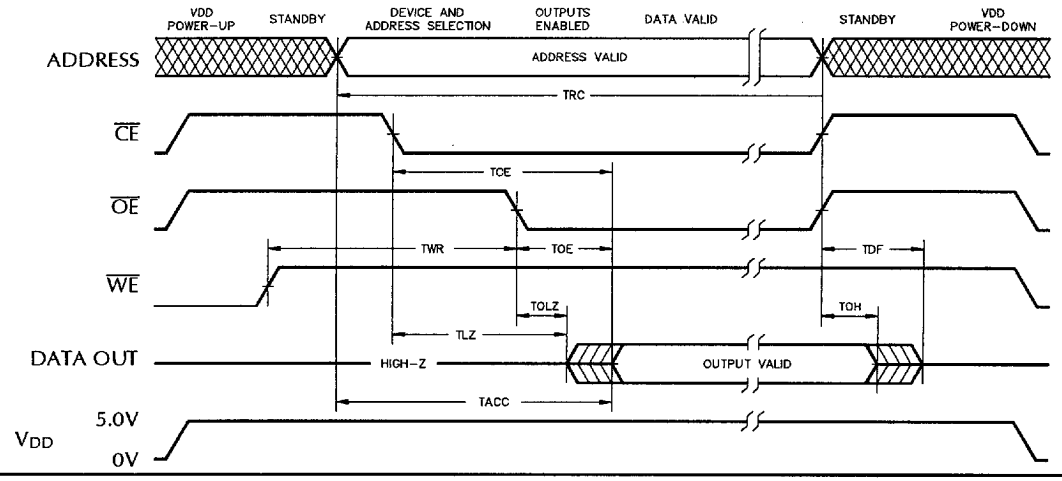


AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges													
No.	**Symbol**	**Parameter**	**120ns †**		**150ns †**		**170ns ‡**		**200ns ‡**		**250ns ‡**		**Unit**
			Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
1	t_{RC}	Read Cycle Time	120		150		170		200		250		ns
2	t_{CE}	Chip Enable Access Time		120		150		170		200		250	ns
3	t_{ACC}	Address Access Time		120		150		170		200		250	ns
4	t_{OE}	Output Enable Access Time		50		55		60		60		65	ns
5	t_{LZ}	Chip Enable to Output in LOW-Z [6,7]	0		0		0		0		0		ns
6	t_{OLZ}	Output Enable to Output in LOW-Z [6,7]	0		0		0		0		0		ns
7	t_{DF}	Output Disable to Output in HIGH-Z [6,7]		30		35		40		45		60	ns
8	t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Change (whichever occurs first)	0		0		0		0		0		ns

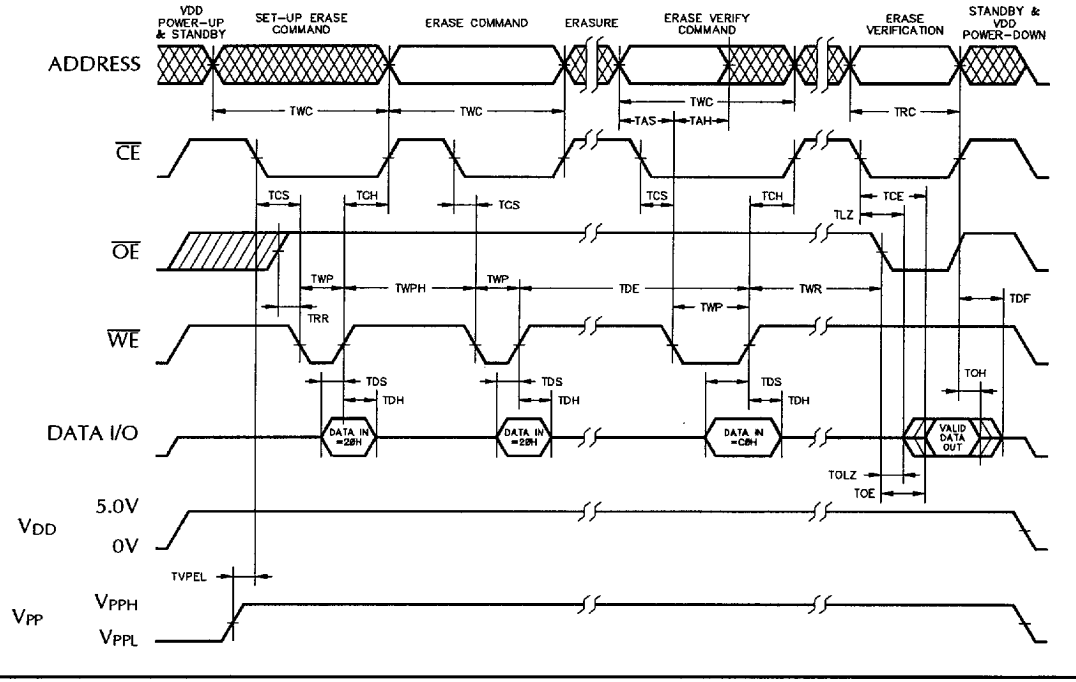
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges													
No.	**Symbol**	**Parameter**	**120ns †**		**150ns †**		**170ns ‡**		**200ns ‡**		**250ns ‡**		**Unit**
			Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
9	t_{WC}	Write Cycle Time	120		150		170		200		250		ns
10	t_{AS}	Address Setup Time	0		0		0		0		0		ns
11	t_{AH}	Address Hold Time	60		60		60		60		60		ns
12	t_{DS}	Data Setup Time	50		50		50		50		50		ns
13	t_{DH}	Data Hold Time	10		10		10		10		10		ns
14	t_{WR}	Write Recovery Time before Read	6		6		6		6		6		µs
15	t_{RR}	Read Recover Time before Write	0		0		0		0		0		ns
16	t_{CS}	Chip Enable Setup Time before Write	20		20		20		20		20		ns
17	t_{CH}	Chip Enable Hold Time	0		0		0		0		0		ns
18	t_{WP}	Write Pulse Width [8]	60		60		80		80		80		ns
19	t_{WPH}	Write Pulse Width HIGH [8]	20		20		20		20		20		ns
20	t_{DP}	Duration of Programming Operation	10		10		10		10		10		µs
21	t_{DE}	Duration of Erase Operation	9.5	10.5	9.5	10.5	9.5	10.5	9.5	10.5	9.5	10.5	ms
22	t_{VPEL}	V_{PP} Setup Time to Chip Enable LOW [3]	1.0		1.0		1.0		1.0		1.0		µs

† Commercial only.
‡ Military only.

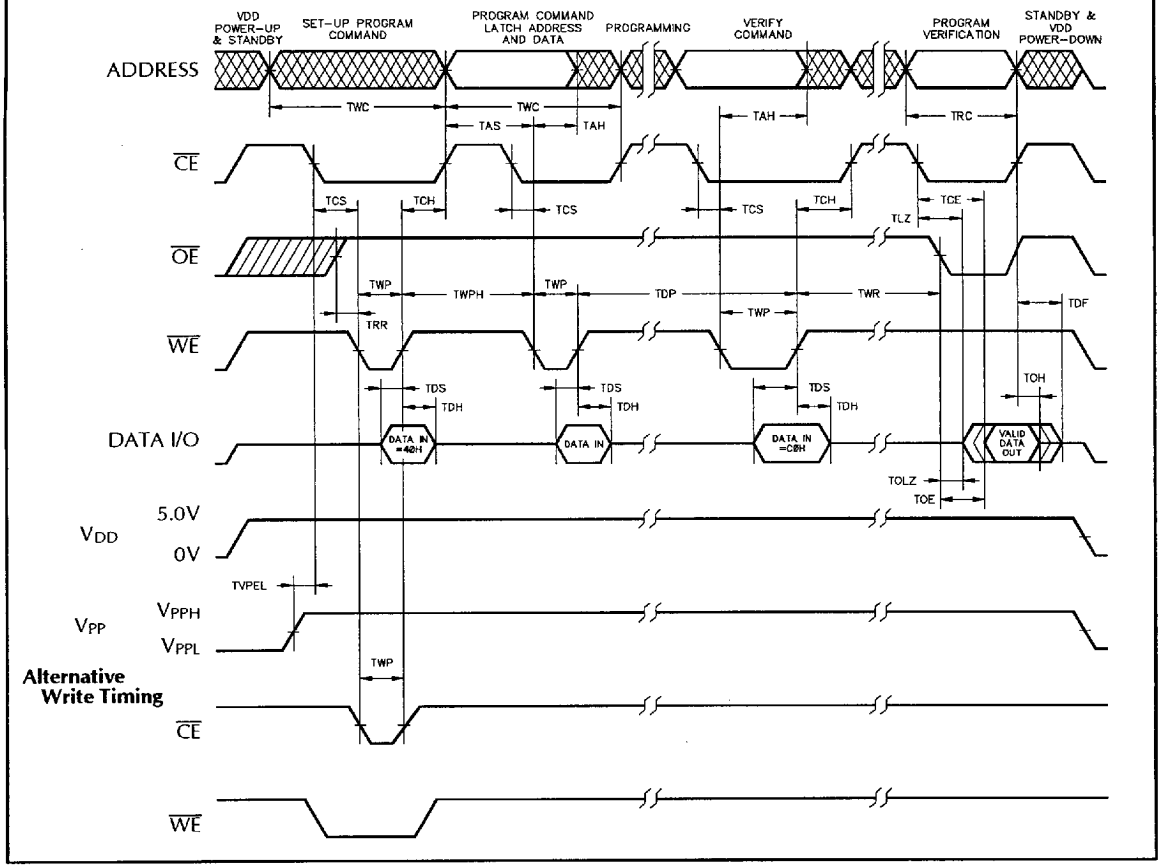
READ CYCLE



ERASE CYCLE



PROGRAMMING CYCLE [8]



NOTES:

1. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Maximum DC voltage on V_{PP} or A9 may over shoot to +14.0V for periods less than 20ns.
4. Output shorted for no more than 1 second. No more than one output shorted at a time.
5. All voltages are with respect to V_{SS}.
6. This parameter is guaranteed and not 100% tested.
7. Transition is measured at the point of ±500mV from steady state voltage.
8. Chip Enable Controlled Writes: Write operations are driven by the valid combination of Chip Enable and Write Enable. In systems where Chip Enable defines the write pulse width *(within a longer Write Enable timing waveform)* all Set-up, Hold, and inactive Write Enable times should be measured relative to the Chip Enable waveform.

FIGURE 2: WRITE ALGORITHM

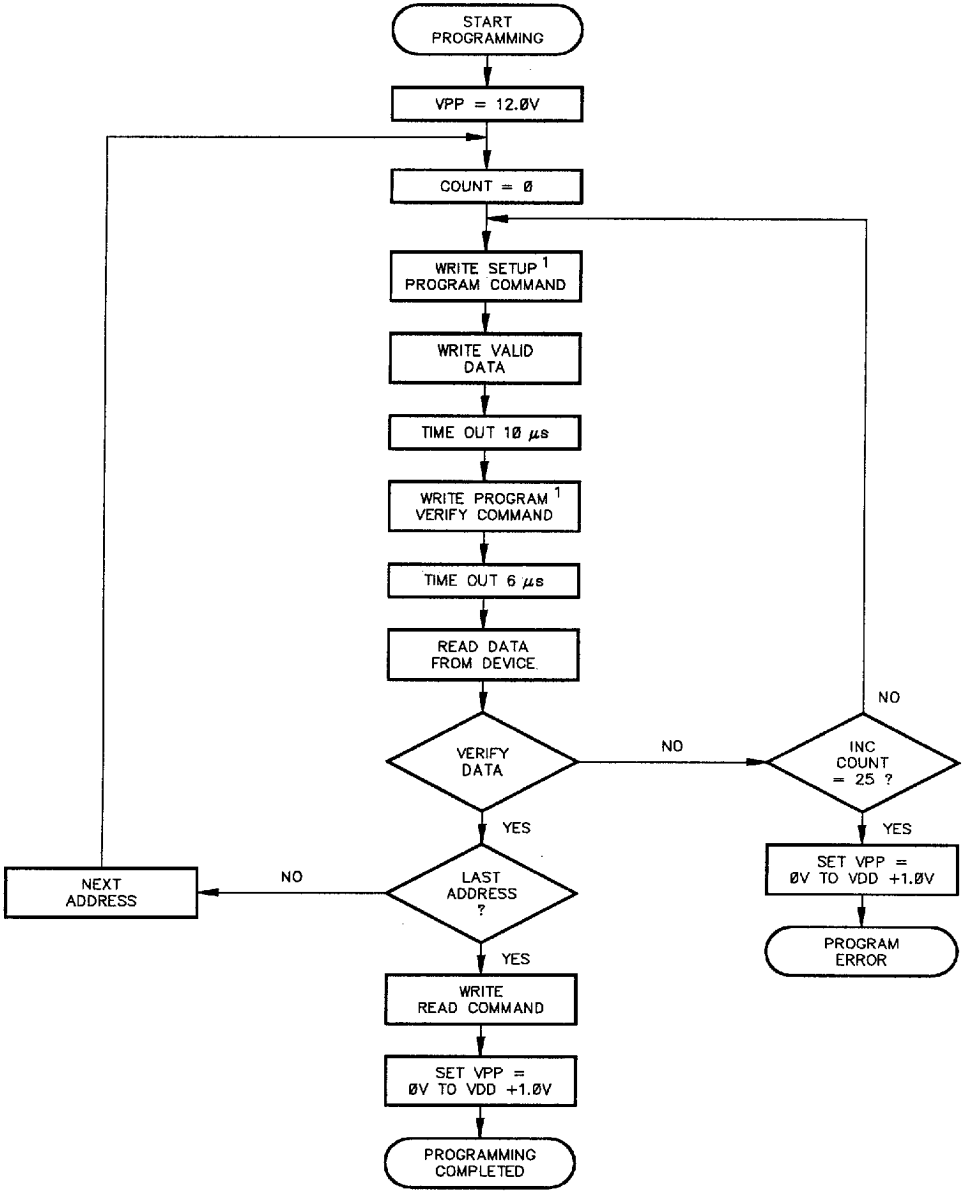


FIGURE 3: ERASE ALGORITHM

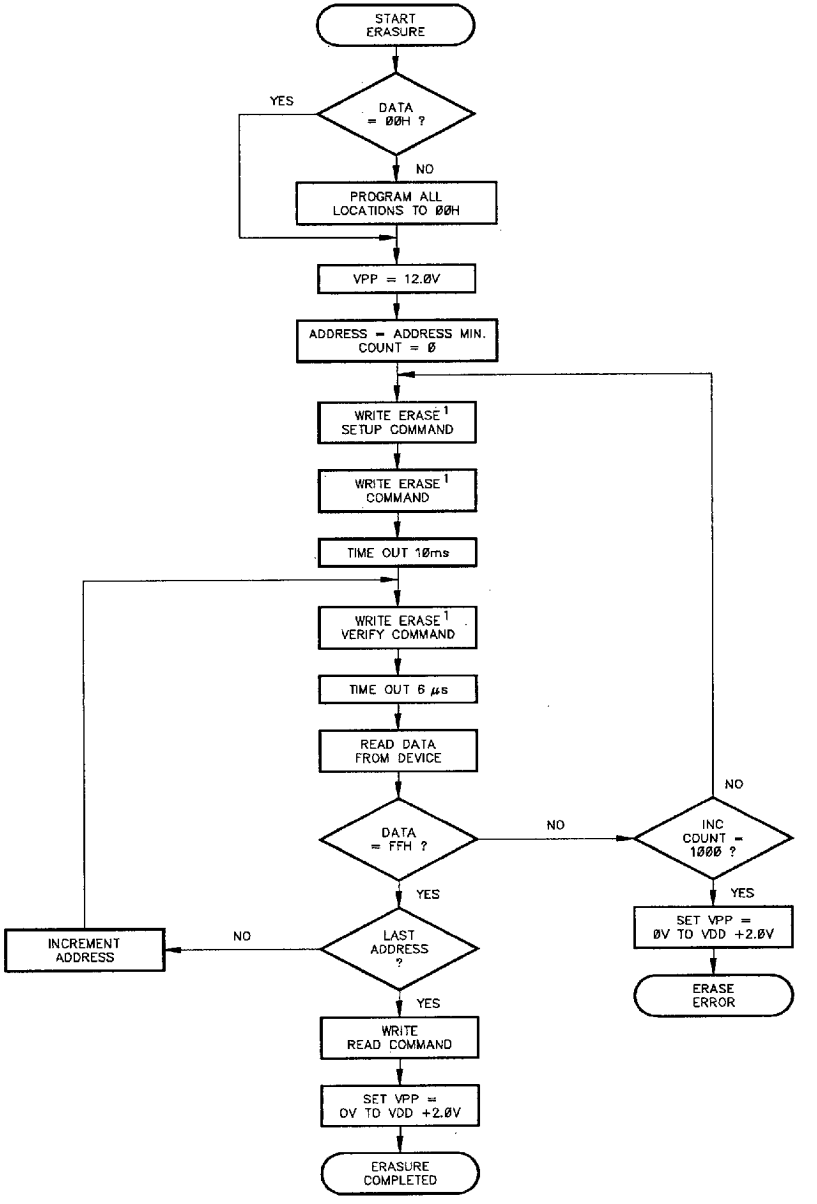


FIGURE 4: HIGH PERFORMANCE PARALLEL ERASURE (Conceptual Device)

NOTES:

[1] You mask the device by substituting a reset command for the erase and verify commands, that way the erased byte idles through the next erase loop.

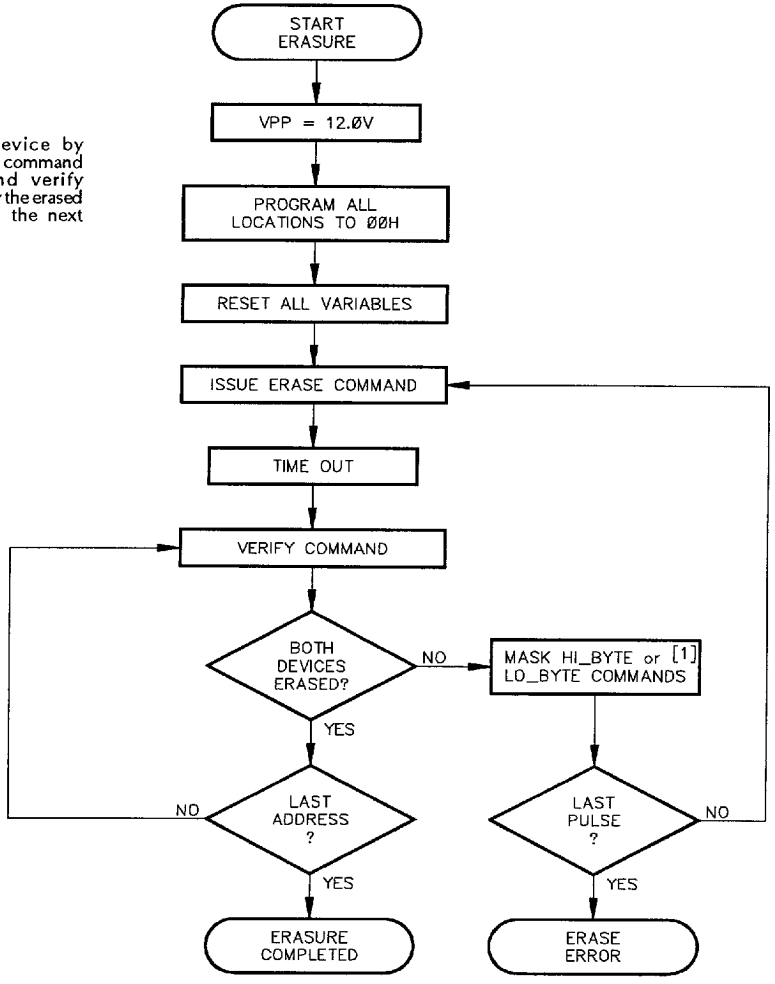


FIGURE 5: PARALLEL ERASE FLOW CHART

NOTES:

[1] Wait for VPP to stabilize.

[2] Use Quick-Pulse Programming algorithm.

[3] Initialize Variables:

PLSCNT_HI	=	High Byte Pulse Counter
PLSCNT_LO	=	Low Byte Pulse Counter
FLAG	=	Erase Error Flag
ADRS	=	Address
E_COM	=	Erase Command
V_COM	=	Verify Command

[4] Erase Verify Command stops erasure.

[5] See Figure 6 for subroutine.

[6] When both devices at ADRS are erased, F_DATA = FFFFH.

[7] Reset commands to default E_COM = 2020H, V_COM = A0A0H before verifying next ADRS.

[8] Reset device for read operation.

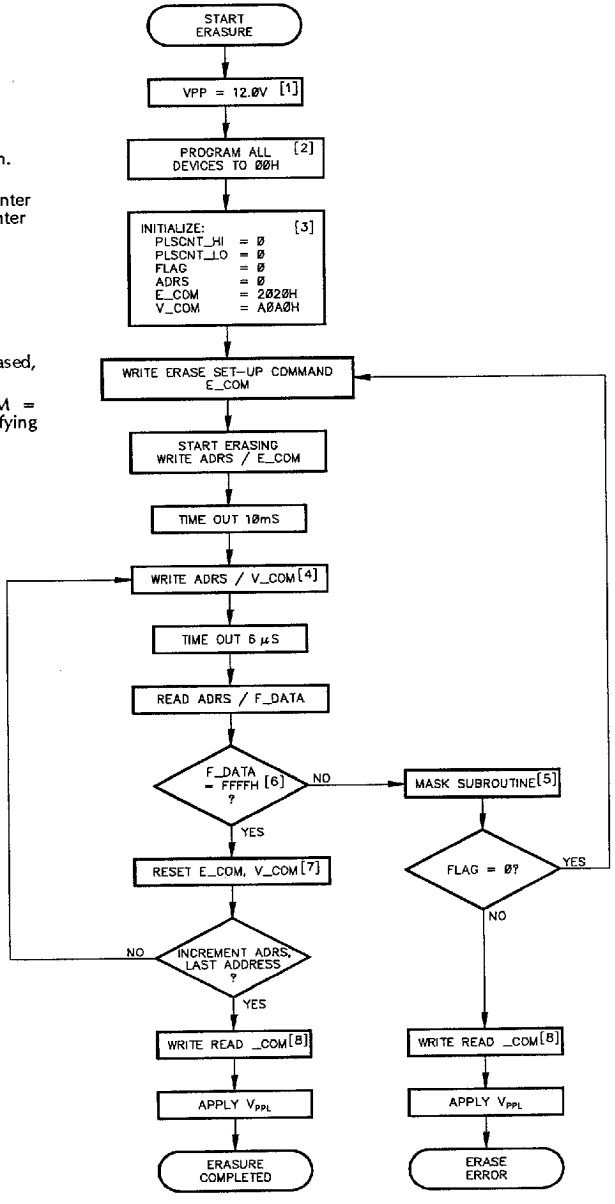


FIGURE 6: DEVICE ERASE VERIFY AND MASK SUBROUTINE

NOTES:

[1] This subroutine masks the High byte or Low Byte of the Erase and Verify commands from executing during the next operation.

[2] Mask the High byte with 00H.

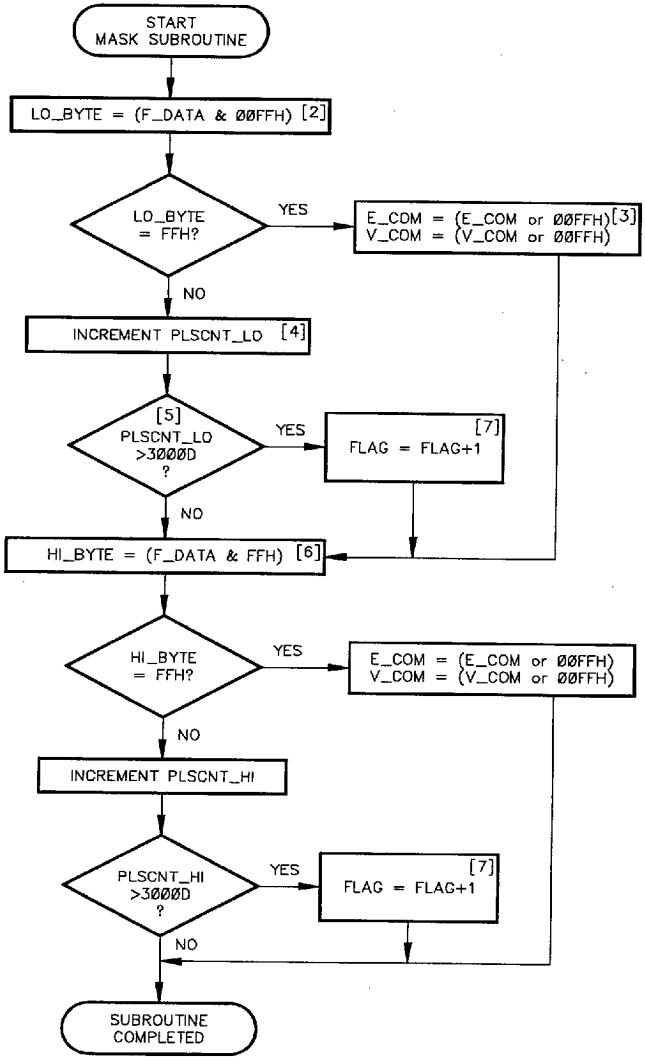
[3] If the Low byte verifies erasure, then mask the next erase and verify commands with FFH (reset).

[4] If the Low byte does not verify, increment its pulse counter.

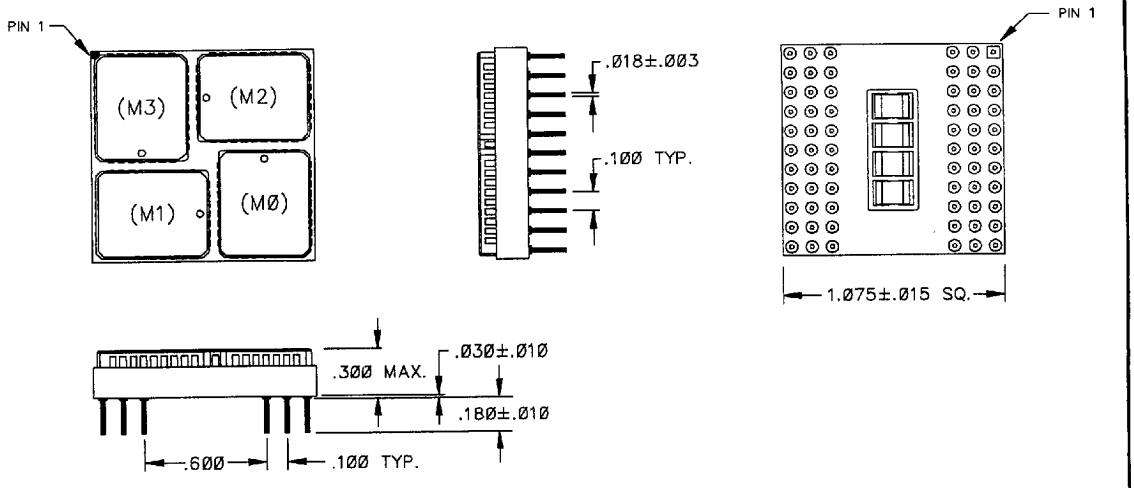
[5] Check for max. count. FLAG = 1 denotes a Low byte error.

[6] Repeat sequence for High byte.

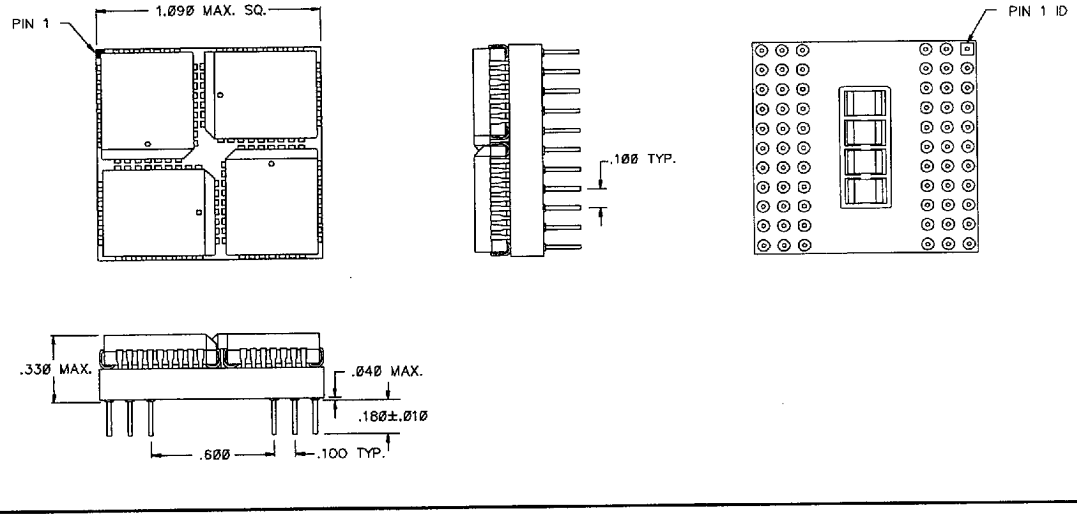
[7] FLAG = 2 denotes a High byte error. FLAG = 3 denotes both High byte and Low byte errors.



DPZ128X32VI - MECHANICAL DRAWING



DPZ128X32VIP - MECHANICAL DRAWING



ORDERING INFORMATION

DP Z 128 X 32 V I P – XX X

PREFIX | TYPE | MEMORY DEPTH | DESIG. | MEMORY DEPTH | PACKAGE | VENDOR | DESIG. | SPEED | GRADE

GRADE:
- C** COMMERCIAL Ø° to +7Ø°C
- M MILITARY –55° to +125°C
- B* MIL–PROCESSED –55° to +125°C

SPEED:
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- 17 170ns M/B GRADE ONLY
- 2Ø 200ns M/B GRADE ONLY
- 25 250ns M/B GRADE ONLY

DESIG.:
- BLANK CERAMIC DEVICES
- P PLASTIC DEVICES

VENDOR: INTEL 28F01Ø DEVICES

PACKAGE: VERSAPAC, 66 PIN PGA (PIN GRID ARRAY)

MEMORY DEPTH: MODULE WITHOUT LOGIC SUPPORT

TYPE: CMOS FLASH EEPROM

* Built with 883 devices.
** Available in plastic PLCC's only.

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