

74ABT162244

16-Bit Buffer/Line Driver

with 25Ω Series Resistors in the Outputs

General Description

The 'ABT162244 contains sixteen non-inverting buffers with TRI-STATE® outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Individual TRI-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

Features

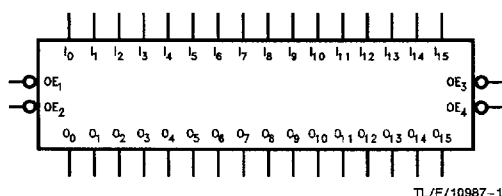
- Separate control logic for each nibble
- 16-bit version of the 'ABT2244
- Guaranteed latch protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

Commercial	Package Number	Package Description
74ABT162244CSSC (Note 1)	MS48A	48-Lead (0.300" Wide) Molded Shrink Small Outline, JEDEC (SSOP)
74ABT162244CMTD (Notes 1, 2)	MTD48	48-Lead Molded Thin Shrink Small Outline, JEDEC (TSSOP)

Note 1: Devices also available in 13" reel. Use suffix = SSCX and MTDX.

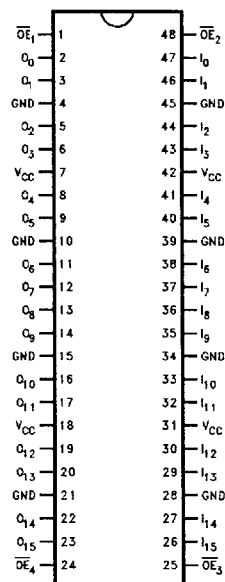
Note 2: Contact factory for package availability

Logic Symbol



Connection Diagram

Pin Assignment for SSOP



Pin Description

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
I_0-I_{15}	Inputs
O_0-O_{15}	Outputs

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Functional Description

The ABT162244 contains sixteen non-inverting buffers with TRI-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but indepen-

dent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0-I_3	O_0-O_3
L	L	L
L	H	H
H	X	Z

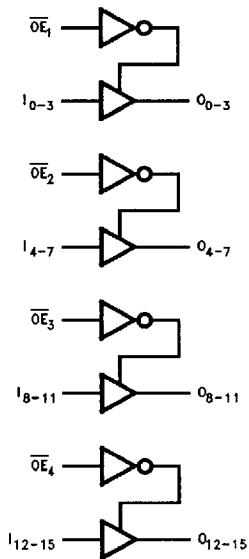
Inputs		Outputs
$\overline{OE}_2$	I_4-I_7	O_4-O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8-I_{11}	O_8-O_{11}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	$I_{12}-I_{15}$	$O_{12}-O_{15}$
L	L	L
L	H	H
H	X	Z

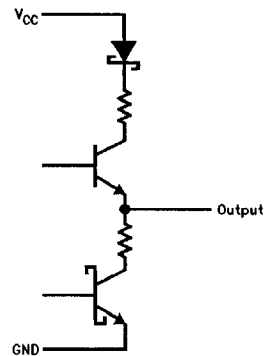
H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagrams



TL/F/10987-3

Schematic of each Output



TL/F/10987-4

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias Plastic	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	−40°C to +85°C
Supply Voltage Commercial	+4.5V to +5.5V
Minimum Input Edge Rate (ΔV/Δt)	
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT162244			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	74ABT	2.5		V	Min	I _{OH} = −3 mA
		74ABT	2.0		V	Min	I _{OH} = −32 mA
V _{OL}	Output LOW Voltage	74ABT		0.8	V	Min	I _{OL} = 12 mA
I _{IH}	Input HIGH Current			5	μA	Max	V _{IN} = 2.7V (Note 1) V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current			−5	μA	Max	V _{IN} = 0.5V (Note 1) V _{IN} = 0.0V
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OZH}	Output Leakage Current			50	μA	0 − 5.5V	V _{OUT} = 2.7V; $\overline{OE}_n$ = 2.0V
I _{OZL}	Output Leakage Current			−50	μA	0 − 5.5V	V _{OUT} = 0.5V; $\overline{OE}_n$ = 2.0V
I _{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V _{OUT} = 0.0V
I _{CEX}	Output High Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test			100	μA	0.0	V _{OUT} = 5.5V; All Others GND
I _{CCH}	Power Supply Current			2.0	mA	Max	All Outputs HIGH
I _{CCCL}	Power Supply Current			60	mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current			2.0	mA	Max	$\overline{OE}_n$ = V _{CC} All Others at V _{CC} or GND
I _{CCCT}	Additional I _{CC} /Input	Outputs Enabled Outputs TRI-STATE Outputs TRI-STATE	3.0		mA	Max	V _I = V _{CC} − 2.1V
			3.0		mA		Enable Input V _I = V _{CC} − 2.1V
			50		μA		Data Input V _I = V _{CC} − 2.1V All Others at V _{CC} or GND
I _{CCD}	Dynamic I _{CC} (Note 1)	No Load		0.1	mA/ MHz	Max	Outputs Open $\overline{OE}_n$ = GND One Bit Toggling, 50% Duty Cycle

Note 1: Guaranteed, but not tested

AC Electrical Characteristics

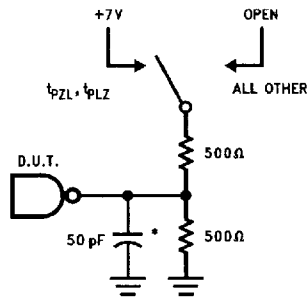
Symbol	Parameter	74ABT			74ABT		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5\text{V}$ $C_L = 50\text{ pF}$			$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	
t_{pLH} t_{pHL}	Propagation Delay Data to Outputs	1.0	2.4	3.9	1.0	3.9	ns
		1.0	3.2	4.7	1.0	4.7	
t_{pZH} t_{pZL}	Output Enable Time	1.5	3.5	6.3	1.5	6.3	ns
		1.5	4.2	6.9	1.5	6.9	
t_{pHZ} t_{pLZ}	Output Disable Time	1.0	4.2	6.7	1.0	6.7	ns
		1.0	3.8	6.7	1.0	6.7	

Capacitance

Symbol	Parameter	Typ	Units	Conditions, $T_A = 25^{\circ}\text{C}$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0.0\text{V}$
$C_{OUT}(\text{Note 1})$	Output Capacitance	9.0	pF	$V_{CC} = 5.0\text{V}$

Note 1: C_{OUT} is measured at frequency $f = 1\text{ MHz}$ per MIL-STD-883B, Method 3012

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

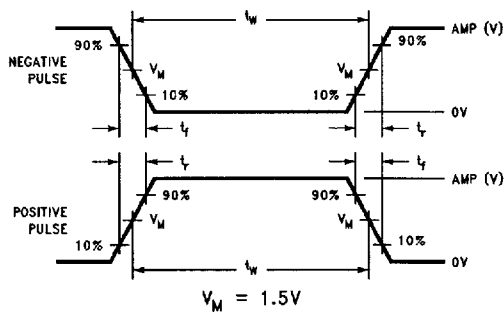


FIGURE 2a. Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 2b. Test Input Signal Requirements

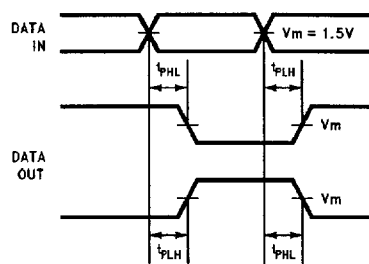


FIGURE 3. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

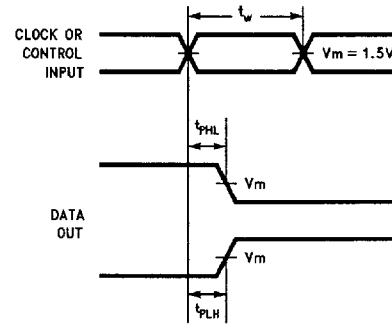


FIGURE 4. Propagation Delay, Pulse Width Waveforms

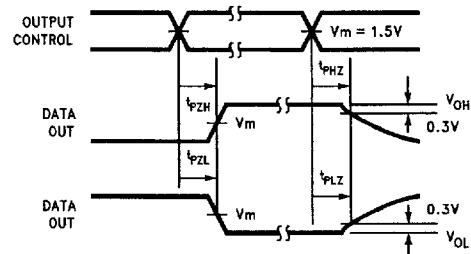


FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Times

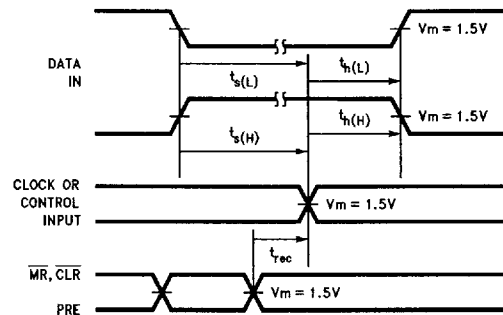
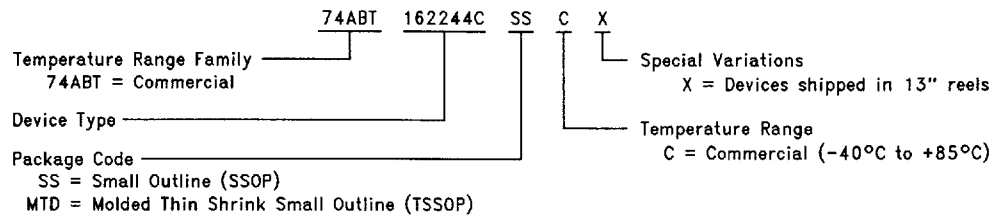


FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

Ordering Information

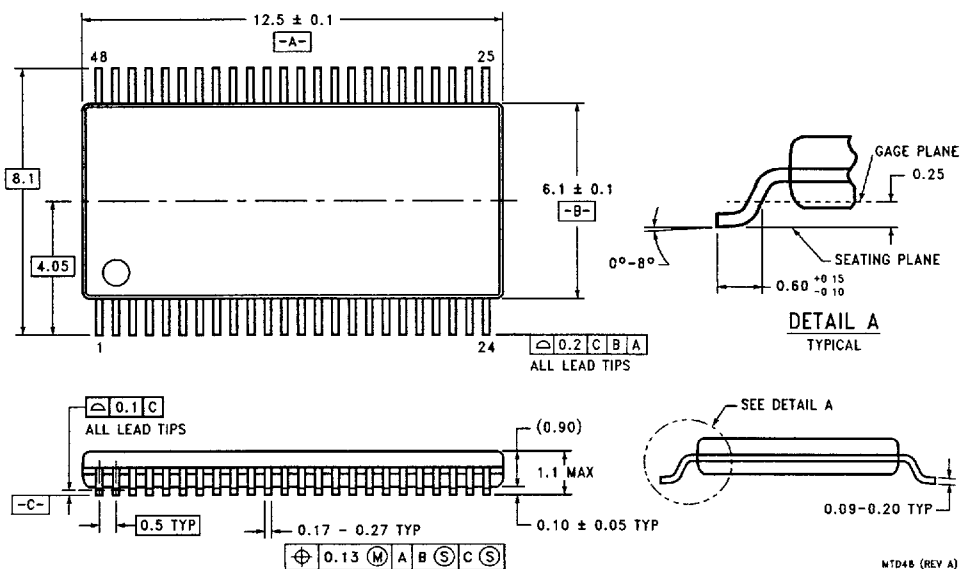
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/10987-13

**74ABT162244 16-Bit Buffer/Line Driver
with 25Ω Series Resistors in the Outputs**

Physical Dimensions millimeters (Continued)



**48-Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTD48**

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