

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature (T_{STG})	-65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
V_{EE} Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 2)	≥2000V

Military Version DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$

Symbol	Parameter	Min	Max	Units	T _C	Conditions		Notes
V _{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V _{IN} = V _{IH (Max)} or V _{IL (Min)}	Loading with 50Ω to −2.0V	(Notes 3, 4, 5)
		−1085	−870	mV	−55°C			
V _{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V _{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V _{IN} = V _{IH (Min)} or V _{IL (Max)}	Loading with 50Ω to −2.0V	(Notes 3, 4, 5)
		−1085		mV	−55°C			
V _{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V _{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for All Inputs		(Notes 3, 4, 5, 6)
V _{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs		(Notes 3, 4, 5, 6)
I _{IL}	Input LOW Current	0.50		μA	−55°C to +125°C	V _{EE} = −4.2V V _{IN} = V _{IL (Min)}		(Notes 3, 4, 5)
I _{IH}	Input HIGH Current					V _{EE} = −5.7V V _{IN} = V _{IH (Max)}		(Notes 3, 4, 5)
	Data Enable		350	μA	0°C to +125°C			
	Data Enable		240					
			500	μA	−55°C			
			340					
I _{EE}	Power Supply Current	−65	−20	mA	−55°C to +125°C	Inputs Open		(Notes 3, 4, 5)

Note 3: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 4: Screen tested 100% on each device at -55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 5: Sample tested (Method 5005, Table I) on each manufactured lot at -55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 6: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Recommended Operating Conditions

Case Temperature (T_C)

Military -55°C to +125°C

Supply Voltage (V_{EE})

-5.7V to -4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH}	Propagation Delay	0.30	2.00	0.30	1.80	0.30	2.30	ns	Figures 1, 2	(Notes 7, 8, 10, 11)
t_{PHL}	Data to Output									
t_{PLH}	Propagation Delay	0.50	2.40	0.60	2.30	0.60	2.70	ns		
t_{PHL}	Enable to Output									
t_{TLH}	Transition Time	0.30	2.00	0.30	1.90	0.30	2.00	ns		(Note 10)
t_{THL}	20% to 80%, 80% to 20%									

Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

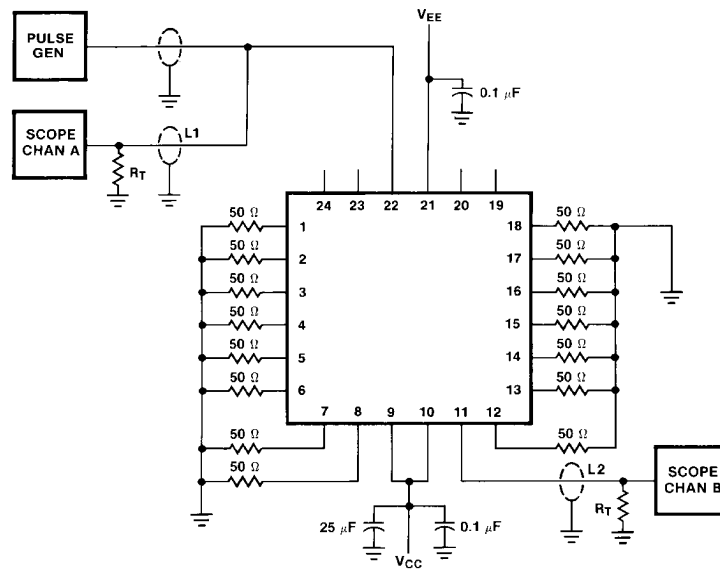
Note 8: Screen tested 100% on each device at $+25^\circ C$, Subgroup A9.

Note 9: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 10: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Note 11: The propagation delay specified is for single output switching. Delays may vary up to 150 ps with multiple outputs switching.

Test Circuitry



DS100297-5

Notes:

V_{CC} , $V_{CCA} = +2V$, $V_{EE} = -2.5V$.

L1 and L2 = equal length 50Ω impedance lines.

$R_T = 50\Omega$ terminator internal to scope.

Decoupling 0.1 μF from GND to V_{CC} and V_{EE} .

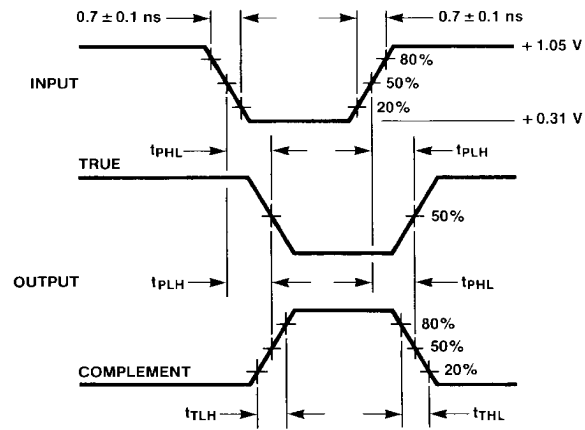
All unused outputs are loaded with 50Ω to GND.

C_L = Fixture and stray capacitance ≤ 3 pF.

Pin numbers shown are for flatpak; for DIP see logic symbol.

FIGURE 1. AC Test Circuit

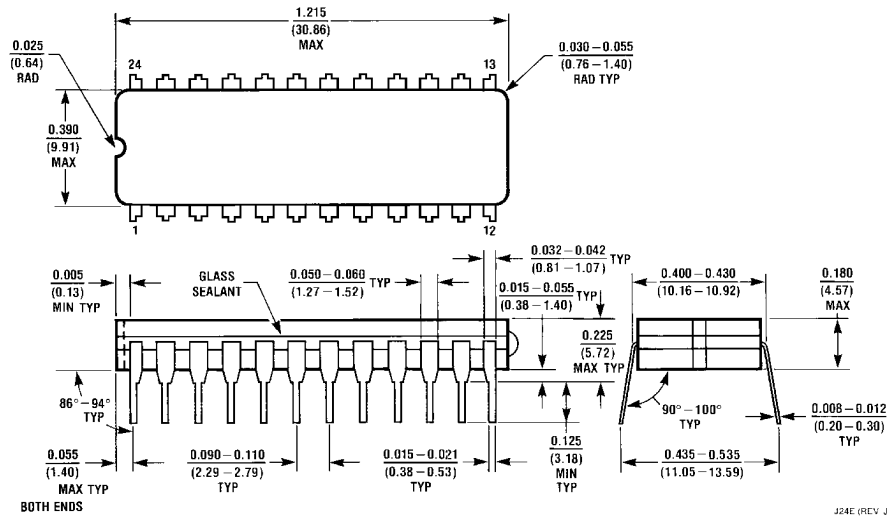
Switching Waveforms



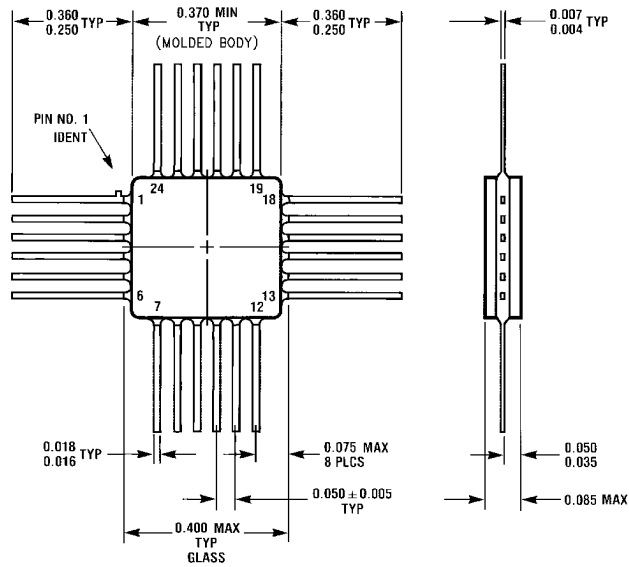
DS100297-6

FIGURE 2. Propagation Delay and Transition Times

Physical Dimensions inches (millimeters) unless otherwise noted



24-Pin Ceramic Dual-In-Line Package (D)
NS Package Number J24E



24-Pin Quad Cerpak (F)
NS Package Number W24B