



32Mx64bits PC133 SDRAM SO DIMM

based on 32Mx8 SDRAM with LVTTL, 4 banks & 8K Refresh

HYM72V32M636T8 Series

DESCRIPTION

The HYM72V32M636T8 Series are 32Mx64bits Synchronous DRAM Modules. The modules are composed of eight 32Mx8bits CMOS Synchronous DRAMs in 400mil 54pin TSOP-II package, one 2Kbit EEPROM in 8pin TSSOP package on a 144pin glass-epoxy printed circuit board. One 0.22uF and one 0.0022uF decoupling capacitors per each SDRAM are mounted on the PCB.

The HYM72V32M636T8 Series are Dual In-line Memory Modules suitable for easy interchange and addition of 256Mbytes memory. The HYM72V32M636T8 Series are fully synchronous operation referenced to the positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth.

FEATURES

- PC133/PC100MHz support
- 144pin SDRAM SO DIMM
- Serial Presence Detect with EEPROM
- 1.155" (29.34mm) Height PCB with single sided components
- Single 3.3±0.3V power supply
- All device pins are compatible with LVTTL interface
- Data mask function by DQM
- SDRAM internal banks : four banks
- Module bank : one physical bank
- Auto refresh and self refresh
- 8192 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
 - 1, 2, 4 or 8 or Full page for Sequential Burst
 - 1, 2, 4 or 8 for Interleave Burst
- Programmable $\overline{\text{CAS}}$ Latency ; 2, 3 Clocks

ORDERING INFORMATION

Part No.	Clock Frequency	Internal Bank	Ref.	Power	SDRAM Package	Plating
HYM72V32M636T8-H	133MHz	4 Banks	8K	Normal	TSOP-II	Gold
HYM72V32M636T8-H	133MHz			Low Power		

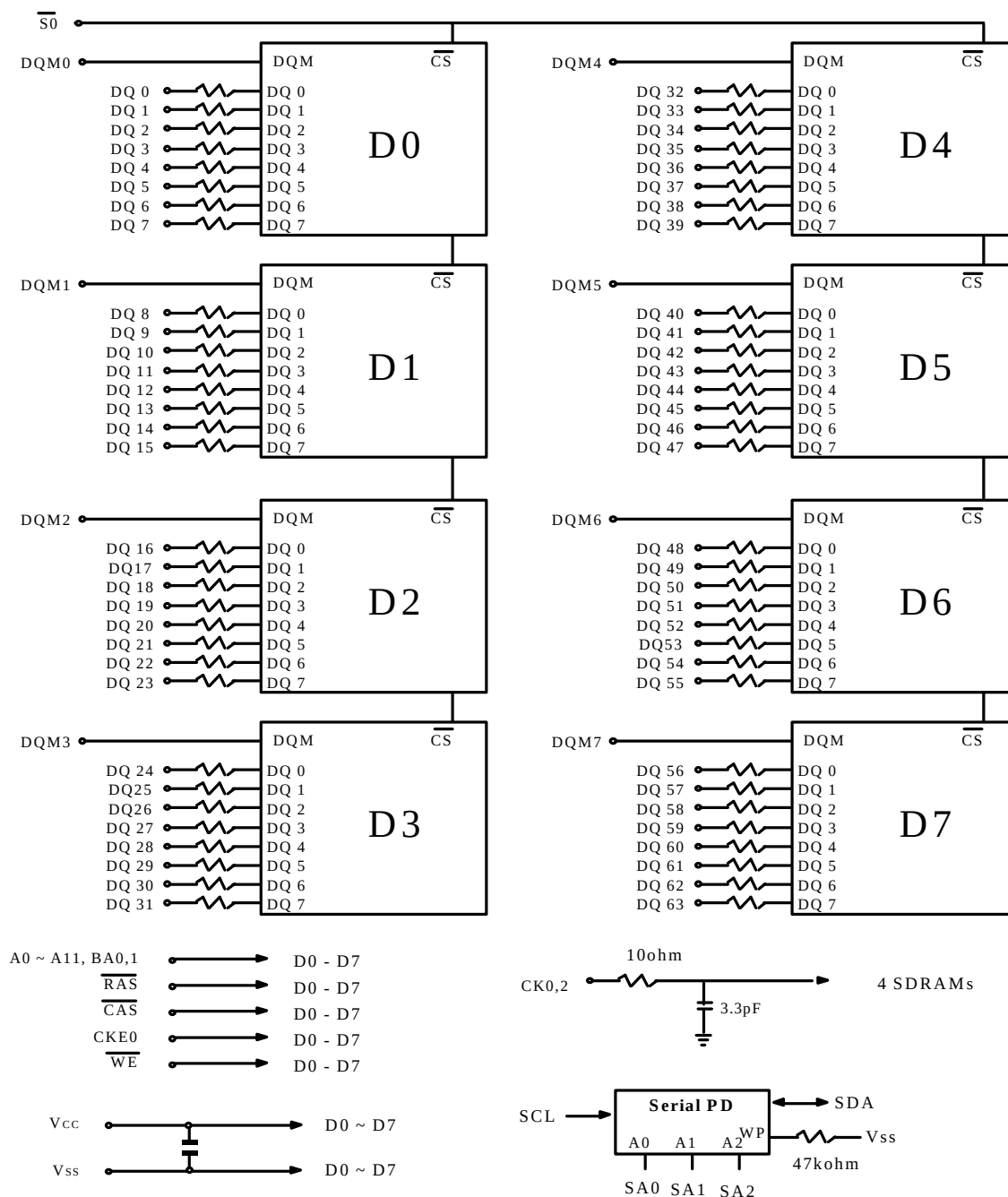
PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CK0, CK1	Clock Inputs	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
CKE0	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
/S0, /S1	Chip Select	Enables or disables all inputs except CK, CKE and DQM
BA0, BA1	SDRAM Bank Address	Selects bank to be activated during /RAS activity Selects bank to be read/written during /CAS activity
A0 ~ A12	Address	Row Address : RA0 ~ RA12, Column Address : CA0 ~ CA9 Auto-precharge flag : A10
/RAS, /CAS, /WE	Row Address Strobe, Column Address Strobe, Write Enable	/RAS, /CAS and /WE define the operation Refer function truth table for details
DQM0~DQM7	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ63	Data Input/Output	Multiplexed data input / output pin
VCC	Power Supply (3.3V)	Power supply for internal circuits and input buffers
VSS	Ground	Ground
SCL	SPD Clock Input	Serial Presence Detect Clock input
SDA	SPD Data Input/Output	Serial Presence Detect Data input/output
SA0~2	SPD Address Input	Serial Presence Detect Address Input
NC	No Connection	No connection

PIN ASSIGNMENTS

FRONT SIDE		BACK SIDE		FRONT SIDE		BACK SIDE	
PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	VSS	2	VSS	71	S1	72	NC
3	DQ0	4	DQ32	73	NC	74	CK1
5	DQ1	6	DQ33	75	VSS	76	VSS
7	DQ2	8	DQ34	77	NC	78	NC
9	DQ3	10	DQ35	79	NC	80	NC
11	VCC	12	VCC	81	VCC	82	VCC
13	DQ4	14	DQ36	83	DQ16	84	DQ48
15	DQ5	16	DQ37	85	DQ17	86	DQ49
17	DQ6	18	DQ38	87	DQ18	88	DQ50
19	DQ7	20	DQ39	89	DQ19	90	DQ51
21	VSS	22	VSS	91	VSS	92	VSS
23	DQM0	24	DQM4	93	DQ20	94	DQ52
25	DQM1	26	DQM5	95	DQ21	96	DQ53
27	VCC	28	VCC	97	DQ22	98	DQ54
29	A0	30	A3	99	DQ23	100	DQ55
31	A1	32	A4	101	VCC	102	VCC
33	A2	34	A5	103	A6	104	A7
35	VSS	36	VSS	105	A8	106	BA0
37	DQ8	38	DQ40	107	VSS	108	VSS
39	DQ9	40	DQ41	109	A9	110	BA1
41	DQ10	42	DQ42	111	A10/AP	112	A11
43	DQ11	44	DQ43	113	VCC	114	VCC
45	VCC	46	VCC	115	DQM2	116	DQM6
47	DQ12	48	DQ44	117	DQM3	118	DQM7
49	DQ13	50	DQ45	119	VSS	120	VSS
51	DQ14	52	DQ46	121	DQ24	122	DQ56
53	DQ15	54	DQ47	123	DQ25	124	DQ57
55	VSS	56	VSS	125	DQ26	126	DQ58
57	NC	58	NC	127	DQ27	128	DQ59
59	NC	60	NC	129	VCC	130	VCC
Voltage Key				131	DQ28	132	DQ60
				133	DQ29	134	DQ61
61	CK0	62	CKE0	135	DQ30	136	DQ62
63	VCC	64	VCC	137	DQ31	138	DQ63
65	/RAS	66	/CAS	139	VSS	140	VSS
67	/WE	68	NC	141	SDA	142	SCL
69	/S0	70	A12	143	VCC	144	VCC

BLOCK DIAGRAM



Note : 1. The serial resistor values of DQs are 10ohms
2. The padding capacitance of termination R/C for CK1,CK3 is 10pF

SERIAL PRESENCE DETECT

BYTE NUMBER	FUNCTION DESCRIPTION	FUNCTION	VALUE	NOTE
		-H	-H	
BYTE0	# of Bytes Written into Serial Memory at Module Manufacturer	128 Bytes	80h	
BYTE1	Total # of Bytes of SPD Memory Device	256 Bytes	08h	
BYTE2	Fundamental Memory Type	SDRAM	04h	
BYTE3	# of Row Addresses on This Assembly	13	0Dh	1
BYTE4	# of Column Addresses on This Assembly	9	09h	
BYTE5	# of Module Banks on This Assembly	1 Bank	01h	
BYTE6	Data Width of This Assembly	64 Bits	40h	
BYTE7	Data Width of This Assembly (Continued)	-	00h	
BYTE8	Voltage Interface Standard of This Assembly	LVTTL	01h	
BYTE9	SDRAM Cycle Time @/CAS Latency=3	7.5ns	75h	
BYTE10	Access Time from Clock @/CAS Latency=3	5.4ns	54h	
BYTE11	DIMM Configuration Type	None	00h	
BYTE12	Refresh Rate/Type	7.8125us / Self Refresh Supported	82h	
BYTE13	Primary SDRAM Width	x16	10h	
BYTE14	Error Checking SDRAM Width	None	00h	
BYTE15	Minimum Clock Delay Back to Back Random Column Address	tCCD = 1 CLK	01h	
BYTE16	Burst Length Supported	1,2,4,8,Full Page	8Fh	2
BYTE17	# of Banks on Each SDRAM Device	4 Banks	04h	
BYTE18	SDRAM Device Attributes, /CAS Latency	/CAS Latency=2,3	06h	
BYTE19	SDRAM Device Attributes, /CS Latency	/CS Latency=0	01h	
BYTE20	SDRAM Device Attributes, /WE Latency	/WE Latency=0	01h	
BYTE21	SDRAM Module Attributes	Neither Buffered nor Registered	00h	
BYTE22	SDRAM Device Attributes, General	+/- 10% voltage tolerance, Burst Read Single Bit Write, Precharge All, Auto Precharge, Early RAS Precharge	0Eh	
BYTE23	SDRAM Cycle Time @/CAS Latency=2	-	00h	
BYTE24	Access Time from Clock @/CAS Latency=2	-	00h	
BYTE25	SDRAM Cycle Time @/CAS Latency=1	-	00h	
BYTE26	Access Time from Clock @/CAS Latency=1	-	00h	
BYTE27	Minimum Row Precharge Time (tRP)	20ns	14h	
BYTE28	Minimum Row Active to Row Active Delay (tRRD)	15ns	0Fh	
BYTE29	Minimum /RAS to /CAS Delay (tRCD)	20ns	14h	
BYTE30	Minimum /RAS Pulse Width (tRAS)	45ns	2Dh	
BYTE31	Module Bank Density	256MB	40h	
BYTE32	Command and Address Signal Input Setup Time	1.5ns	15h	
BYTE33	Command and Address Signal Input Hold Time	0.8ns	08h	
BYTE34	Data Signal Input Setup Time	1.5ns	15h	
BYTE35	Data Signal Input Hold Time	0.8ns	08h	
BYTE36 ~61	Superset Information (may be used in future)	-	00h	
BYTE62	SPD Revision	Intel SPD 1.2B	12h	3, 8
BYTE63	Checksum for Byte 0~62	-	BAh	
BYTE64	Manufacturer JEDEC ID Code	Hynix JEDEC ID	ADh	
BYTE65 ~71	Manufacturer JEDEC ID Code	Unused	FFh	
BYTE72	Manufacturing Location	Hynix (Korea Area) HSA (United States Area) HSE (Europe Area) HSJ (Japan Area) ASIA Area	0*h 1*h 2*h 3*h 4*h	10

BYTE NUMBER	FUNCTION DESCRIPTION	FUNCTION	VALUE	NOTE
		-H	-H	
BYTE73	Manufacturer's Part Number (Component)	7 (SDRAM)	37h	4, 5
BYTE74	Manufacturer's Part Number (128Mb based)	2	32h	4, 5
BYTE75	Manufacturer's Part Number (Voltage Interface)	V (3.3V, LVTTTL)	56h	4, 5
BYTE76	Manufacturer's Part Number (Memory Width)	3	33h	4, 5
BYTE77	Manufacturer's Part Number (Memory Width)	2	32h	4, 5
BYTE78	Manufacturer's Part Number (Module Type)	M (SO DIMM)	4Dh	4, 5
BYTE79	Manufacturer's Part Number (Data Width)	6	36h	4, 5
BYTE80	Manufacturer's Part Number (Data Width)	3	33h	4, 5
BYTE81	Manufacturer's Part Number (Refresh, SDRAM Bank)	6 (8K Refresh, 4Banks)	36h	4, 5
BYTE82	Manufacturer's Part Number (Package Type)	T	54h	4, 5
BYTE83	Manufacturer's Part Number (Component Configuration)	8 (x8 based)	38h	4, 5
BYTE84	Manufacturer's Part Number (Hyphen)	- (Hyphen)	2Dh	4, 5
BYTE85	Manufacturer's Part Number (Min. Cycle Time)	H	48h	4, 5
BYTE86 ~90	Manufacturer's Part Number	Blanks	20h	4, 5
BYTE91	Revision Code (for Component)	Process Code	-	4, 6
BYTE92	Revision Code (for PCB)	Process Code	-	4, 6
BYTE93	Manufacturing Date	Work Week	-	3, 6
BYTE94	Manufacturing Date	Year	-	3, 6
BYTE95 ~98	Assembly Serial Number	Serial Number	-	6
BYTE99 ~125	Manufacturer Specific Data (may be used in future)	None	00h	
BYTE126	Reserved	Refer to Note9	64h	7, 8, 9
BYTE127	Intel Specification Details for 100MHz Support	Refer to Note7	A5h	7, 8, 9
BYTE128 ~256	Unused Storage Locations	-	00h	

Note :

1. The bank address is excluded
2. 1, 2, 4, 8 for Interleave Burst Type
3. BCD adopted
4. ASCII adopted
5. Basically Hynix writes Part No. except for HYM'in Byte 73~90 to use the limited 18 bytes from byte 73 to byte 90
6. Not fixed but dependent
7. CK0, CK1 connected to DIMM, TBD junction temp, CL2(3) support, Intel defined Concurrent Auto Precharge support
8. Refer to the most recent Intel and JEDEC SPD Specification
9. These values are applied to PC100 applications only per Intel PC SDRAM specification
10. Refer to Hynix Web site.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	1	W
Soldering Temperature - Time	TSOLDER	260 · 10	°C · Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability.

DC OPERATING CONDITION (TA=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	VDD, VDDQ	3.0	3.3	3.6	V	1
Input High voltage	VIH	2.0	3.0	VDDQ + 0.3	V	1,2
Input Low voltage	VIL	-0.3	0	0.8	V	1,3

Note :

- 1.All voltages are referenced to VSS = 0V
- 2.VIH(max) is acceptable 5.6V AC pulse width with <=3ns of duration.
- 3.VIL(min) is acceptable -2.0V AC pulse width with <=3ns of duration.

AC OPERATING TEST CONDITION (TA=0 to 70°C, VDD=3.3±0.3V, VSS=0V)

Parameter	Symbol	Value	Unit	Note
AC Input High / Low Level Voltage	VIH / VIL	2.4/0.4	V	
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V	
Input Rise / Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level Voltage	Voutref	1.4	V	
Output Load Capacitance for Access Time Measurement	CL	50	pF	1

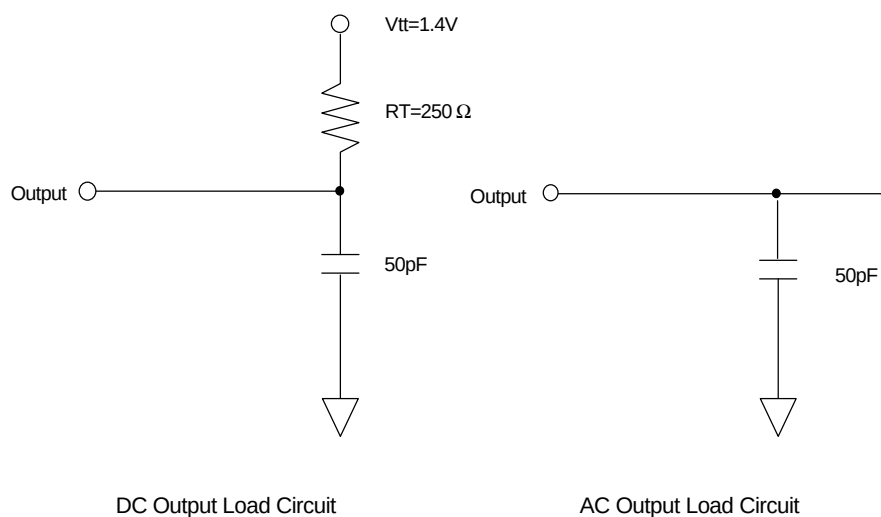
Note :

- 1.Output load to measure access times is equivalent to two TTL gates and one capacitor (50pF). For details, refer to AC/DC output load circuit

CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Pin	Symbol	-K		Unit
			Min	Max	
Input Capacitance	CK0, CK2	CI1	25	45	pF
	CKE0	CI2	35	55	pF
	/S0, /S2	CI3	25	40	pF
	A0~11, BA0, BA1	CI4	40	60	pF
	/RAS, /CAS, /WE	CI5	40	60	pF
	DQM0~DQM7	CI6	5	15	pF
Data Input / Output Capacitance	DQ0 ~ DQ63	CI/O	5	15	pF

OUTPUT LOAD CIRCUIT



DC CHARACTERISTICS I (TA=0 to 70°C, VDD=3.3±0.3V)

Parameter	Symbol	Min.	Max	Unit	Note
Input Leakage Current	ILI	-8	8	uA	1
Output Leakage Current	ILO	-1	1	uA	2
Output High Voltage	VOH	2.4	-	V	IOH = -4mA
Output Low Voltage	VOL	-	0.4	V	IOL = +4mA

Note :

1. VIN = 0 to 3.6V, All other pins are not tested under VIN = 0V
2. DOUT is disabled, VOUT=0 to 3.6

DC CHARACTERISTICS II

Parameter	Symbol	Test Condition	Speed	Unit	Note
			-H		
Operating Current	IDD1	Burst length=1, One bank active tRC ≥ tRC(min), IOL=0mA	600	mA	1
Precharge Standby Current in Power Down Mode	IDD2P	CKE ≤ VIL(max), tCK = min	16	mA	
	IDD2PS	CKE ≤ VIL(max), tCK = ∞	16		
Precharge Standby Current in Non Power Down Mode	IDD2N	CKE ≥ VIH(min), $\overline{CS} \geq \overline{VIH}(\min)$, tCK = min Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V	160	mA	
	IDD2NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.	80		
Active Standby Current in Power Down Mode	IDD3P	CKE ≤ VIL(max), tCK = min	56	mA	
	IDD3PS	CKE ≤ VIL(max), tCK = ∞	56		
Active Standby Current in Non Power Down Mode	IDD3N	CKE ≥ VIH(min), $\overline{CS} \geq \overline{VIH}(\min)$, tCK = min Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V	320	mA	
	IDD3NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.	320		
Burst Mode Operating Current	IDD4	tCK ≥ tCK(min), IOL=0mA All banks active	800	mA	1
Auto Refresh Current	IDD5	tRRC ≥ tRRC(min), All banks active	980	mA	2
Self Refresh Current	IDD6	CKE ≤ 0.2V	24	mA	3
			12	mA	4

Note :

1. IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open
2. Min. of tRRC (Refresh RAS cycle time) is shown at AC CHARACTERISTICS II
3. HYM72V32M636T8-H
4. HYM72V32M636LT8-H

AC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

Parameter		Symbol	-H		Unit	Note
			Min	Max		
System Clock Cycle Time	CAS Latency = 3	tCK3	7.5	1000	ns	
	CAS Latency = 2	tCK2	10		ns	
Clock High Pulse Width		tCHW	2.5	-	ns	1
Clock Low Pulse Width		tCLW	2.5	-	ns	1
Access Time From Clock	CAS Latency = 3	tAC3	-	5.4	ns	2
	CAS Latency = 2	tAC2	-	6	ns	
Data-Out Hold Time		tOH	2.7	-	ns	
Data-Input Setup Time		tDS	1.5	-	ns	1
Data-Input Hold Time		tDH	0.8	-	ns	1
Address Setup Time		tAS	1.5	-	ns	1
Address Hold Time		tAH	0.8	-	ns	1
CKE Setup Time		tCKS	1.5	-	ns	1
CKE Hold Time		tCKH	0.8	-	ns	1
Command Setup Time		tCS	1.5	-	ns	1
Command Hold Time		tCH	0.8	-	ns	1
CLK to Data Output in Low-Z Time		tOLZ	1	-	ns	
CLK to Data Output in High-Z Time	CAS Latency = 3	tOHZ3	2.7	5.4	ns	
	CAS Latency = 2	tOHZ2	3	6	ns	

Note :

1. Assume t_R / t_F (input rise and fall time) is 1ns
If t_R & $t_F > 1ns$, then $[(t_R+t_F)/2-1]ns$ should be added to the parameter
2. Access times to be measured with input signals of 1v/ns edge rate, from 0.8v to 2.0v
If $t_R > 1ns$, then $(t_R/2-0.5)ns$ should be added to the parameter

AC CHARACTERISTICS II

Parameter		Symbol	-H		Unit	Note
			Min	Max		
RAS Cycle Time	Operation	tRC	65	-	ns	
	Auto Refresh	tRRC	65	-	ns	
RAS to CAS Delay		tRCD	20	-	ns	
RAS Active Time		tRAS	45	100K	ns	
RAS Precharge Time		tRP	20	-	ns	
RAS to RAS Bank Active Delay		tRRD	15	-	ns	
CAS to CAS Delay		tCCD	1	-	CLK	
Write Command to Data-In Delay		tWTL	0	-	CLK	
Data-In to Precharge Command		tDPL	2	-	CLK	
Data-In to Active Command		tDAL	5	-	CLK	
DQM to Data-Out Hi-Z		tDQZ	2	-	CLK	
DQM to Data-In Mask		tDQM	0	-	CLK	
MRS to New Command		tMRD	2	-	CLK	
Precharge to Data Output Hi-Z	CAS Latency = 3	tPROZ3	3	-	CLK	
	CAS Latency = 2	tPROZ2	2	-	CLK	
Power Down Exit Time		tPDE	1	-	CLK	
Self Refresh Exit Time		tSRE	1	-	CLK	1
Refresh Time		tREF	-	64	ms	

Note :

1. A new command can be given tRRC after self refresh exit

DEVICE OPERATING OPTION TABLE
HYM72V32M636(L)T8-H

	CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
133MHz(7.5ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.4ns	2.7ns
125MHz(8ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	3ns
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns

COMMAND TRUTH TABLE

Command	CKEn-1	CKEn	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	DQM	ADDR	A10/ AP	BA	Note
Mode Register Set	H	X	L	L	L	L	X	OP code			
No Operation	H	X	H	X	X	X	X	X			
			L	H	H	H					
Bank Active	H	X	L	L	H	H	X	RA		V	
Read	H	X	L	H	L	H	X	CA	L	V	
Read with Autoprecharge									H		
Write	H	X	L	H	L	L	X	CA	L	V	
Write with Autoprecharge									H		
Precharge All Banks	H	X	L	L	H	L	X	X	H	X	
Precharge selected Bank									L	V	
Burst Stop	H	X	L	H	H	L	X	X			
DQM	H	X					V	X			
Auto Refresh	H	H	L	L	L	H	X	X			
Burst-Read-Single-WRITE	H	X	L	L	L	H	X	A9 Pin High (Other Pins OP code)			
Self Refresh ¹	Entry	H	L	L	L	L	H	X	X		
	Exit	L	H	H	X	X	X				
Precharge power down	Entry	H	L	H	X	X	X	X	X		
				L	H	H	H				
	Exit	L	H	H	X	X	X				
				L	H	H	H				
Clock Suspend	Entry	H	L	H	X	X	X	X	X		
				L	V	V	V				
	Exit	L	H	X			X				

Note :

1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high
2. X = Don't care, H = Logic High, L = Logic Low. BA = Bank Address, RA = Row Address, CA = Column Address,

PACKAGE DEMENSION

