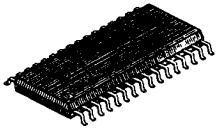
SONY CXK59290M/TM -70L/10L/12L

32768-word × 9-bit High Speed CMOS Static RAM

Description

The CXK59290M/TM is a 294912 bits high speed CMOS static RAM organized as 32768 words by 9 bits and operates from a single 5V supply. This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

CXK59290M
32 pin SOP (Plastic)



CXK59290TM
32 pin TSOP (Plastic)

Features

- Fast access time: (Access time)
  CXK59290M/TM-70L 70ns (Max.)
  CXK59290M/TM-10L 100ns (Max.)
  CXK59290M/TM-12L 120ns (Max.)
- Low power operation: Standby/Operation
  CXK59290M/TM-70L, 10L, 12L:
  2.5μW (Typ.)/15mW (Typ.)
- Single +5V supply: +5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time
- Common data input and output: three state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)
- Available in 32 pin 450mil SOP and
  32 pin 8mm × 20mm TSOP (EIAJ Standard)

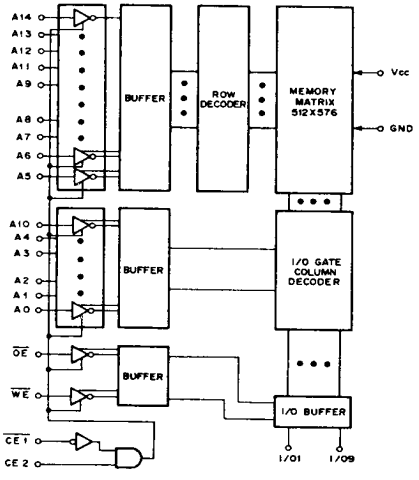
Function

32768-word × 9-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram



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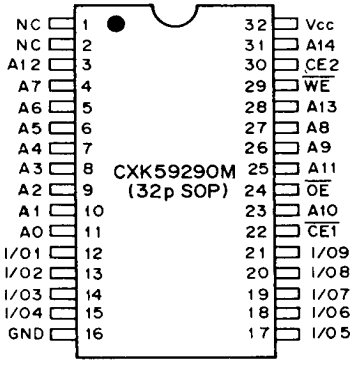
E90943A22 - ST

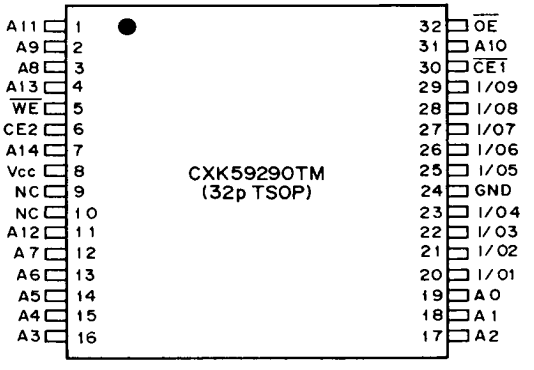
Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O9	Data input/output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

Pin Configuration

(Top View)





Absolute Maximum Ratings (Ta=25℃, GND=0V)

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		−0.5 to +7.0	V
Input voltage	V_{IN}		−0.5 * to Vcc+0.5	V
Input and output voltage	$V_{I/O}$		−0.5 * to Vcc+0.5	V
Allowable power dissipation	P_D		0.7	W
Operating temperature	Topr		0 to +70	℃
Storage temperature	Tstg		−55 to +150	℃
Soldering temperature	Tsolder	M	260 • 10	℃ • sec
		TM	235 • 10	

* V_{IN}, $V_{I/O}$=−3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O9	Vcc Current
H	×	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	H	×	L	Write	Data in	I_{CC1}, I_{CC2}

× : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70℃, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	Vcc+0.3	V
Input low voltage	V_{IL}	−0.3 *	—	0.8	V

* V_{IL}=−3.0V Min. for pulse width less than 50ns.

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Electrical Characteristics

• DC and operating characteristics

(Vcc=5V ± 10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test conditions		Min.	Typ. *	Max.	Unit
Input leakage current	I_{LI}	V_{IN}=GND to Vcc		–0.5	—	0.5	µA
Output leakage current	I_{LO}	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=GND to Vcc		–0.5	—	0.5	µA
Operating power supply current	I_{CC1}	$\overline{CE1}$=V_{IL}, CE2=V_{IH}, I_{OUT}=0mA V_{IN}=V_{IH} or V_{IL}		—	25	50	mA
		$\overline{CE1}$ ≦ 0.2V, CE2 ≧ Vcc–0.2V V_{IN} ≦ 0.2V or ≧ Vcc–0.2V		—	23	45	mA
Average operating current	I_{CC2}	Min. cycle Duty=100% I_{OUT}=0mA	70L	—	—	70	mA
			10L	—	—	70	
			12L	—	—	70	
Standby current	I_{SB1}	CE2 ≦ 0.2V or $\overline{CE1}$ ≧ Vcc–0.2V CE2 ≧ Vcc–0.2V	0 to +70°C	—	—	25	µA
			0 to +40°C	—	—	5	
			25°C	—	0.5	2	
	I_{SB2}	$\overline{CE1}$=V_{IH} or CE2=V_{IL}		—	0.4	2	mA
Output high voltage	V_{OH}	I_{OH}=–1.0mA		2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	V

* Vcc=5V, Ta=25°C

I/O capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	8	pF

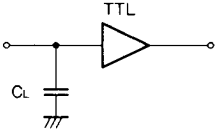
Note) This parameter is sampled and is not 100% tested.

AC characteristics

• AC test conditions (Vcc=5V ± 10%, Ta=0 to +70°C)

Item		Conditions
Input pulse high level		V_{IH}=2.2V
Input pulse low level		V_{IL}=0.8V
Input rise time		tr=5ns
Input fall time		tf=5ns
Input and output reference level		1.5V
Output load conditions	10L/12L	C_L * =100pF, 1TTL
	70L	C_L * =30pF, 1TTL

* C_L includes scope and jig capacitances.



• Read cycle

Item	Symbol	-70L		-10L		-12L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	70	—	100	—	120	—	ns
Address access time	t_{AA}	—	70	—	100	—	120	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	70	—	100	—	120	ns
Chip enable access time (CE2)	t_{CO2}	—	70	—	100	—	120	ns
Output enable to output valid	t_{OE}	—	35	—	50	—	60	ns
Output hold from address change	t_{OH}	5	—	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}, t_{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}, t_{HZ2} *	0	30	0	30	0	30	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ} *	0	30	0	30	0	30	ns

* t_{HZ} and t_{OHZ} are defined as the time at which the outputs become the high impedance state and are not referred to as output voltage levels.

• Write cycle

Item	Symbol	-70L		-10L		-12L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	70	—	100	—	120	—	ns
Address valid to end of write	t_{AW}	65	—	80	—	100	—	ns
Chip enable to end of write	t_{CW}	65	—	80	—	100	—	ns
Data to write time overlap	t_{DW}	30	—	35	—	40	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	50	—	60	—	70	—	ns
Address set up time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ} *	0	25	0	25	0	25	ns

* t_{WHZ} is defined as the time at which the outputs become the high impedance state and are not referred to as output voltage levels.

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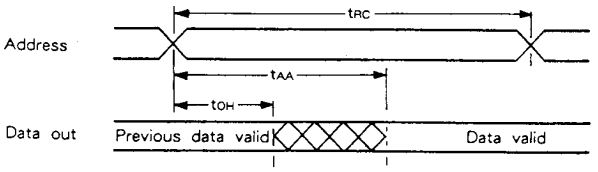
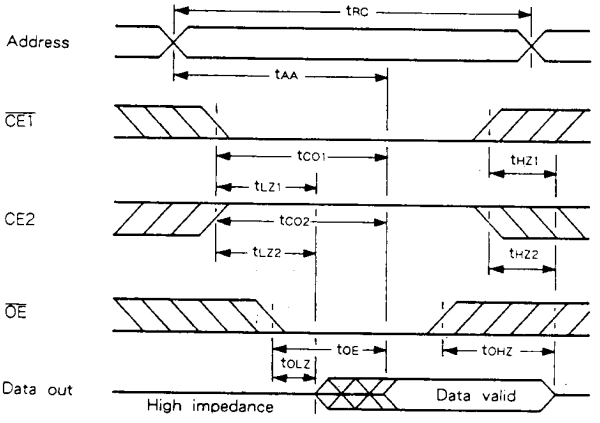
Timing Waveform

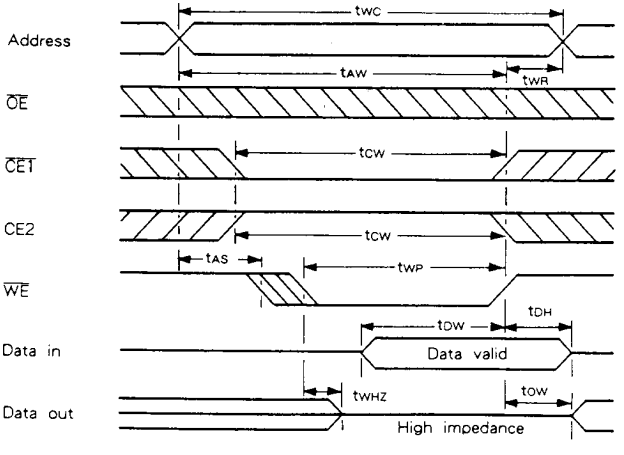
• Read cycle (1) : $\overline{CE1}$=$\overline{OE}$=V_{IL}, CE2=V_{IH}, $\overline{WE}$=V_{IH}



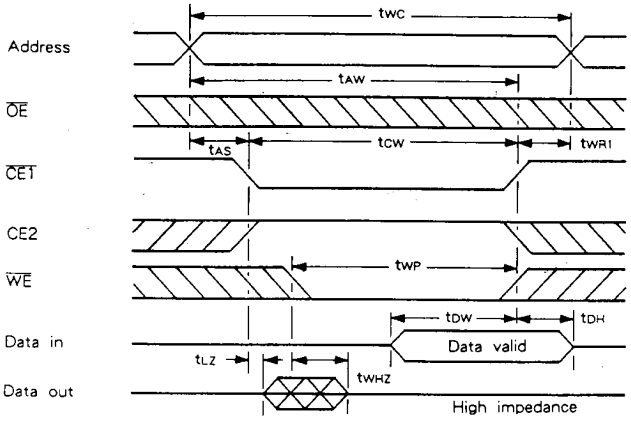
• Read cycle (2) : $\overline{WE}$=V_{IH}



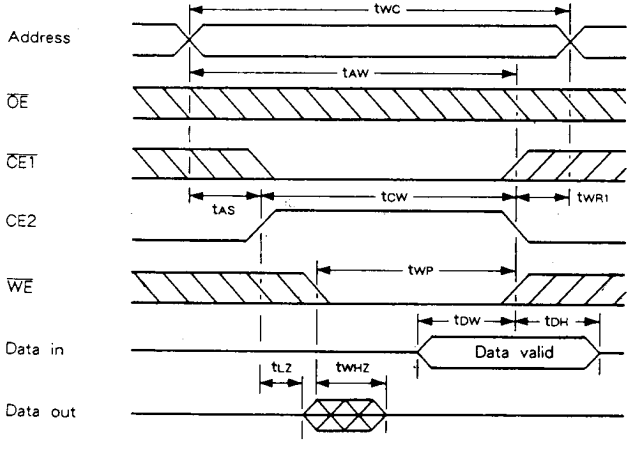
• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



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* During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

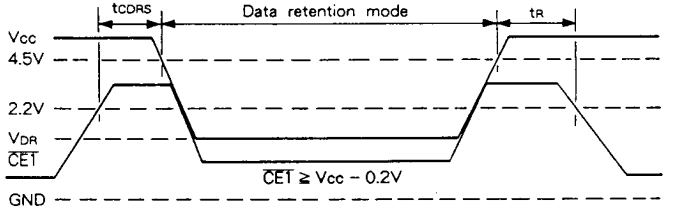
Data Retention Characteristics

(Ta=0 to +70°C)

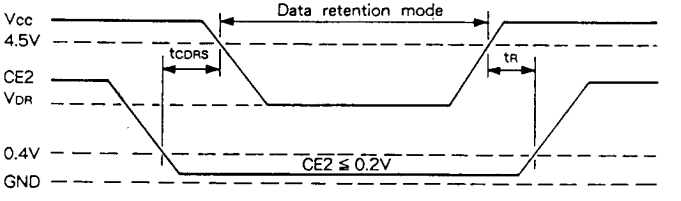
Item	Symbol	Test conditions		Min.	Typ.	Max.	Unit
Data retention voltage	V_{DR}	*1		2.0	—	5.5	V
Data retention current	I_{CCDR1}	Vcc=3.0V *1	0 to +70°C	—	—	10	μA
			0 to +40°C	—	—	2	
			25°C	—	0.25	1	
	I_{CCDR2}	Vcc=2.0 to 5.5V *1		—	0.5 *3	25	μA
Data retention setup time	t_{CDRS}	Chip disable to data retention		0	—	—	ns
Recovery time	t_R	mode		t_{RC} *2	—	—	ns

*1. $\overline{CE1} \geqq$ Vcc−0.2V, CE2 ≧ Vcc−0.2V ($\overline{CE1}$ control) or CE2 ≦ 0.2V (CE2 control)
*2. t_{RC} : Read cycle time
*3. Vcc=5V, Ta=25°C

• Low supply voltage data retention waveform (1) : $\overline{CE1}$ control

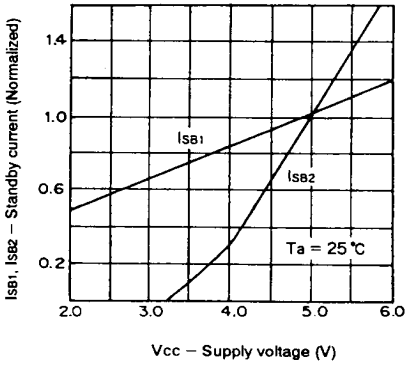


• Low supply voltage data retention waveform (2) : CE2 control

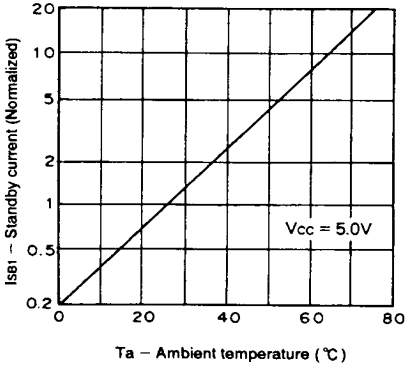


Example of Representative Characteristics

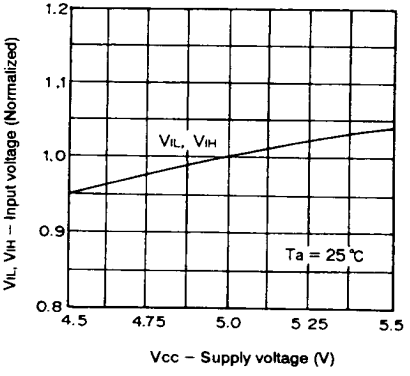
Standby current vs. Supply voltage



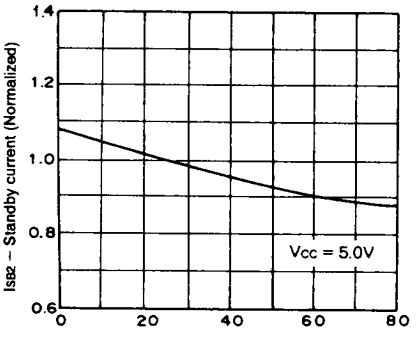
Standby current vs. Ambient temperature



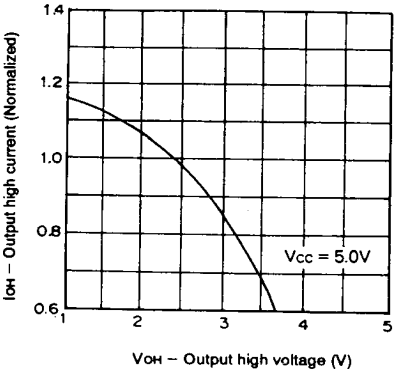
Input voltage level vs. Supply voltage



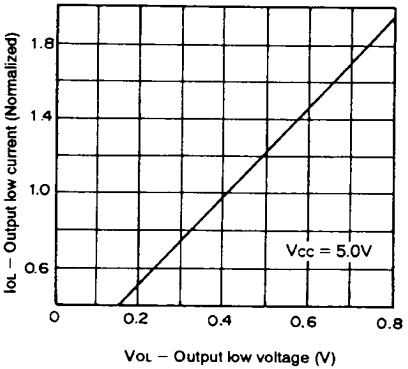
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



Output low current vs. Output low voltage



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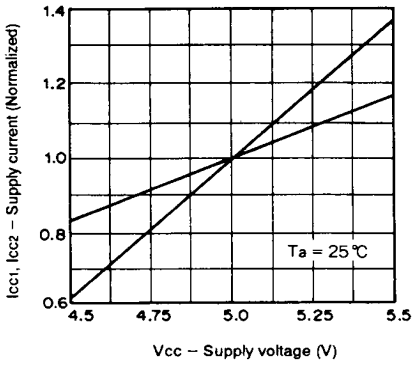
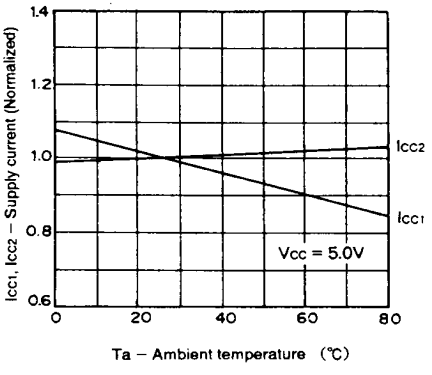
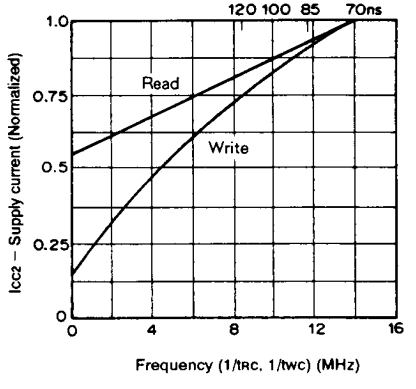
Supply current vs. Supply voltage



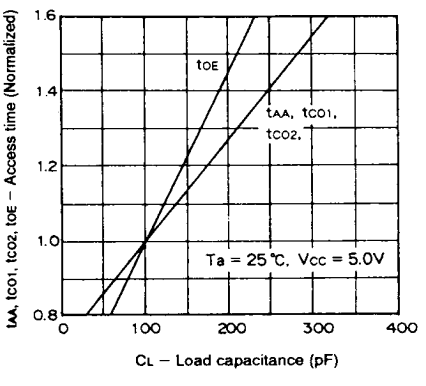
Supply current vs. Ambient temperature



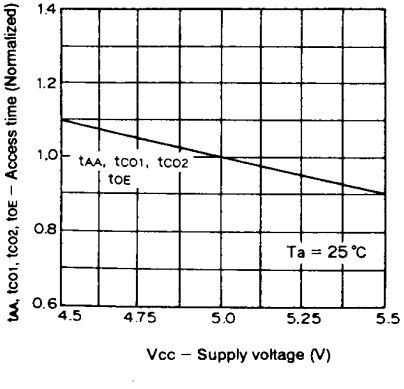
Supply current vs. Frequency



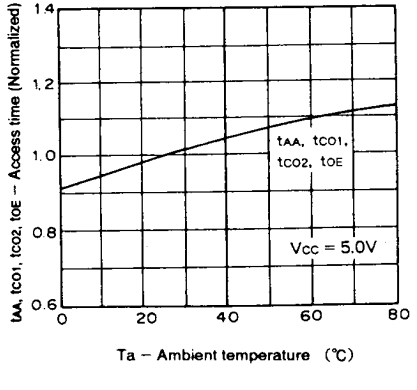
Access time vs. Load capacitance



Access time vs. Supply voltage



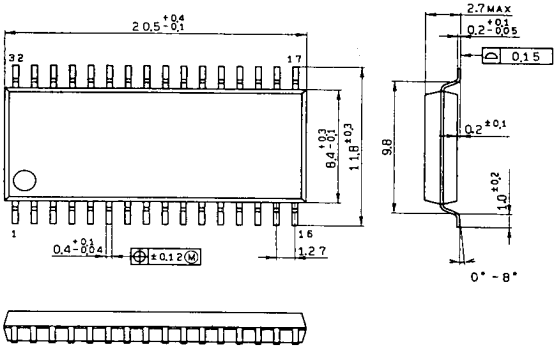
Access time vs. Ambient temperature



Package Outline Unit : mm

CXK59290M

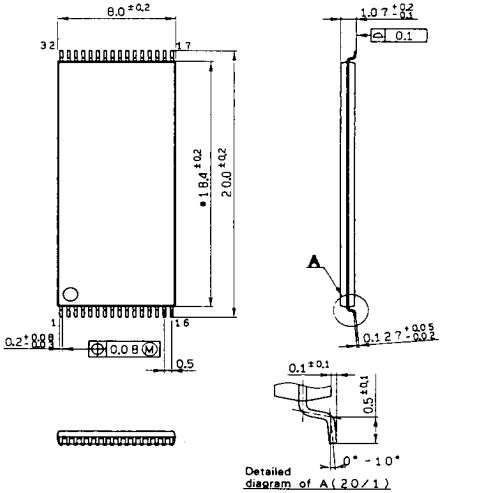
32pin SOP (Plastic) 450mil



SONY NAME	SOP-32P-L03
EIAJ NAME	*SOP032-P-0450-B
JEDEC CODE	———

CXK59290TM

32pin TSOP (Plastic)



Detailed diagram of A(20/1)

Note) Dimensions marked with * does not include resin residue.

SONY NAME	TSOP-32P-L01
EIAJ NAME	TSOP032-P-0820-A
JEDEC CODE	———

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