

CD54/74HC182

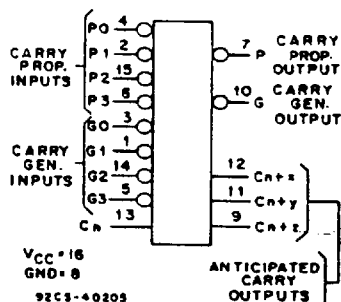
CD54/74HCT182



High-Speed CMOS Logic

December 1997

NOT RECOMMENDED FOR NEW DESIGNS



FUNCTIONAL DIAGRAM

The Harris CD54/74HC182 and CD54/74HCT182 carry look-ahead generators are high-speed silicon-gate CMOS devices and are pin compatible with low-power Schottky TTL (LSTTL).

The CD54/74HC/HCT182 accept up to four pairs of active LOW carry propagate ($\overline{P}_0, \overline{P}_1, \overline{P}_2, \overline{P}_3$) and carry generate ($\overline{G}_0, \overline{G}_1, \overline{G}_2, \overline{G}_3$) signals and an active HIGH carry input (C_n). The devices provide anticipated active HIGH carries ($C_{n+x}, C_{n+y}, C_{n+z}$) across four groups of binary adders. The HC/HCT182 also has active LOW carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs which may be used for further levels of look ahead.

The logic equations provided at the outputs are:

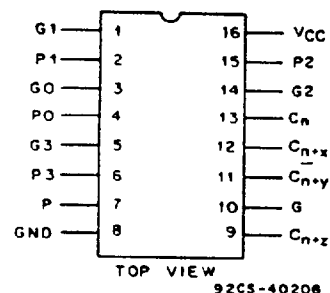
$$\begin{aligned} C_{n+x} &= P_0 C_n + G_0 \\ C_{n+y} &= G_1 + P_1 G_0 + P_1 P_0 C_n \\ C_{n+z} &= G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n \\ \overline{G} &= \overline{G}_3 + P_3 \overline{G}_2 + P_3 P_2 \overline{G}_1 + P_3 P_2 P_1 \overline{G}_0 \\ \overline{P} &= \overline{P}_3 P_2 P_1 P_0 \end{aligned}$$

The CD54/74HC/HCT182 can also be used with binary ALUs in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry look-ahead generator are identical in both cases.

The CD54HC182 and CD54HCT182 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC182 and CD74HCT182 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- Fanout (over temperature range):
Standard outputs - 10 LSTTL loads
Bus driver outputs - 15 LSTTL loads
- Wide operating temperature range:
-55 to +125°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- Alternate source is Philips/Signetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High noise immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} ,
@ $V_{CC} = 5$ V
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL input logic compatibility
 $V_{IL} = 0.8$ V max., $V_{IH} = 2$ V Min.
CMOS input compatibility
 $I_i \leq 1 \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

File Number 1830.1

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CD54/74HCT182

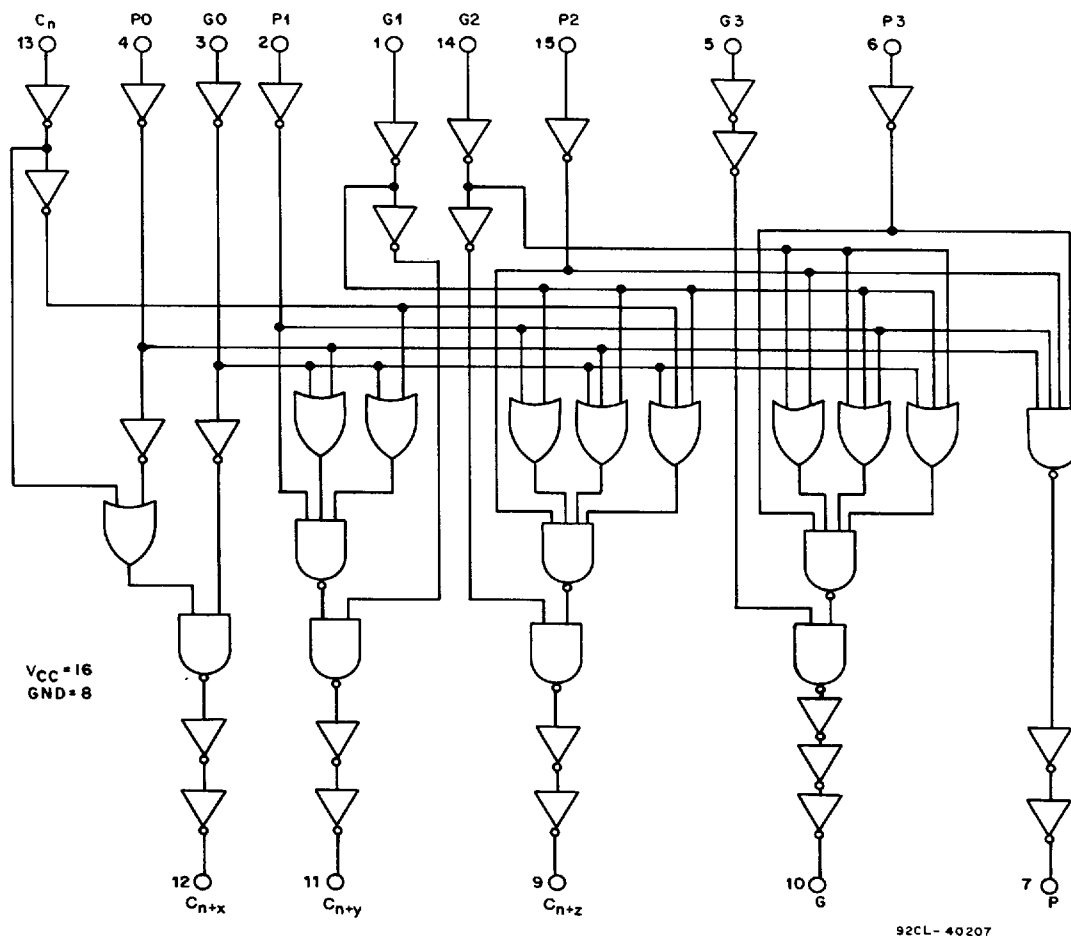


Fig. 1 - Logic diagram.

MAXIMUM RATINGS, Absolute-Maximum Values:**DC SUPPLY-VOLTAGE, (V_{CC}):**

(Voltages referenced to ground) -0.5 to +7 V

DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V) ± 20 mADC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V) ± 20 mADC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} + 0.5$ V) ± 25 mADC V_{CC} OR GROUND CURRENT (I_{CC}) ± 50 mA**POWER DISSIPATION PER PACKAGE (P_D):**For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE E, F, H) 500 mWFor $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E, F, H) Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mWFor $T_A = -55$ to $+70^\circ\text{C}$ (PACKAGE TYPE M) 400 mWFor $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M) Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW**OPERATING-TEMPERATURE RANGE (T_A):** -55 to $+125^\circ\text{C}$ **STORAGE TEMPERATURE (T_{stg}):** -65 to $+150^\circ\text{C}$ **LEAD TEMPERATURE (DURING SOLDERING):**At case distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max. $+265^\circ\text{C}$ Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm)
with solder contacting lead tips only $+300^\circ\text{C}$

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RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC} .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_i , V_o	0	V_{CC}	V
Operating Temperature T_A	-55	+125	°C
Input Rise and Fall Times, t_r , t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

FUNCTION TABLE

INPUTS									OUTPUTS				
C_n	G_0	P_0	G_1	P_1	G_2	P_2	G_3	P_3	C_{n+x}	C_{n+y}	C_{n+z}	G	P
X L X H	H H L X	H X X L							L L H H				
X X L X X H	X H X L X	X H X X L	H H L X X	H X X L L						L L L H H H			
X X X L X X X H	X X H H X X L X	X X H X X X X L	X H H H X L X X	X H X X L L	H H H H L X X X	H X X X L L					L L L L H H H H		
	X X X H X X X L		X X H H X X L X	X X H X X X X L	X H H H X L X X	X H X X L L	H H H H L X X X	H X X X X L L L				H H H H L L L L	
		H X X X L		X H X X L		X X H X L		X X X H L					H H H H L

H = HIGH voltage level

L = LOW voltage level

X = don't care

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		CD74HC182/CD54HC182										CD74HCT182/CD54HCT182										UNITS		
		TEST CONDITIONS			AMBIENT TEMPERATURE (T _A)								TEST CONDITIONS			AMBIENT TEMPERATURE (T _A)								
		V _I V	I _O mA	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C			V _I V	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C				
			Min	Typ	Max	Min	Max	Min	Max				Min			Typ	Max	Min	Max	Min	Max			
High-Level Input Voltage	V _{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V			
			4.5	3.15	—	—	3.15	—	3.15	—														
			6	4.2	—	—	4.2	—	4.2	—														
Low-Level Input Voltage	V _{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V			
			4.5	—	—	1.35	—	1.35	—	1.35														
			6	—	—	1.8	—	1.8	—	1.8														
High-Level Output Voltage CMOS Loads	V _{OH}	V _{IL} or V _{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V _{IL} or V _{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V			
			4.5	4.4	—	—	4.4	—	4.4	—														
			6	5.9	—	—	5.9	—	5.9	—														
TTL Loads	V _{IL} or V _{IH}										V _{IL} or V _{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V				
		-4	4.5	3.98	—	—	3.84	—	3.7	—														
		-5.2	6	5.48	—	—	5.34	—	5.2	—														
Low-Level Output Voltage CMOS Loads	V _{OL}	V _{IL} or V _{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V _{IL} or V _{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V			
			4.5	—	—	0.1	—	0.1	—	0.1														
			6	—	—	0.1	—	0.1	—	0.1														
TTL Loads	V _{IL} or V _{IH}										V _{IL} or V _{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V				
		4	4.5	—	—	0.26	—	0.33	—	0.4														
		5.2	6	—	—	0.26	—	0.33	—	0.4														
Input Leakage Current	I _I	V _{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V _{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA			
Quiescent Device Current	I _{CC}	V _{CC} or Gnd	0	6	—	—	8	—	80	—	160	V _{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA			
Additional Quiescent Device Current per Input pin: 1 unit load	ΔI _{CC} *											V _{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA			

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
P ₀ , P ₁ , P ₂ , G ₀ , G ₁	1.5
P ₃ , G ₂ , C _n	1.25
G ₃	0.3

* Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

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SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 6\text{ ns}$)

CHARACTERISTIC	C_L (pF)	TYPICAL VALUES		UNITS
		HC	HCT	
Propagation Delay Time:				
P_n to P	t_{PHL}, t_{PLH}	15	9	11
C_n to any output	t_{PHL}, t_{PLH}	15	12	17
P_n to any output	t_{PHL}, t_{PLH}	15	12	13
G_n to any output	t_{PHL}, t_{PLH}	15	11	13
Power Dissipation Capacitance *	C_{PD}	—	66	72
				pF

* C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o)$ where: f_i = input frequency

f_o = output frequency

C_L = output load capacitance

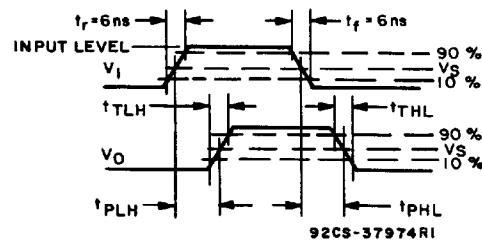
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS ($C_L = 50\text{ pF}$, Input $t_r, t_f = 6\text{ ns}$)

CHARACTERISTIC	TEST CONDITIONS V _{CC} V	AMBIENT TEMPERATURE (T _A)												UNITS
		25° C				-40° C to +85° C				-55° C to +125° C				
		HC		HCT		HC		HCT		HC		HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, t _{PLH}	2	—	120	—	—	—	150	—	—	—	180	—	—	ns
t _{PHL}	4.5	—	24	—	28	—	30	—	35	—	36	—	42	
P _n to P	6	—	20	—	—	—	26	—	—	—	31	—	—	
t _{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
t _{PHL}	4.5	—	30	—	40	—	38	—	50	—	45	—	60	
C _n to any output	6	—	26	—	—	—	33	—	—	—	38	—	—	
t _{PLH}	2	—	145	—	—	—	180	—	—	—	220	—	—	
t _{PHL}	4.5	—	29	—	33	—	36	—	41	—	36	—	50	
P _n to any output	6	—	25	—	—	—	31	—	—	—	31	—	—	
t _{PLH}	2	—	135	—	—	—	170	—	—	—	205	—	—	
t _{PHL}	4.5	—	27	—	32	—	34	—	40	—	41	—	48	
G _n to any output	6	—	23	—	—	—	29	—	—	—	35	—	—	
Transition Time	2	—	75	—	—	—	95	—	—	—	110	—	—	
t _{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C _i	—	10	—	10	—	10	—	10	—	10	—	10	pF

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	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Transition times and propagation delay times.