Features

- **Stores Voice and Data**
- **Complete Recorder with External Microphone and Speaker**
- **2-megabit of Flash Memory Directly Accessible via 2-wire Interface**
- **Automatic Message Management in Stand-alone Mode**
- **Mixed Mode Usage in CPU Mode**
- **Records to and Plays from External Memory**
- **Low-voltage and Low-power Operation:**
  - **1.8V to 3.6V**
  - **10 mA Active I_{CC} current**
  - **0.1 µA Standby I_{CC} current**

Voice Recorder IC

AT72AV020

Description

The AT72AV020 is a complete record/playback IC featuring nonvolatile storage for voice and/or data.

The chip contains all the active circuitry required for the recording and playback of voice. A microphone can be used for voice input while the on-chip power amplifier can directly drive a speaker.

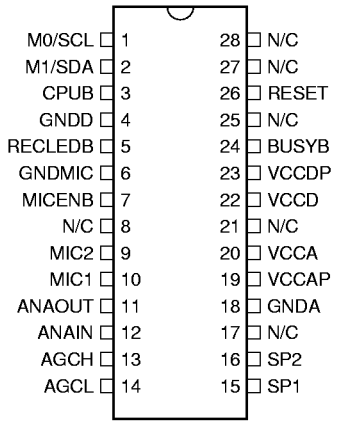
On-chip components include signal amplifiers, filters, companding DAC, power amplifier, 2-megabit of Flash memory, precision oscillator, as well as a controller which accepts commands from manual keys or via a 2-wire serial interface.

At the nominal sampling frequency of 6.4 kHz, approximately 40 seconds of voice can be stored in the on-chip nonvolatile memory.

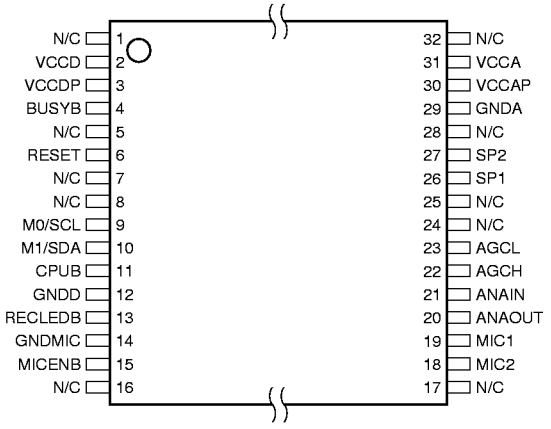
In Stand-alone Mode the key inputs, M0 and M1, combine for STANDBY, RECORD, PLAY and ERASE modes. In CPU Mode the control inputs, SCL and SDA, are used for 2-wire serial protocol commands to initiate RECORD, PLAY, ERASE or data oriented commands such as DATA WRITE and DATA READ.

In CPU Mode the device can also use external memory to extend recording time indefinitely.

DIP
Top View



TSOP Type 1
Top View



Rev. 1485A–10/99

Pin Description

M0, M1

Manual key inputs kept low by open drain pull-downs when CPUB is high. Can be pulled high with switches to V_{CC}. See "Device Operation" for detailed description.

SCL, SDA

2-wire serial-interface pins when CPUB is low. SCL is the serial clock input and SDA is the serial data I/O pin. Data is clocked in on the rising edge of clock and clocked out on the falling edge.

CPUB

Digital input used to switch between Stand-alone Mode (high) and CPU Mode (low).

GNDD

Ground pin for digital circuitry.

RECLEDB

Open-drain output which connects to GNDD during recording. Can be used to bias an LED recording indicator.

GNDMIC

Ground pin associated with MICENB.

MICENB

Open-drain output which connects to GNDMIC during recording. Can be used to bias a microphone through a dedicated ground connection.

MIC1, MIC2

Pre-amplifier inputs which should be capacitively coupled to the Microphone

ANAOUT

Multiplexed analog output; acting as pre-amplifier output during recording and as Equalizer output during playback.

ANAIN

Multiplexed analog input acting as amplifier input during recording and as power amplifier input during playback.

AGCH, AGCL

Analog I/O pins used for connecting external AGC components (i.e. a parallel combination of resistor and capacitor).

SP1, SP2

Power amplifier outputs during playback. Open-drain pull-ups to VCCAP outside of playback.

GNDA

Ground pin for analog circuitry.

VCCAP

Power analog V_{CC} supply.

VCCA

Analog V_{CC} supply.

VCCD

Non-permanent digital V_{CC} supply; can be disconnected from V_{CC} during standby.

VCCDP

Permanent digital V_{CC} supply.

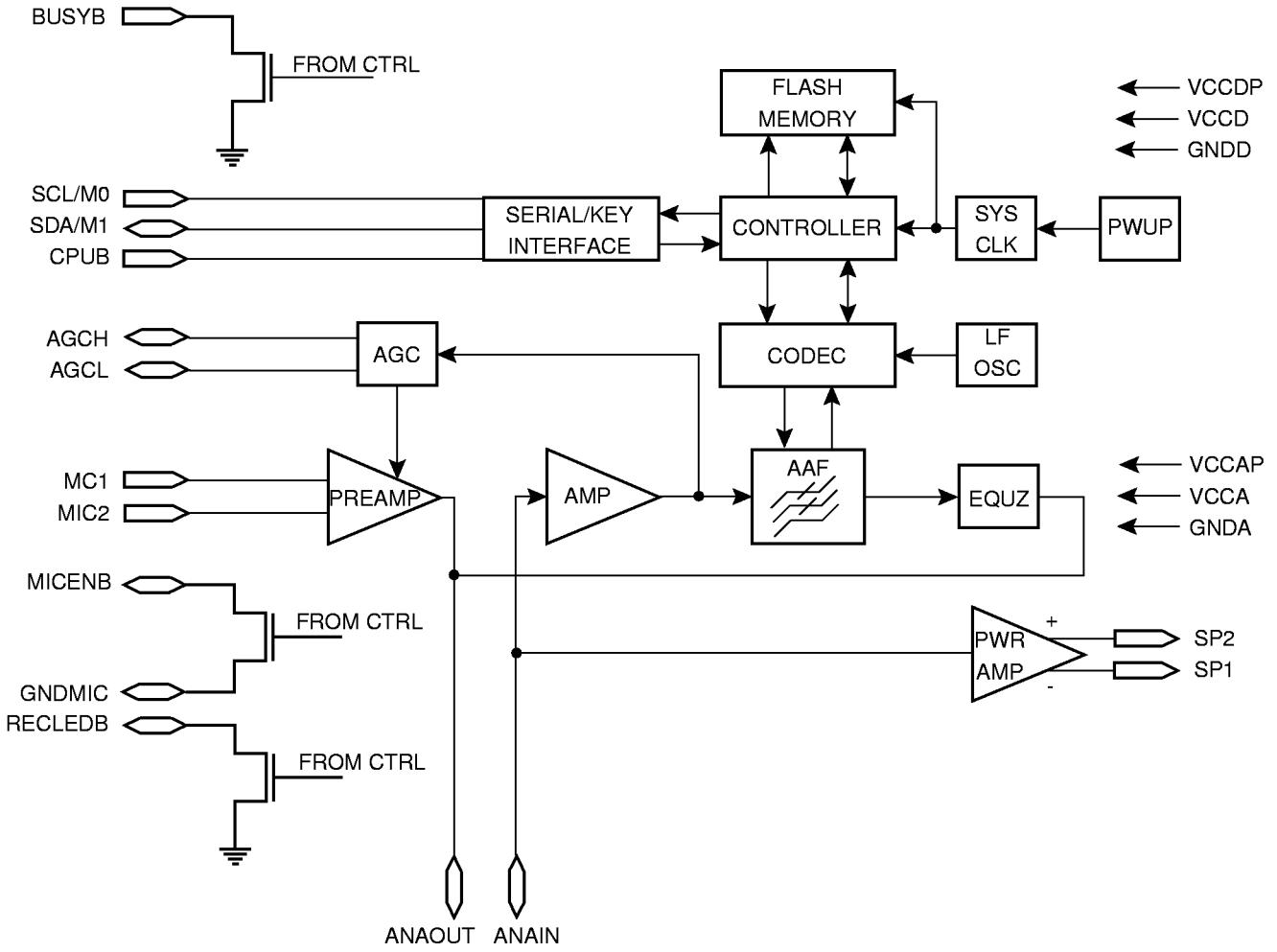
BUSYB

Open-drain pull-down which provides a constant current sink upon wake up. Can be used to bias a PNP transistor connecting the non-permanent VCCD pin to V_{CC}.

RESET

Digital input kept low by an open-drain pull-down. Can be pulled high with a switch to V_{CC}. A high level on RESET will send the chip into standby mode.

Figure 1. AT72AV020 System Diagram



Pin Capacitance[1]

Symbol	Parameter	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (SCL)	6	pF	$V_{I/O}$ = 0V

Note: 1. This parameter is characterized and is not 100% tested

DC Characteristics

T_A= 0°C to 70°C

Symbol	Parameter	Condition	At Pin	Min	Typ	Max	Unit
V_{CC}	Supply Voltage			1.8	3.0	3.6	V
I_{WUP} I_{RD} I_{WR} I_{REC} I_{PLY} I_{ERS}	Supply Current	Wake Up Read Write Record Play Erase			2 3 7 10 10 10		mA
I_{S1}	Standby Current	CMOS	VCCAP + VCCA+ VCCDP			0.1	µA
I_{S2}	Standby Current	CMOS	VCCD		1	10	µA
V_{IL}	Input “L” level			-0.3		0.3 V_{CC}	V
V_{IH}	Input “H” level			0.7 V_{CC}		V_{CC} +0.3	V
I_{SINK}	Input Sink	V_{IH}	M0 or M1 or RESET		30		µA
I_{LEAK}	Input Leakage	V_{IH}	SCL or SDA or BUSYB or MICENB or RECLEDB			0.1	µA
V_{OL}	Output “L” level	I_{OL} = 2 mA	SDA or MICENB or RECLEDB			0.3	V
I_{BS}	BUSYB Sink	V_{CC} -0.7 V	BUSYB	0.5	1.0	1.5	mA
V_{OHPD}	Standby Output	I_{OH} = -1 mA	SP1 or SP2	V_{CC} -0.1			V

Analog AC Characteristics

V_{CC} = 1.8V to 3.6V, T_A= 0°C to 70°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_S	Sampling Frequency(1)			6.4	8.0	kHz
BW	Bandwidth(1)	f_S = 6.4 kHz f_S = 8.0 kHz			2.803 3.504	kHz
$\Delta f_S / f_S$	f_S Tolerance		-5		+5	%
R_{MIC}	MIC Input Resistance(2)	Differential		40		kΩ
R_{ANAIN}	ANAIN Input Resistance(2)	VG Referenced		15		kΩ
V_{IN}	Input Voltage(2)	Differential			32	mV_{PP}
A_V	Analog Gain(3)	Automatic/ Fixed	45		75	dB
ΔA_P	Pre-Amp Gain Tolerance(3)	Fixed Gain	-1.5		+ 1.5	dB
V_O	Output Voltage Swing(3)	Differential			4.8	V_{PP}
V_{OS}	Output Offset Voltage(4)	Silent Play			50	mV
THD	Output Total Harmonic Distortion(5)	@ 1 kHz VO = $4.5V_{PP}$		1	3	%
R_{OUT}	Output Resistance(6)	Not in PLAY		60		Ω
Z_L	Speaker Impedance	Differential	32			Ω

Note: 1. Sampling frequency is factory set to 6.4 kHz. Upper bandwidth limit tracks sampling frequency. The low cutoff frequency results from AC couplings: microphone to MIC inputs and ANAOUT to ANAIN. The on-chip codec has a built-in low cutoff frequency <50 Hz.
A 5th-order elliptic switched capacitor filter (SCF) band-limits the input signal. The filter parameters are:

Sampling Frequency	Pass Band	Ripple	Stop Band	Attenuation
6.4 kHz	2.803 kHz	0.5 dB	3.472 kHz	>36 dB
8.0 kHz	3.504 kHz	0.5 dB	4.340 kHz	>36 dB

2. The DC level of the MIC, ANAOUT and ANAIN pins is at virtual ground (VG). VG is approximately halfway between GND and V_{CC}. The input voltage V_{IN} can be applied to the pre-amplifier or directly to the amplifier input.
3. Pre-amp gain can be adjusted in 3 dB steps from 0 dB to 30 dB. Fixed gain or automatic gain control (AGC) is selected at the factory. Amplifier gain is fixed at approximately 28 dB. Maximum input signal to the amplifier is 32 mV_{PP}, resulting in a recorded full-scale signal of approximately 800 mV_{PP}. The power amplifier further amplifies the stored signal by 16 dB, yielding a maximum differential output signal of 4.80 V_{PP}. The DC level of the power amplifier outputs is at VG.
4. Output offset can be measured by playing back constant memory content, or by (capacitively) grounding the ANAIN input during playback.
5. V_{CC} must match the output signal amplitude to avoid clipping.
6. The power amplifier outputs SP1 and SP2 are connected to VCCAP in any mode, but PLAY.

Serial Bus Waveforms

Serial Clock (SCL) and Serial Data I/O (SDA)

Figure 2. Data Validity

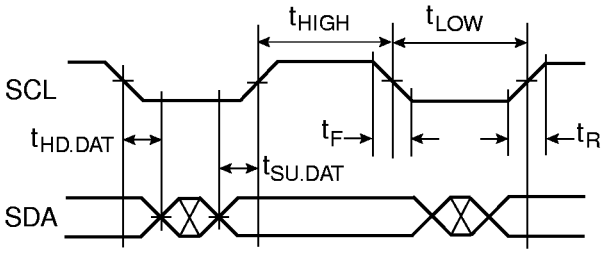


Figure 3. Start and Stop Definition

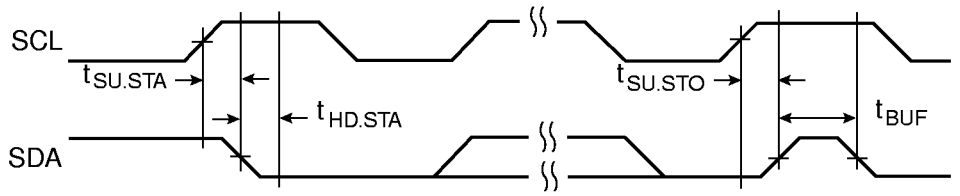
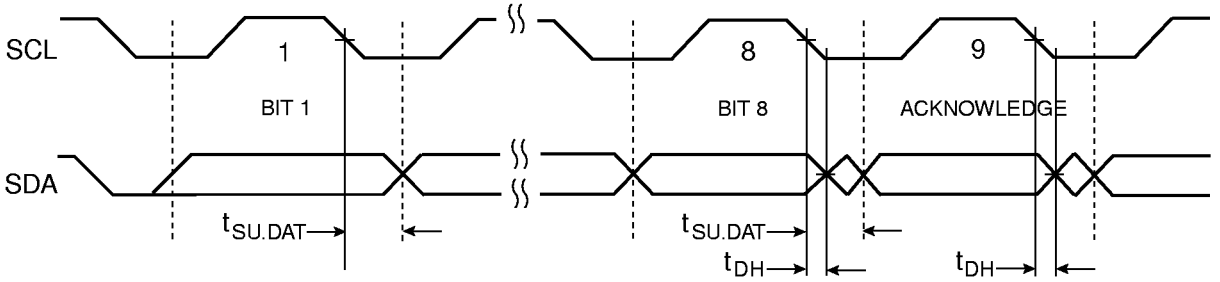


Figure 4. Serial Bus Timing



Digital AC Characteristics

V_{CC} = 1.8V to 3.6V, T_A = 0°C to 70°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{SCL}	Serial Clock Frequency	Internal Memory External Memory	 90		50 110	kHz
t_{LOW}	Serial Clock Low	Internal Memory External Memory	10 4.5		 5.5	µs
t_{HIGH}	Serial Clock High	Internal Memory External Memory	10 4.5		 5.5	µs
t_{BUF}	Buffer Time(1)		5			µs
$t_{SU.STA}$	Start Setup		5			µs
$t_{HD.STA}$	Start Hold		5			µs
$t_{SU.STO}$	Stop Setup		5			µs
$t_{SU.DAT}$	Data In Setup		1			µs
$t_{HD.DAT}$	Data In Hold		1			µs
t_R	Input Rise Time				1	µs
t_F	Input Fall Time				0.3	µs
t_{DH}	Data Out Hold		0.3		1.6	µs
t_{SER}	Sector Erase Time(2)	CPU Mode		180		ms
t_{ERS}	Chip Erase Time(2)	Whole Chip		3		s
t_{NR}	Noise Rejection(3)	CPU Mode		60		ns
t_{DB}	Debounce Time(4)	Stand-alone Mode		80		ms

Notes:
1. Time the bus must be free before a new transition can start.
2. Sector erase time is inversely proportional to sampling frequency. The typical values apply at 6.4 kHz sampling frequency. Chip erase time is approximately 16 times longer than sector erase time.
3. In CPU Mode the control inputs SCL and SDA are filtered to reject spurious pulses.
4. In Stand-alone Mode the control inputs M0 and M1 are debounced.

Device Operation

Stand-alone Mode

A high level on CPUB enables the Stand-alone Mode. The key inputs, M0 and M1 are normally kept low by open drain pull-downs and can be pulled high through switches connected to V_{CC}.

Stand-alone Operation is decoded as follows:

	M0	M1	Condition
Standby	0	0	
Record	1	0	High Level on M0
Play	0	1	High Pulse on M1
Erase	1	1	Overlapping High Pulses on M0 and M1

Up to 16 distinct messages can be stored into on-chip flash memory. Maximum message length, at 6.4 kHz sampling frequency, is 40 seconds. The flash memory is divided into 16 sectors and new messages start at the beginning of sectors.

Recording takes place as long as M0 is high and stops when M0 goes low. Following a RECORD request, the new message will be automatically stored into the next available free sector(s). An attempt to record into a full memory will start PLAY.

Applying a high pulse on M1 activates PLAY. The oldest recorded and not played message will be played first, unless all messages have been played before. In the latter case PLAY will start from beginning of memory. Once started, PLAY will continue until the end of memory. Pulsing M1 during PLAY causes SKIP to the next message. A SKIP request within the last message will stop PLAY. Empty sector sections are not played (i.e. they are skipped).

ERASE is activated by overlapping high pulses on M0 and M1 and is self-timed.

Upon completion of ERASE, PLAY or RECORD the chip powers down to STANDBY mode. Minimum power consumption during STANDBY can be achieved by disconnecting the non-permanent supply pin, VCCD, from main V_{CC} (e.g. battery). For this purpose a PNP transistor driven by BUSYB can be used. The chip will wake up upon detecting high levels on M0 and/or M1 and will “turn on” BUSYB, thus providing base current to a PNP switch which connects the non-permanent supply pin to main V_{CC}. Upon completion of ERASE, PLAY or RECORD, BUSYB will “turn off”, thus disconnecting the non-permanent supply pin from main V_{CC}. A resistor in parallel with the base-emitter junction of the PNP switch should minimize leakage through the switch itself.

CPU Mode

In CPU Mode communication between the chip and the outside world follows a 2-wire bi-directional data transmission protocol. The SDA pin is normally pulled high by an external resistor. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a START or STOP condition. A high-to-low transition of SDA with SCL high is a START condition and must precede every command. A low-to-high transition of SDA with SCL high is a STOP condition and signals the end of a specific activity. Commands and data are serially transmitted to and from the chip in 8-bit words corresponding to eight SCL time slots. The chip will acknowledge receiving the 8-bit word by pulling the SDA line low during the 9th time slot. In DATA READ mode the chip will relinquish control of the SDA line during the 9th time slot. The external controller must acknowledge during the 9th time slot to continue reading or not acknowledge and then follow up with a STOP condition to stop reading. The chip will not acknowledge commands if it is busy.

ERASE, PLAY and RECORD commands are now sector specific – rather than message specific, as they are in Stand-alone Mode. Messages spreading over sector boundaries can be played or recorded by concatenating PLAY or RECORD commands. At the nominal sampling frequency of 6.4 kHz it takes approximately 2.5 seconds to play or record a sector, and less than 1 ms to send a PLAY or RECORD command to the chip; therefore the chip can accept a second command while it executes the first one. The on-chip FIFO address stack can hold two sector addresses and can be updated once the used sector address is no longer needed. This mechanism allows for seamless recording or playback across sector boundaries.

The CPU Mode commands are:

Mnemonic	Command	Opcode	Bytes
	Wake Up	AE (Preamble = P)	1
	Go to Sleep	AF	1
CER	Chip Erase	P + AA	2
SER	Sector Erase	P + AC + Address	5
REC	Sector Record	P + A2 + Address	5
PLY	Sector Play	P + A4 + Address	5
XAM	Exit All Modes	P + AE	2
DWR	Data Write	P + A6 + Address + Data	5+
DRD	Data Read	P + A8 + Address + Data	5+
MIC	Read from Microphone	P + 52 + Data	2+
SPK	Write to Speaker	P + 54 + Data	2+
AGF	AGC Off	P + 64	2
AGR	Gain Reset	P + 62	2
AGI	Gain Increment	P + 66	2

Wake Up: is a command and a preamble to every other command. The 8-bit Wake Up command consists of the sequence 1010 1110 (AE). When terminated with a STOP, the command will simply wake up the chip from STANDBY mode. During wake up the chip will undergo a power up routine, which lasts for approximately 40 ms. Additional commands are rejected during power up. Wake Up will be acknowledged unconditionally. The Wake Up preamble (AE) is part of every other command, except for the complementary Go to Sleep command.

Go to Sleep: is the command that will send the chip into STANDBY mode; it consists of the sequence 1010 1111 (AF) and must be packaged with START, acknowledge slot and STOP.

Chip Erase – CER: is a two-byte command consisting of preamble and the sequence AA; it activates a full chip erase, which is self-timed and non-interruptible.

Sector Erase – SER: is a multiple byte command consisting of preamble, the sequence AC and three address bytes identifying the target sector. The 16 starting sector addresses are:

- 00 00 00
- 00 40 00
- 00 80 00
- 00 C0 00
- 01 00 00
- 01 40 00
- 01 80 00
- 01 C0 00
- 02 00 00
- 02 40 00
- 02 80 00
- 02 C0 00
- 03 00 00
- 03 40 00
- 03 80 00
- 03 C0 00

Sector erase is a self-timed, non-interruptible operation.

Sector Record – REC: is a multiple byte command consisting of preamble, the sequence A2 and three address bytes identifying the target sector. Following the first application of the REC command, the chip will undergo a “warm up” routine which lasts for approximately 40 ms, after which actual recording will commence. The first byte of the first sector will be left blank – to be used as a message marker. Recording will continue until the target sector is full, or can be stopped with an Exit All Modes command. Multiple sector messages require repeated REC requests. Up to two such requests can be queued at one time, while a third one will only be accepted after the previous to last request has been serviced (i.e. the corresponding sector is full).

Sector Play – PLY: is a multiple byte command consisting of preamble, the sequence A4 and three address bytes identifying the target sector. Following the first application of the PLY command, the chip will undergo a “warm up” routine which lasts for approximately 40 ms, after which actual playback will commence. Playback will continue until the target sector is exhausted, or can be stopped with an Exit All Modes command. Multiple sector messages require repeated PLY requests. Up to two such requests can be queued at one time, while a third one will only be accepted after the previous to last request has been serviced (i.e. the corresponding sector has been played).

Exit All Modes – XAM: is a 2-byte command consisting of preamble and the sequence AE. This command will return the chip to WAKE_UP mode; it can be used to stop recording or playback, but it will not be accepted while erase is in progress.

Data Write – DWR: is a multiple byte command consisting of preamble, the sequence A6, three address bytes for the starting address and data. One single byte or many sequential bytes can be written with one DWR command. Applying a STOP condition ends data write.

Data Read – DRD: is a multiple byte command consisting of preamble, the sequence A8 and three address bytes for the starting address. The chip will output data as long as the receiver acknowledges it.

Read from Microphone – MIC: is a multiple byte command consisting of preamble and the sequence 52. This command is used to record encoded data into external memory, instead of writing it to on-chip memory. The chip will output data as long as the receiver acknowledges it.

Write to Speaker – SPK: is a multiple byte command consisting of preamble, the sequence 54 and encoded data. This command is used to playback encoded data from external memory. Data presented by the transmitter on the SDA bus is converted to analog signal at the SP outputs. Applying a STOP condition will end playback.

AGC Off – AGF: is a multiple byte command consisting of preamble and the sequence 64. This command is used to turn off the Automatic Gain Control capability. AGF resets the pre-amp gain to the factory set default.

Gain Reset – AGR: is a multiple byte command consisting of preamble and the sequence 62. AGR, in conjunction with AGF, resets the pre-amp gain to 0 dB.

Gain Increment – AGI: is a multiple byte command consisting of preamble and the sequence 66. AGI, in conjunction with AGF, increments the pre-amp gain by 3 dB.