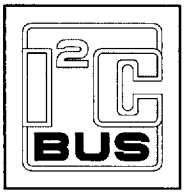
CMOS single-chip 8-bit microcontroller — 87C528



FEATURES

- 80C51 instruction set
  - 32k × 8 EPROM
  - 512 × 8 RAM
  - Memory addressing capability 64k ROM and 64k RAM
  - Three 16-bit counter/timers
  - On-chip watchdog timer with oscillator
  - Full duplex UART
  - I^2C serial interface
- Power control modes
  - Idle mode
  - Power-down mode
  - Warm start from power-down
- CMOS and TTL compatible
- Two speed ranges at V_{CC} = 5V
  - 16MHz
- OTP package available
- EPROM code protection

DESCRIPTION

The 87C528 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 87C528 has the same instruction set as the 80C51.

This device provides architectural enhancements that make it applicable in a variety of applications in consumer, telecom and general control systems, especially in those systems which need large ROM and RAM capacity on-chip.

The 87C528 contains a 32k × 8 EPROM, a 512 × 8 RAM, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a 16-bit timer (identical to the timer 2 of the 80C52), a watchdog timer with a separate oscillator, a multi-source, two-priority-level, nested interrupt structure, two serial interfaces (UART and I^2C-bus), and on-chip oscillator and timing circuits.

In addition, the 87C528 has two software selectable modes of power reduction — idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG DESIGNATOR*
40-pin Ceramic DIP	87C528/BQA	GDIP1-T40
44-pin Ceramic Quad Flat Pack (QFP)	87C528/BMA	GQCCI-J44

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

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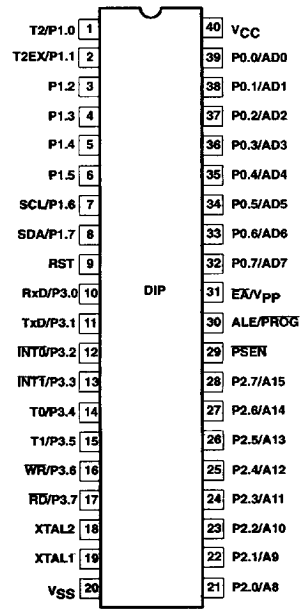
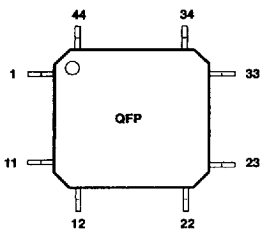
PIN CONFIGURATIONS





Pin	Function	Pin	Function
1	P1 5	23	P2 5/A13
2	P1 6/SCL	24	P2 6/A14
3	P1.7/SDA	25	P2 7/A15
4	RST	26	PSEN
5	P3 0/RxD	27	ALE/PROG
6	NC	28	NC
7	P3.1/TxD	29	EA/VPP
8	P3 2/INT0	30	P0 7/AD7
9	P3 3/INT1	31	P0 6/AD6
10	P3 4/T0	32	P0 5/AD5
11	P3 5/T1	33	P0 4/AD4
12	P3.6/WR	34	P0 3/AD3
13	P3 7/RD	35	P0 2/AD2
14	XTAL2	36	P0 1/AD1
15	XTAL1	37	P0 0/AD0
16	VSS	38	VCC
17	NC	39	NC
18	P2 0/A8	40	P1 0/T2
19	P2 1/A9	41	P1 1/T2EX
20	P2.2/A10	42	P1.2
21	P2.3/A11	43	P1 3
22	P2 4/A12	44	P1.4

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PIN DESCRIPTION

Mnemonic	Pin No. DIP	LCC	QFP	Type	Name and Function
V_{SS}	20	22	16	I	**Ground:** 0V reference
V_{CC}	40	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation
P0 0–0 7	39–32	43–36	37–30	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port Port 0 pins that have 1s written to them float and can be used as high-impedance inputs Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory In this application, it uses strong internal pull-ups when emitting 1s Port 0 also outputs the code bytes during program verification in the P87C528 External pull-ups are required during program verification
P1.0–P1.7	1–8	2–9	40–44 1–3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups, except P1 6 and P1 7 which have open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups (See DC Electrical Characteristics I_{IL}) Port 1 can sink/source one TTL (4 LSTTL) inputs Port 1 receives the low-order address byte during program memory verification Port 1 also serves alternate functions for timer 2.
	1	2	40	I	**T2 (P1.0):** Timer/counter 2 external count input
	2	3	41	I	**T2EX (P1.1):** Timer/counter 2 trigger input
	7	8	2	I/O	**SCL (P1.6):** I^2C serial port clock line
	8	9	3	I/O	**SDA (P1.7):** I^2C serial port data line
P2 0–P2 7	21–28	24–31	18–25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups (See DC Electrical Characteristics I_{IL}) Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR) In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3 7	10–17	11, 13–19	5, 7–13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups (See DC Electrical Characteristics: I_{IL}) Port 3 also serves the special features of the SC80C51 family, as listed below
	10	11	5	I	**RxD (P3.0):** Serial input port
	11	13	7	O	**TxD (P3.1):** Serial output port
	12	14	8	I	**$\overline{INT0}$ (P3.2):** External interrupt
	13	15	9	I	**$\overline{INT1}$ (P3.3):** External interrupt
	14	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	18	12	O	**$\overline{WR}$ (P3.6):** External data memory write strobe
	17	19	13	O	**$\overline{RD}$ (P3.7):** External data memory read strobe
RST	9	10	4	I/O	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC} After a watchdog timer overflow, this pin is pulled high while the internal reset signal is active
ALE/$\overline{PROG}$	30	33	27	I/O	**Address Latch Enable/Program Pulse:** Output pulse for latching the low byte of the address during an access to external memory In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{PROG}$) during EPROM programming.
$\overline{PSEN}$	29	32	26	O	**Program Store Enable:** The read strobe to external program memory When the device is executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
$\overline{EA}$/V_{PP}	31	35	29	I	**External Access Enable/Programming Supply Voltage:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H to 7FFFH If $\overline{EA}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than 7FFFH This pin also receives the 12 75V programming supply voltage (V_{PP}) during EPROM programming
XTAL1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits
XTAL2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier

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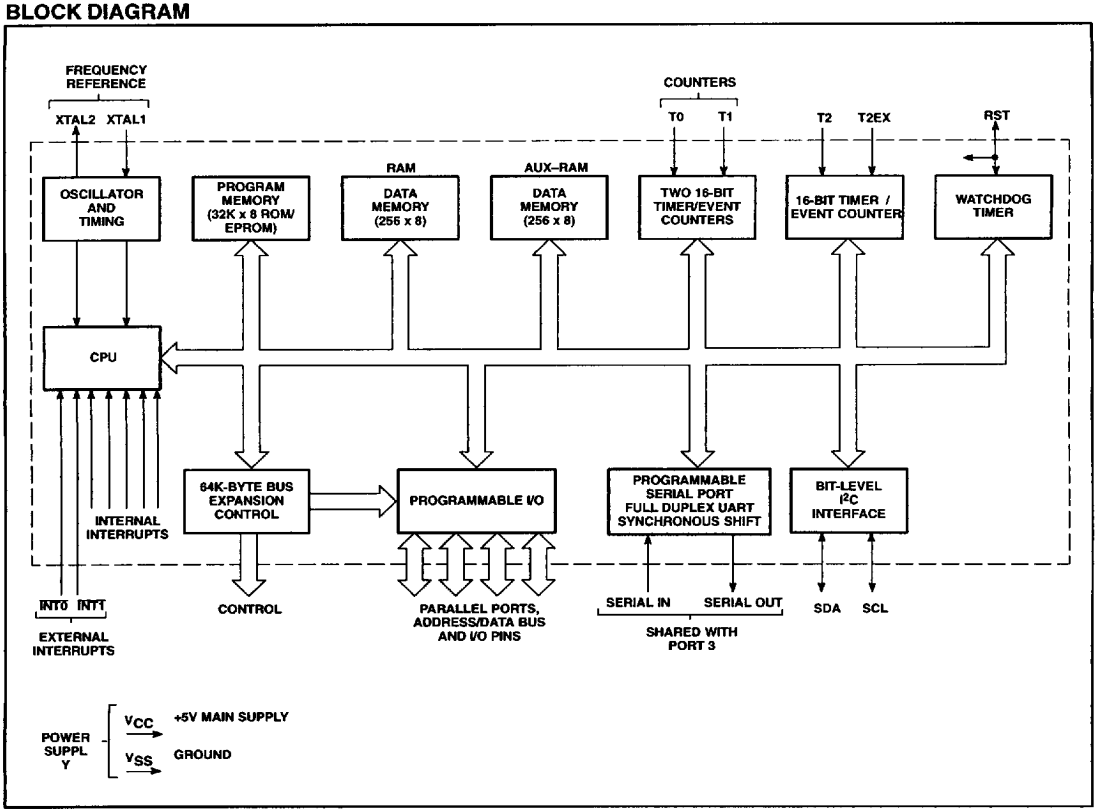
BLOCK DIAGRAM



LOGIC SYMBOL

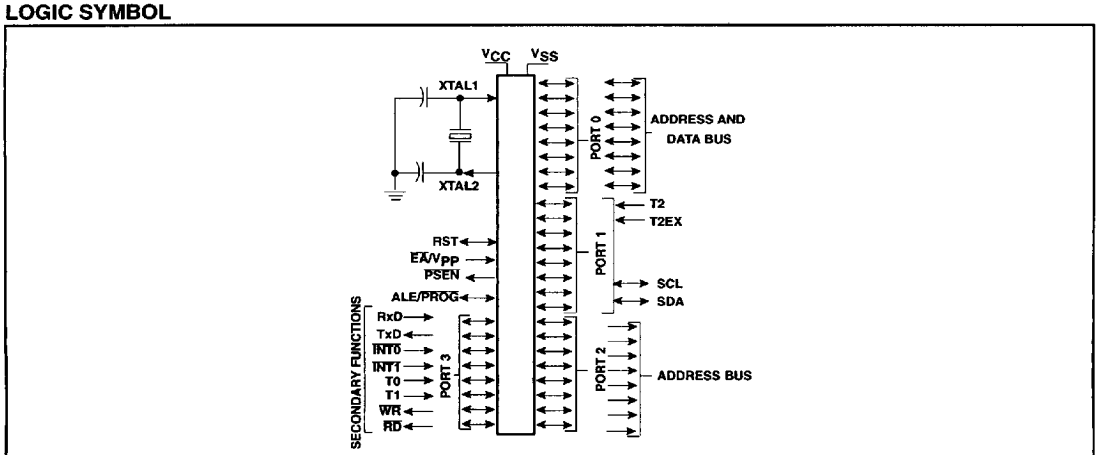


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Table 1. Internal and External Program Memory Access with Security Bit Set

INSTRUCTION	ACCESS TO INTERNAL PROGRAM MEMORY	ACCESS TO EXTERNAL PROGRAM MEMORY
MOVC in internal program memory	YES	YES
MOVC in external program memory	NO	YES

ROM CODE PROTECTION

By setting a mask programmable security bit, the ROM content in the 83C528 is protected, i e , it cannot be read out by any test mode or by any instruction in the external program memory space. The MOVC instructions are the only ones which have access to program code in the internal or external program memory. The $\overline{EA}$ input is latched during RESET and is 'don't care' after RESET This implementation prevents reading from internal program code by switching from external program memory to internal program memory during MOVC instruction or an instruction that handles immediate data Table 1 lists the access to the internal and external program memory by the MOVC instructions when the security bit has been set to logical one If the security bit has been set to a logical 0 there are no restrictions for the MOVC instructions

INTERNAL DATA MEMORY

The internal data memory is divided into three physically separated segments: 256 bytes of RAM, 256 bytes of AUX-RAM, and a 128 bytes special function area These can be addressed each in a different way.

- RAM 0 to 127 can be addressed directly and indirectly as in the 80C51 Address pointers are R0 and R1 of the selected register bank
- RAM 128 to 255 can only be addressed indirectly as in the 80C51. Address pointers are R0 and R1 of the selected register bank
- AUX-RAM 0 to 255 is indirectly addressed in the same way as external data memory with the MOVX instructions Address pointers are R0, R1 of the selected register bank and DPTR An access to AUX-RAM 0 to 255 will not affect ports P0, P2, P3 6 and P3 7

An access to external data memory locations higher than 255 will be performed with the MOVX DPTR instructions in the same way as in the 8051 structure, so with P0 and P2 as data/address bus and P3 6 and P3 7 as write and read timing signals Note that these external data memory cannot be accessed with R0 and R1 as address pointer

TIMER 2

Timer 2 is functionally equal to the Timer 2 of the 8052AH Timer 2 is a 16-bit timer/counter. These 16 bits are formed by two special function registers TL2 and TH2 Another pair of special function register RCAP2L and RCAP2H form a 16-bit capture register or a 16-bit reload register Like Timer 0 and 1, it can operate either as a timer or as an event counter This is selected by bit C/T2N in the special function register T2CON. It has three operating modes. capture, autoload, and baud rate generator mode which are selected by bits in T2CON

WATCHDOG TIMER T3

The watchdog timer consists of an 11-bit prescaler and an 8-bit timer formed by special function register T3 The prescaler is incremented by an on-chip oscillator with a fixed frequency of 1MHz. The maximum tolerance on this frequency is –50% and +100% The 8-bit timer increments every 2048 cycles of the on-chip oscillator When a timer overflow occurs, the microcontroller is reset and a reset output pulse of 16 x 2048 cycles of the on-chip oscillator is generated at pin RST The internal RESET signal is not inhibited when the external RST pin is kept low by, for example, an external reset circuit The RESET signal drives port 1, 2, 3 into the high state and port 0 into the high impedance state.

The watchdog timer is controlled by one special function register WDCON with the direct address location A5H WDCON can be read and written by software. A value of A5H in WDCON halts the on-chip oscillator and clears both the prescaler and timer T3 After the RESET signal, WDCON contains A5H Every value other than A5H in WDCON enables the watchdog timer When the watchdog timer is enabled, it runs independently of the XTAL-clock.

Timer T3 can be read on the fly. Timer T3 can only be written if WDCON contains the value 5AH A successful write operation to T3 will clear the prescaler and WDCON, leaving the watchdog enabled and preventing inadvertent changes of T3 To prevent an overflow of the watchdog timer, the user program has to reload the watchdog timer within periods that are shorter than the programmed watchdog timer internal This time interval is determined by an 8-bit value that has to be loaded in register T3 while at the same time the prescaler is cleared by hardware.

Watchdog timer interval =

$$\frac{[256 - (T3)] \times 2048}{\text{on - chip oscillator frequency}}$$

BIT-LEVEL I²C INTERFACE

This bit-level serial I/O interface supports the I²C-bus. P1 6/SCL and P1.7/SDA are the serial I/O pins. These two pins meet the I²C specification concerning the input levels and output drive capability Consequently, these pins have an open drain output configuration All the four modes of the I²C-bus are supported

- master transmitter
- master receiver
- slave transmitter
- slave receiver

The advantages of the bit-level I²C hardware compared with a full software I²C implementation are:

- the hardware can generate the SCL pulse
- Testing a single bit (RBF respectively, WBF) is sufficient as a check for error free transmission

The bit-level I²C hardware operates on serial bit level and performs the following functions

- filtering the incoming serial data and clock signals
- recognizing the START condition
- generating a serial interrupt request SI after reception of a START condition and the first falling edge of the serial clock
- recognizing the STOP condition
- recognizing a serial clock pulse on the SCL line
- latching a serial bit on the SDA line (SDI)

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- stretching the SCL LOW period of the serial clock to suspend the transfer of the next serial data bit
- setting Read Bit Finished (RBF) when the SCL clock pulse has finished and Write Bit Finished (WBF) if there is no arbitration loss detected (i.e., SDA = 0 while SDO = 1)
- setting a serial clock Low-to-High detected (CLH) flag
- setting a Bus Busy (BB) flag on a START condition and clearing this flag on a STOP condition
- releasing the SCL line and clearing the CLH, RBF and WBF flags to resume transfer of the next serial data bit
- generating an automatic clock if the single bit data register S1BIT is used in master mode.

The following functions must be done in software:
- handling the I^2C START interrupts
- converting serial to parallel data when receiving
- converting parallel to serial data when transmitting
- comparing the received slave address with its own
- interpreting the acknowledge information
- guarding the I^2C status if RBF or WBF = 0.

Additionally, if acting as master:
- generating START and STOP conditions
- handling bus arbitration
- generating serial clock pulses if S1BIT is not used.

Three SFRs control the bit-level I^2C interface: S1INT, S1BIT and S1SCS.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the Logic Symbol.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-up reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-up, the voltage on V_{CC} and RST must come up at the same time for a proper start-up.

IDLE MODE

In idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. The power-down mode can be terminated by a RESET in the same way as in the 80C51 or in addition by one of two external interrupts, INT0 or INT1. A termination with an external interrupt does not affect the internal data memory and does not affect the special function registers. This makes it possible to exit power-down without changing the port output levels. To terminate the power-down mode with an external interrupt $\overline{INT0}$ or $\overline{INT1}$ must be switched to level-sensitive and must be enabled. The external interrupt input signal $\overline{INT0}$ and $\overline{INT1}$ must be kept low until the oscillator has restarted and stabilized. An instruction following the instruction that puts the device in the power-down mode will be executed. A reset generated by the watchdog timer terminates the power-down mode in the same way as an external RESET, and only the contents of the on-chip RAM are preserved. The control bits for the reduced power modes are in the special function register PCON.

DESIGN CONSIDERATIONS

At power-on, the voltage on V_{CC} and RST must come up at the same time for a proper start-up.

When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when idle is terminated by reset, the instruction following the one that invokes idle should not be one that writes to a port pin or to external memory

Table 2 shows the state of I/O ports during low current operating modes.

Table 2. External Pin Status During Idle and Power-Down Modes

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

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ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

PARAMETER	RATING	UNIT
Operating temperature under bias	-55 to +125	°C
Storage temperature range	–65 to +150	°C
Voltage on $\overline{EA}/V_{PP}$ pin to V_{SS}	0 to +13.0	V
Voltage on any other pin to V_{SS}	–0.5 to V_{CC} +0.5	V
Input, output current on any two pins	±10	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1 0	W

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified All voltages are with respect to V_{SS} unless otherwise noted.

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DC ELECTRICAL CHARACTERISTICS

T_{amb} = –55°C to +125°C, V_{CC} = 5V±10%, V_{SS}=0V

SYMBOL	PARAMETER	Test Conditions	LIMITS MIN	LIMITS MAX	UNIT
V_{IL}	Input low voltage, except $\overline{EA}$, P1.6/SCL, P1.7/SDA		–0.5	$0.2V_{CC}$–0.25	V
V_{IL1}	Input low voltage to $\overline{EA}$		0	$0.2V_{CC}$–0.45	V V
V_{IL2}	Input low voltage to P1.6/SCL, P1.7/SDA[5]		–0.5	$0.3V_{CC}$	V
V_{IH}	Input high voltage, except XTAL1, RST, P1.6/SCL, P1.7/SDA		$0.2V_{CC}$+1.1	V_{CC}+0.5	V
V_{IH1}	Input high voltage, XTAL1, RST		$0.7V_{CC}$+0.2	V_{CC}+0.5	V
V_{IH2}	Input high voltage, P1.6/SCL, P1.7/SDA[5]		$0.7V_{CC}$	6.0	V
V_{OL}	Output low voltage, ports 1, 2, 3, except P1.6/SCL, P1.7/SDA	V_{CC} = 4.5V; I_{OL} = 100µA I_{OL} = 1.6mA I_{OL} = 3.5mA		0.3 0.45 1.0	V V V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$	V_{CC} = 4.5V; I_{OL} = 200µA I_{OL} = 3.2mA I_{OL} = 7.0mA		0.3 0.45 1.0	V V V
V_{OL2}	Output low voltage, P1.6/SCL, P1.7/SDA	I_{OL} = 3.0mA		0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 (except P1.6 and P1.7)	V_{CC} = 4.5V; I_{OH} = –10µA I_{OH} = –30µA I_{OH} = –60µA	 V_{CC}-0.3 V_{CC}-0.7 V_{CC}-1.5		V V V
V_{OH1}	Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$)	V_{CC} = 4.5V; I_{OH} = –200µA I_{OH} = –3.2mA I_{OH} = –7.0mA	 V_{CC}-0.3 V_{CC}-0.7 V_{CC}-1.5		V V V
I_{IL}	Logical 0 input current, ports 1, 2, 3, except P1.6/SCL, P1.7/SDA	V_{IN} = 0.45V		–75	V
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3, except P1.6/SCL, P1.7/SDA	See note 3		–750	µA
I_{L1}	Input leakage current, port 0, $\overline{EA}$	0.45V <V_I <V_{CC}	–10	10	µA
I_{L2}	Input leakage current, P1.6/SCL, P1.7/SDA	0V <Vi < 6.0V 0V <V_{CC} < 5.5V	–10	10	µA
I_{CC}	Power supply current: Active mode @ 16MHz Idle mode @ 16MHz Power down mode	See note 4		 39 7 200	 mA mA µA
R_{RST}	Internal reset pull-down resistor		50	225	kΩ
C_{IO}	Pin capacitance[6]			10	pF

NOTES:

1. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows: 10mA per port pin, port 0 total (all bits) 26mA, ports 1, 2, and total each (all bits) 15mA.
2. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
3. Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
4. See Figures 8 through 12 for I_{CC} test conditions.
5. The input threshold voltage of P1.6 and P1.7 (SIO1) meets the I^2C specification, so an input voltage below 1.5V will be recognized as a logic 0 while an input voltage above 3.0V will be recognized as a logic 1.
6. These values are characterized but not 100% tested.

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AC ELECTRICAL CHARACTERISTICS[1, 2]

SYMBOL	FIGURE	PARAMETER	16MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	1	Oscillator frequency **Speed Versions** 87C528 3.5MHz			3.5	16	MHz
t_{LHLL}	1	ALE pulse width	70		$2t_{CLCL}-55$		ns
t_{AVLL}	1	Address valid to ALE low	23		$t_{CLCL}-40$		ns
t_{LLAX}	1	Address hold after ALE low	13		$t_{CLCL}-50$		ns
t_{LLIV}	1	ALE low to valid instruction in		138		$4t_{CLCL}-115$	ns
t_{LLPL}	1	ALE low to $\overline{PSEN}$ low	7		$t_{CL}-55$		ns
t_{PLPH}	1	$\overline{PSEN}$ pulse width	138		$3t_{CLCL}-50$		ns
t_{PLIV}	1	$\overline{PSEN}$ low to valid instruction in		67		$3t_{CLCL}-120$	ns
t_{PXIX}	1	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	1	Input instruction float after $\overline{PSEN}$		37		$t_{CLCL}-25$	ns
t_{AVIV}	1	Address to valid instruction in		172		$5t_{CLCL}-140$	ns
t_{PLAZ}	1	$\overline{PSEN}$ low to address float		20		20	ns
Data Memory							
t_{RLRH}	2, 3	$\overline{RD}$ pulse width	275		$6t_{CLCL}-100$		ns
t_{WLWH}	2, 3	$\overline{WR}$ pulse width	275		$6t_{CLCL}-100$		ns
t_{RLDV}	2, 3	$\overline{RD}$ low to valid data in		137		$5t_{CLCL}-175$	ns
t_{RHDX}	2, 3	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	2, 3	Data float after $\overline{RD}$		40		$2t_{CLCL}-85$	ns
t_{LLDV}	2, 3	ALE low to valid data in		330		$8t_{CLCL}-170$	ns
t_{AVDV}	2, 3	Address to valid data in		377		$9t_{CLCL}-185$	ns
t_{LLWL}	2, 3	ALE low to $\overline{RD}$ or $\overline{WR}$ low	137	237	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	2, 3	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	120		$4t_{CLCL}-130$		ns
t_{QVWX}	2, 3	Data valid to $\overline{WR}$ transition	12		$t_{CLCL}-50$		ns
t_{WHQX}	2, 3	Data hold after $\overline{WR}$	12		$t_{CLCL}-50$		ns
t_{RLAZ}	2, 3	$\overline{RD}$ low to address float		0		0	ns
t_{WHLH}	2, 3	$\overline{RD}$ or $\overline{WR}$ high to ALE high	22	102	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
External Clock							
t_{CHCX}	6	High time	20		20		ns
t_{CLCX}	6	Low time	20		20		ns
t_{CLCH}	6	Rise time		20		20	ns
t_{CHCL}	6	Fall time		20		20	ns
Shift Register							
t_{XLXL}	4	Serial port clock cycle time	750		$12t_{CLCL}$		ns
t_{QVXH}	4	Output data setup to clock rising edge	492		$10t_{CLCL}-133$		ns
t_{XHQX}	4	Output data hold after clock rising edge	8		$2t_{CLCL}-117$		ns
t_{XHDX}	4	Input data hold after clock rising edge	0		0		ns
t_{XHDV}	4	Clock rising edge to input data valid		492		$10t_{CLCL}-133$	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.

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AC ELECTRICAL CHARACTERISTICS – I²C INTERFACE[7]

SYMBOL	PARAMETER	INPUT	OUTPUT	I²C SPECIFICATION
SCL TIMING CHARACTERISTICS				
t_{HD}; STA	START condition hold time	≥ 14 t_{CLCL}[1]	Note 2	≥ 4.0µs
t_{LOW}	SCL LOW time	≥ 16 t_{CLCL}	Note 2	≥ 4.7µs
t_{HIGH}	SCL HIGH time	≥ 14 t_{CLCL}[1]	≥ 80 t_{CLCL}[3]	≥ 4.0µs
t_{RC}	SCL rise time	≤ 1µs[4]	Note 5	≤ 1.0µs
t_{FC}	SCL fall time	≤ 0.3µs[4]	≤ 0.3µs[6]	≤ 0.3µs
SDA TIMING CHARACTERISTICS				
t_{SU}; DAT1	Data set-up time	≥ 250ns	Note 2	≥ 250ns
t_{HD}; DAT	Data hold time	≥ 0ns	Note 2	≥ 0ns
t_{SU}; STA	Repeated START set-up time	≥ 14 t_{CLCL}[1]	Note 2	≥ 4.7µs
t_{SU}; STO	STOP condition set-up time	≥ 14 t_{CLCL}[1]	Note 2	≥ 4.0µs
t_{BUF}	Bus free time	≥ 14 t_{CLCL}[1]	Note 2	≥ 4.7µs
t_{RD}	SDA rise time	≤ 1µs[4]	Note 5	≤ 1.0µs
t_{FD}	SDA fall time	≤ 0.3µs[4]	≤ 0.3µs[6]	≤ 0.3µs

NOTES:
1. At f_{CLK} = 3.5MHz, this evaluates to 14 × 286ns = 4µs, i.e., the bit-level I²C interface can respond to the I²C protocol for f_{CLK} ≥ 3.5MHz.
2. This parameter is determined by the user software, it has to comply with the I²C.
3. This value gives the autoclock pulse length which meets the I²C specification for the specified XTAL clock frequency range. Alternatively, the SCL pulse may be timed by software.
4. Spikes on SDA and SCL lines with a duration of less than 4 × f_{CLK} will be filtered out.
5. The rise time is determined by the external bus line capacitance and pull-up resistor, it must be ≤ 1µs.
6. The maximum capacitance on bus lines SDA and SCL is 400pF.
7. These valves are characterized but not 100% production tested.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address
C – Clock
D – Input data
H – Logic level high
I – Instruction (program memory contents)
L – Logic level low, or ALE
P – $\overline{PSEN}$
Q – Output data
R – $\overline{RD}$ signal
t – Time
V – Valid
W – $\overline{WR}$ signal
X – No longer a valid logic level
Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.
t_{LLPL} = Time for ALE low to $\overline{PSEN}$ low.

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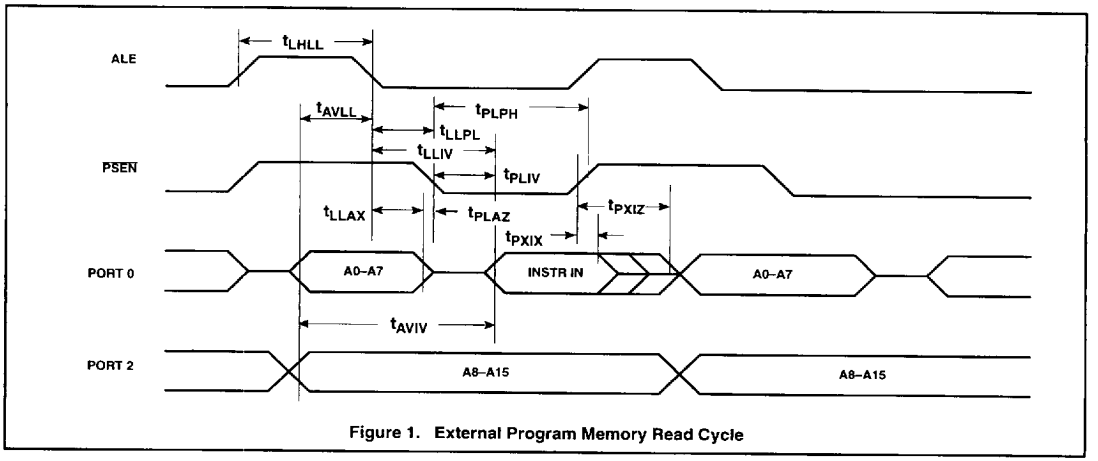

Figure 1. External Program Memory Read Cycle

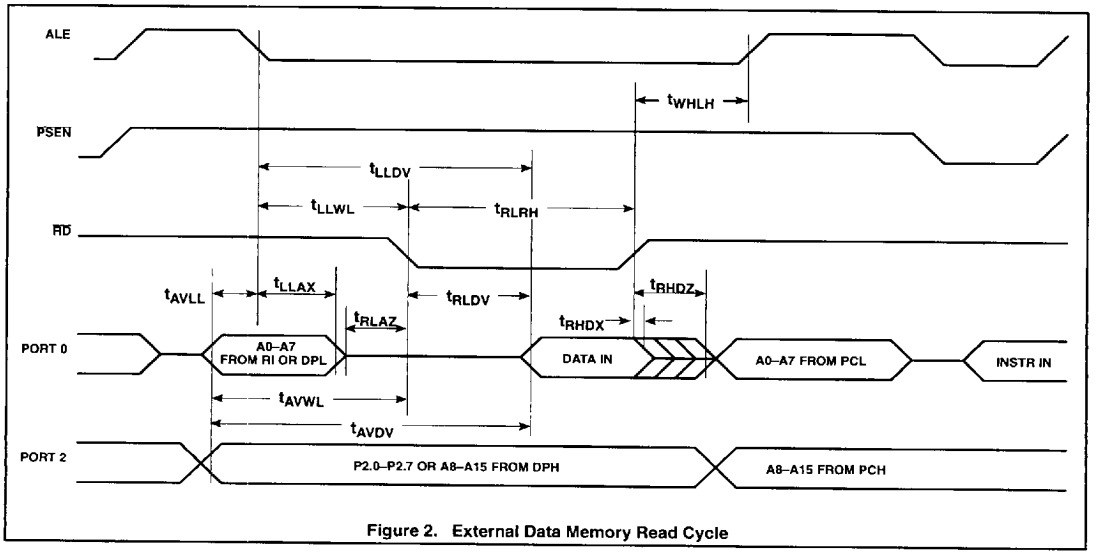

Figure 2. External Data Memory Read Cycle

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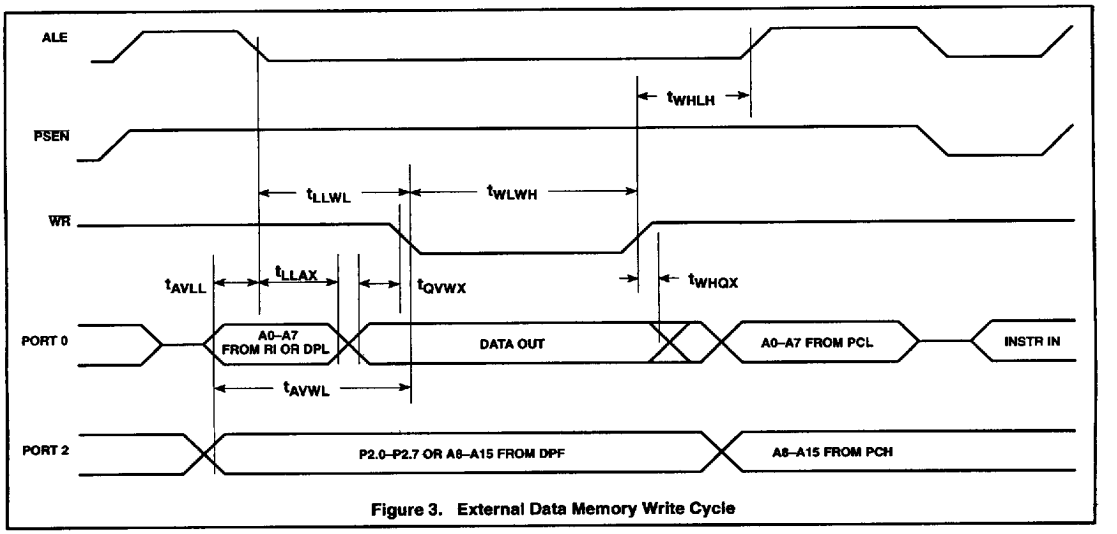

Figure 3. External Data Memory Write Cycle

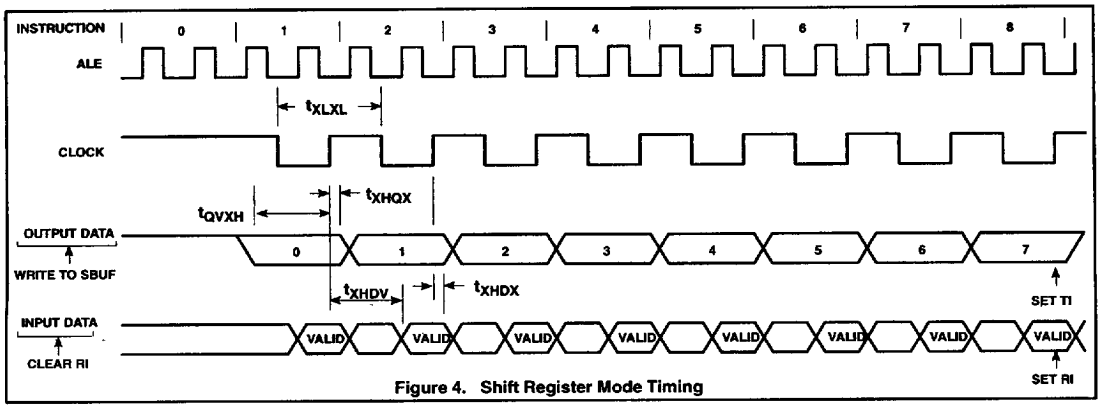

Figure 4. Shift Register Mode Timing

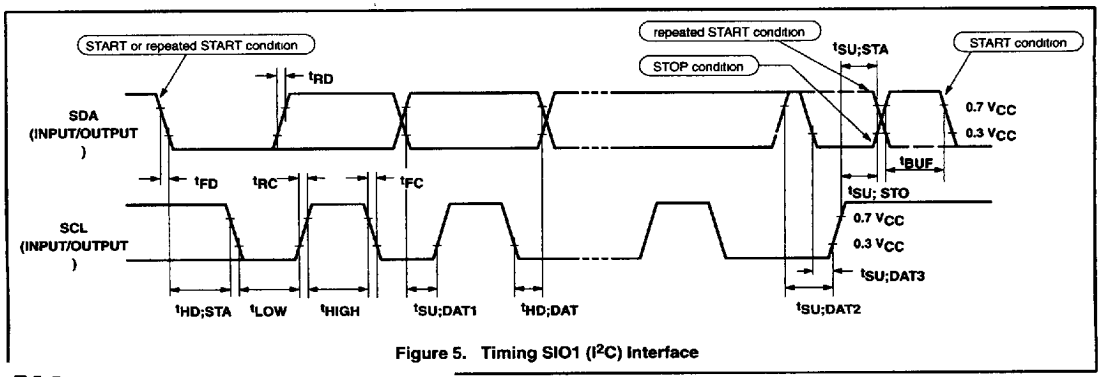

Figure 5. Timing SIO1 (I^2C) Interface

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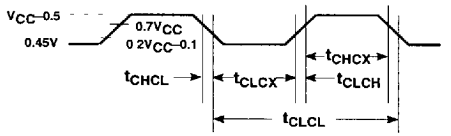
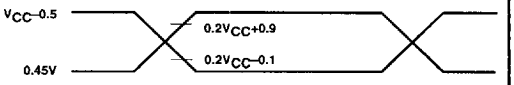
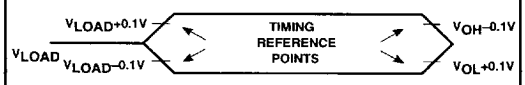


Figure 6. External Clock Drive



NOTE:
AC inputs during testing are driven at V_{CC} –0 5 for a logic '1' and 0 45V for a logic '0 Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} for a logic '0'

Figure 7. AC Testing Input/Output



NOTE:
For timing purposes a port is no longer floating when a 100mV change from load voltage occurs and begins to float when a 100mV change from the loaded V_{OH}/V_{OL} level occurs $I_{OH}/I_{OL} \geq \pm 20$mA

Figure 9. Float Waveform

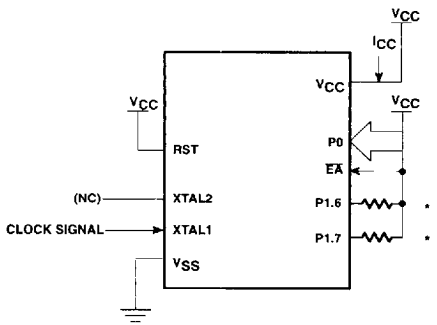


Figure 8. I_{CC} Test Condition, Active Mode
All other pins are disconnected

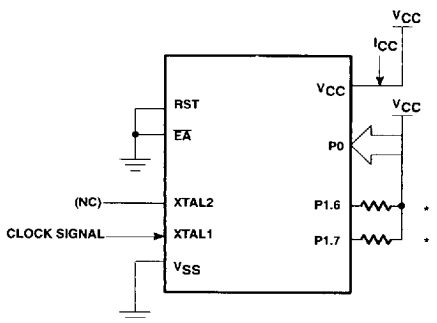


Figure 10. I_{CC} Test Condition, Idle Mode
All other pins are disconnected

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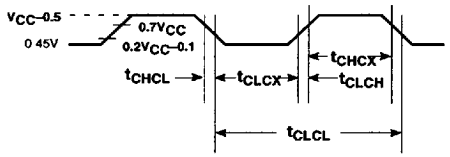

Figure 11. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes $t_{CLCH} = t_{CHCL} = 5ns$

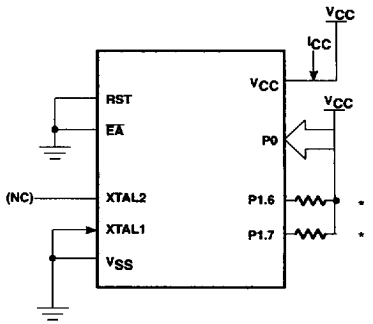

Figure 12. I_{CC} Test Condition, Power Down Mode All other pins are disconnected. V_{CC} = 2V to 5.5V

NOTE:

* Ports 1.6 and 1.7 should be connected to V_{CC} through resistors of sufficiently high value such that the sink current into these pins does not exceed the I_{OL1} specifications.

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EPROM CHARACTERISTICS

The 87C528 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/$\overline{PROG}$ pulses

The 87C528 contains two signature bytes that can be read and used by an EPROM programming system to identify the device The signature bytes identify the device as an 87C528 manufactured by Philips.

Table 3 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the lock bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 13 and 14 Figure 15 shows the circuit configuration for normal program memory verification

Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 13 Note that the 87C528 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers

The address of the EPROM location to be programmed is applied to ports 1, 2 and 3, as shown in Figure 13 The code byte to be programmed into that location is applied to port 0 RST, $\overline{PSEN}$ and pins of ports 2 and 3 specified in Table 3 are held at the 'Program Code Data' levels indicated in Table 3 The ALE/$\overline{PROG}$ is pulsed low 25 times as shown in Figure 14.

To program the encryption table, repeat the 25 pulse programming sequence for addresses 0 through 3FH, using the'"Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the lock bits, repeat the 25 pulse programming sequence using the 'Pgm Lock Bit' levels After one lock bit is programmed, further programming of the code memory and encryption table is disabled. However, the other lock bit can still be programmed.

Note that the $\overline{EA}$/V_{PP} pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot

Program Verification

If lock bit 2 has not been programmed, the on-chip program memory can be read out for program verification The address of the program memory locations to be read is applied to ports 1, 2 and 3 as shown in Figure 15 The other pins are held at the 'Verify Code Data' levels indicated in Table 3 The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

(030H) = 15H indicates manufactured by Philips

(031H) = 97H indicates 87C528

Program Lock Bits

The 87C528 has 3 programmable lock bits that will provide different levels of protection for the on-chip code and data (see Table 4)

Erasing the EPROM also erases the encryption array and the program lock bits, returning the part to full functionality.

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 3, and which satisfies the timing specifications, is suitable.

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345-5, or equivalent

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-sec/cm^2 Exposing the EPROM to an ultraviolet lamp of 12,000uW/cm^2 rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient

Erasure leaves the array in an all 1s state.

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Table 3. EPROM Progamming Modes

MODE	RST	PSEN	ALE/PROG	EA/V_{PP}	P2.7	P2.6	P3.7	P3.6
Read signature	1	0	1	1	0	0	0	0
Program code data	1	0	0*	V_{PP}	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Pgm encryption table	1	0	0*	V_{PP}	1	0	1	0
Pgm lock bit 1	1	0	0*	V_{PP}	1	1	1	1
Pgm lock bit 2	1	0	0*	V_{PP}	1	1	0	0
Pgm lock bit 3	1	0	0*	V_{PP}	0	1	0	1

NOTES:
'0' = Valid low for that pin, '1' = valid high for that pin.
V_{PP} = 12.75V ±0.25V.
V_{CC} = 5V±10% during programming and verification.
* ALE/PROG receives 25 programming pulses while V_{PP} is held at 12.75V. Each programming pulse is low for 100µs (±10µs) and high for a minimum of 10µs.

Table 4.

PROGRAM LOCK BITS[1,2]				
	LB1	LB2	LB3	PROTECTION DESCRIPTION
1	U	U	U	No Program Lock features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is jumped and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, external execution is disabled. Internal data RAM is not accessable.

NOTES:
1. P – programmed. U – unprogrammed.
2. Any other combination of the lock bits is not defined.

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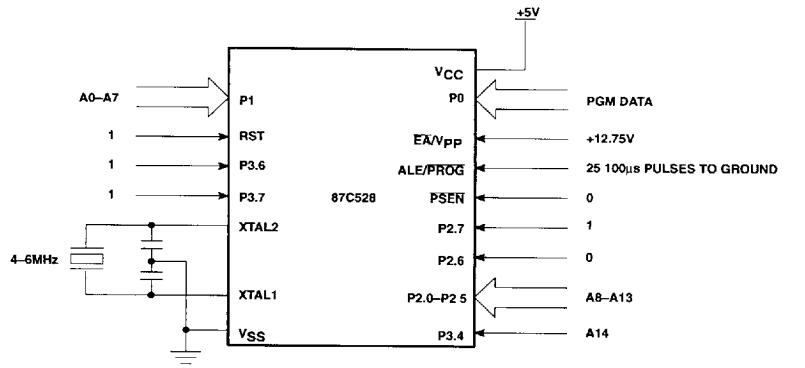

Figure 13. Programming Configuration

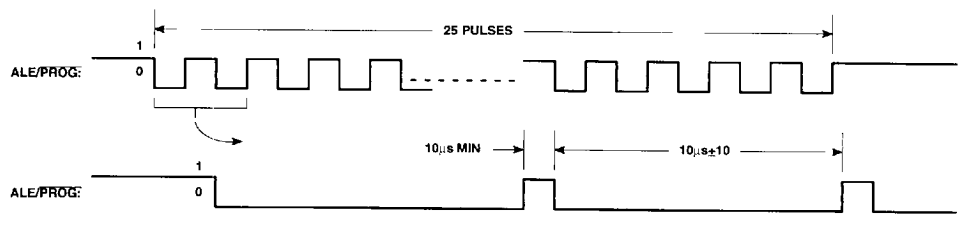

Figure 14. PROG Waveform

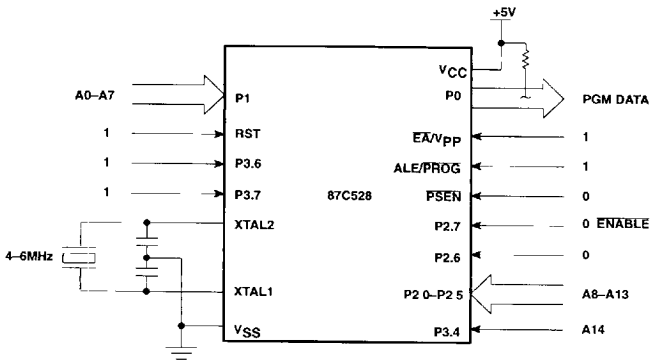

Figure 15. Program Verification

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EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_{amb} = 21°C to +27°C, V_{CC} = 5V±10%, V_{SS} = 0V (See Figure 16)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{PP}	Programming supply voltage	12.5	13.0	V
I_{PP}	Programming supply current		50	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
t_{AVGL}	Address setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHAX}	Address hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHDX}	Data hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) high to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} setup to $\overline{PROG}$ low	10		µs
t_{GHSL}	V_{PP} hold after $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ width	90	110	µs
t_{AVQV}	Address to data valid		$48t_{CLCL}$	
t_{ELQZ}	$\overline{ENABLE}$ low to data valid		$48t_{CLCL}$	
t_{EHQZ}	Data float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHGL}	$\overline{PROG}$ high to $\overline{PROG}$ low	10		µs

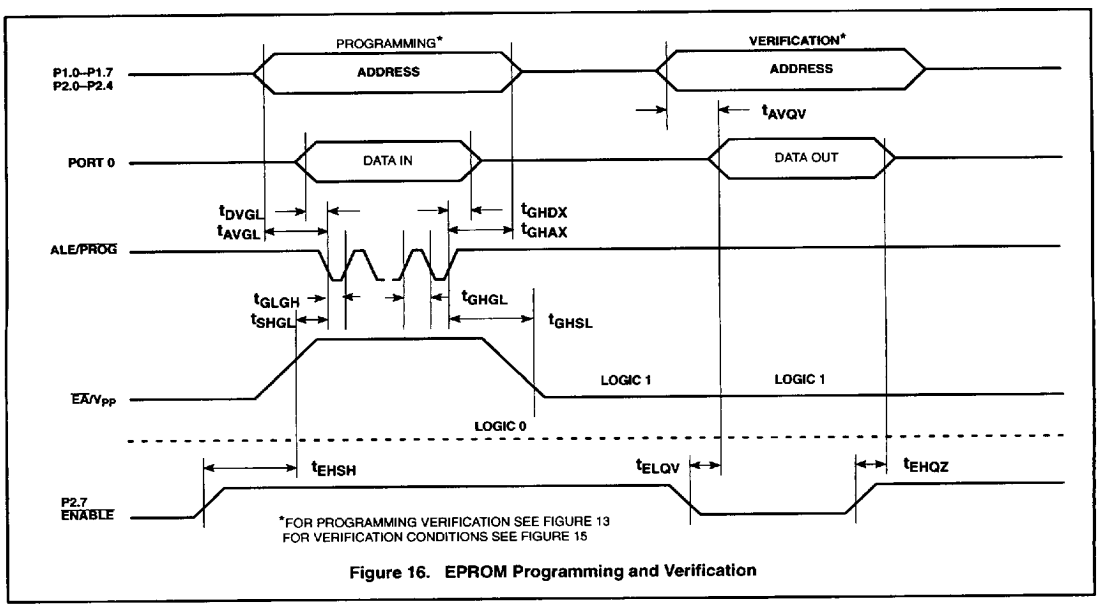

Figure 16. EPROM Programming and Verification

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

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