NEC

MOS INTEGRATED CIRCUIT

μPD29F800L

8 M-BIT CMOS 3.0 V-ONLY FLASH MEMORY
1 M-WORD BY 8-BIT (BYTE MODE) / 512 K-WORD BY 16-BIT (WORD MODE)

Description

The μPD29F800L is an electrically programmable/erasable high-speed 3.0 V-only flash memory with a 8,388,608-bit configuration.

The word organization is selectable (BYTE mode: 1,048,576 words by 8 bits, WORD mode: 524,288 words by 16 bits). It possesses an automatic single Byte/Word program function and an automatic block erase function that are effected by command register input.

This memory consists of 19 blocks: one protection block (8 K word/16 K byte), two condition blocks (4 K word/8 K byte by 2 blocks), and sixteen main blocks (16 K word/32 K byte by 1 block, 32 K word/64 K byte by 15 blocks).

The μPD29F800L comes in two types: the type T with the protection block having a protect funciton located at the top address and the type B with the protection block having a protect function located at the bottom address.

In addition, a sleep mode in which the power dissipation is lowered to 1.0 μA or less is also provided.

The μPD29F800L is packed in 44-pin SOP and 48-pin TSOP (I) (12 × 20 mm).

Features

- 1,048,576 words by 8 bit
  524,288 words by 16 bit
- Two types of protection block locations
  type T : protection block at the top address
  type B : protection block at the bottom address
- Fast access time : 120, 150 ns (MAX.)
- Fast program/erase time.
  Byte program : 9 μs (TYP.)
  Word program : 11 μs (TYP.)
- Block erase
  Protection block : 1.0 s (TYP.)
  Condition block : 1.0 s (TYP.)
  Main block : 1.0 s (TYP.)
- Command register input
- Automatic program function
- Hardware reset
- Ready (/Busy) output (RY (/BY))
- Data polling and toggle bit
- Automatic erase function
- Functions for automatic erasure:
  Erase suspend and resume functions
- Minimum number of repetitions for program/erase:
  100,000 times
- Directly drive TTL or CMOS
- Low power dissipation
  Reset mode : 5.0 μA (MAX.)
  Standby mode : 5.0 μA (MAX.)
  Operating mode : 35 mA (MAX.)
- Voltage range
  V_{CC}: 3.0 V + 20 %/-10 % (Extend voltage)

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The mark ★ shows major revised points.

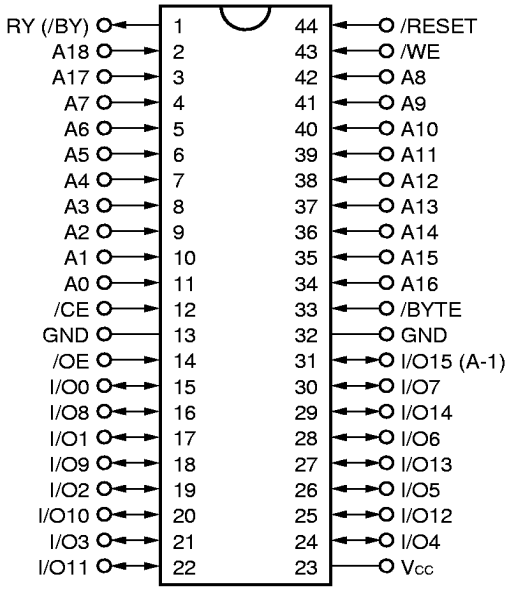
Ordering Information

Part number	Access time (MAX.)	Protection block	Package
μPD29F800LGX-B12T	120 ns	The top address	44-pin plastic SOP (600 mil)
μPD29F800LGX-B15T	150 ns		
μPD29F800LGX-B12B	120 ns	The bottom address	
μPD29F800LGX-B15B	150 ns		
μPD29F800LGZ-B12T-MJH	120 ns	The top address	48-pin plastic TSOP (I) (12 × 20 mm) (Normal bent)
μPD29F800LGZ-B15T-MJH	150 ns		
μPD29F800LGZ-B12B-MJH	120 ns	The bottom address	
μPD29F800LGZ-B15B-MJH	150 ns		
μPD29F800LGZ-B12T-MKH	120 ns	The top address	48-pin plastic TSOP (I) (12 × 20 mm) (Reverse bent)
μPD29F800LGZ-B15T-MKH	150 ns		
μPD29F800LGZ-B12B-MKH	120 ns	The bottom address	
μPD29F800LGZ-B15B-MKH	150 ns		

Remark For the address locations of the blocks, see the memory maps in **Erase Block Layout**.

Pin Configuration (Marking Side)

44-pin plastic SOP (600 mil)
μPD29F800LGX-xxxT
μPD29F800LGX-xxxB



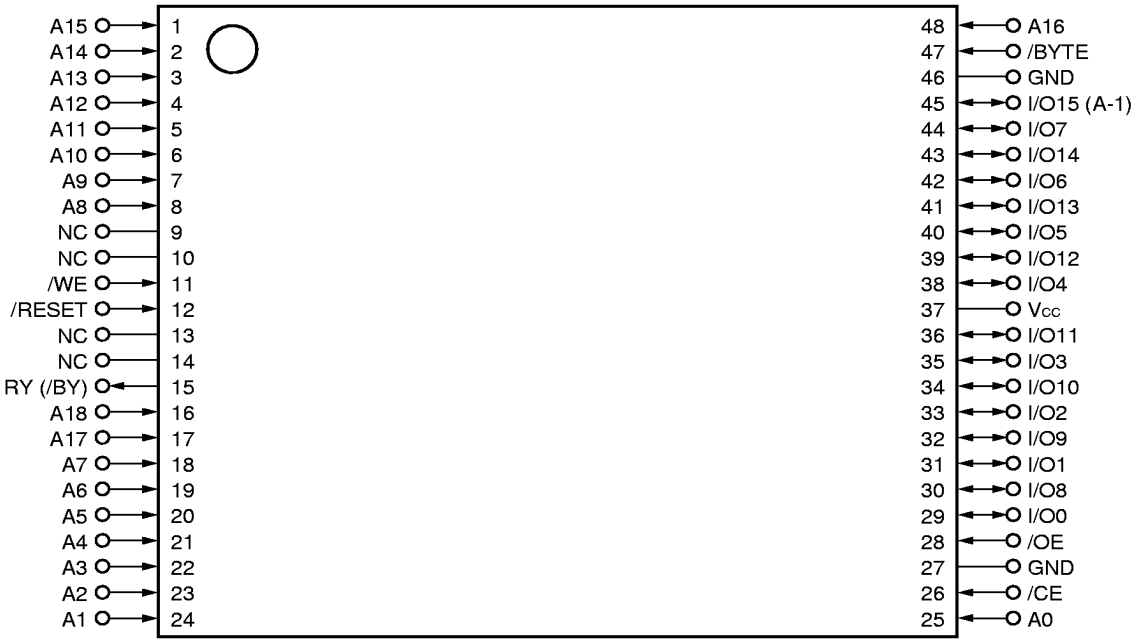
A0 to A18	: Address inputs
I/O0 to I/O15	: Data inputs/outputs
/CE	: Chip enable
/WE	: Write enable
/OE	: Output enable
/RESET	: Hardware reset input
/BYTE	: Byte enable
V_{CC}	: Supply voltage
GND	: Ground
NC[Note]	: No connection
RY (/BY)	: Ready (/Busy) output

Note Some signals can be applied because this pin is not connected to the inside of the chip.

48-pin plastic TSOP (I) (12 × 20 mm) (Normal bent)

μPD29F800LGZ-xxxT-MJH

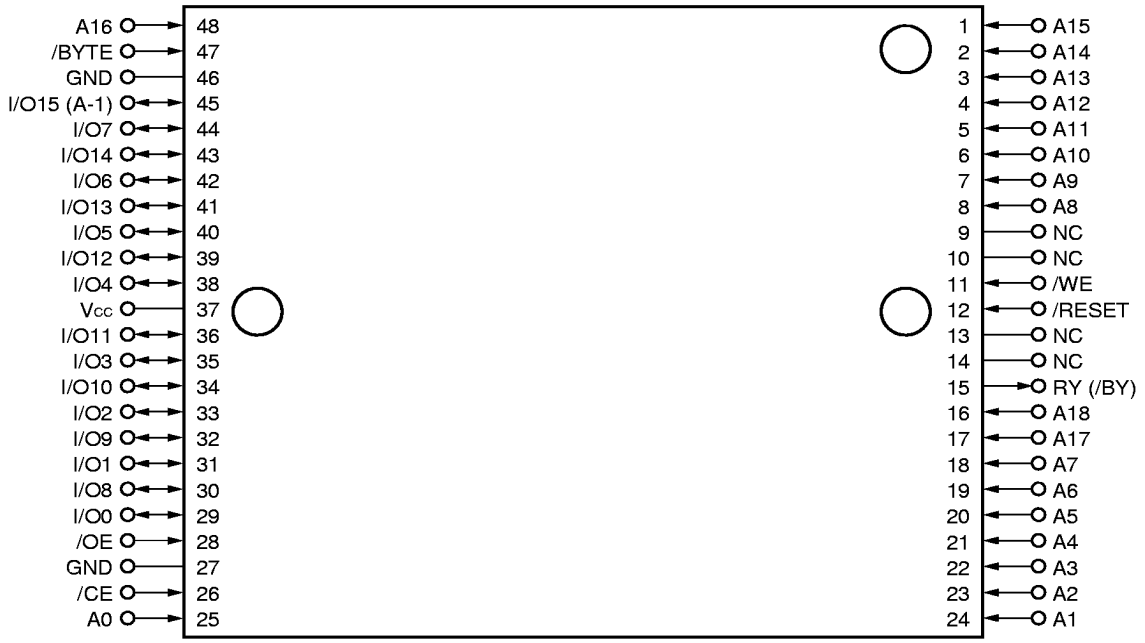
μPD29F800LGZ-xxxB-MJH



48-pin plastic TSOP (I) (12 × 20 mm) (Reverse bent)

μPD29F800LGZ-xxxT-MKH

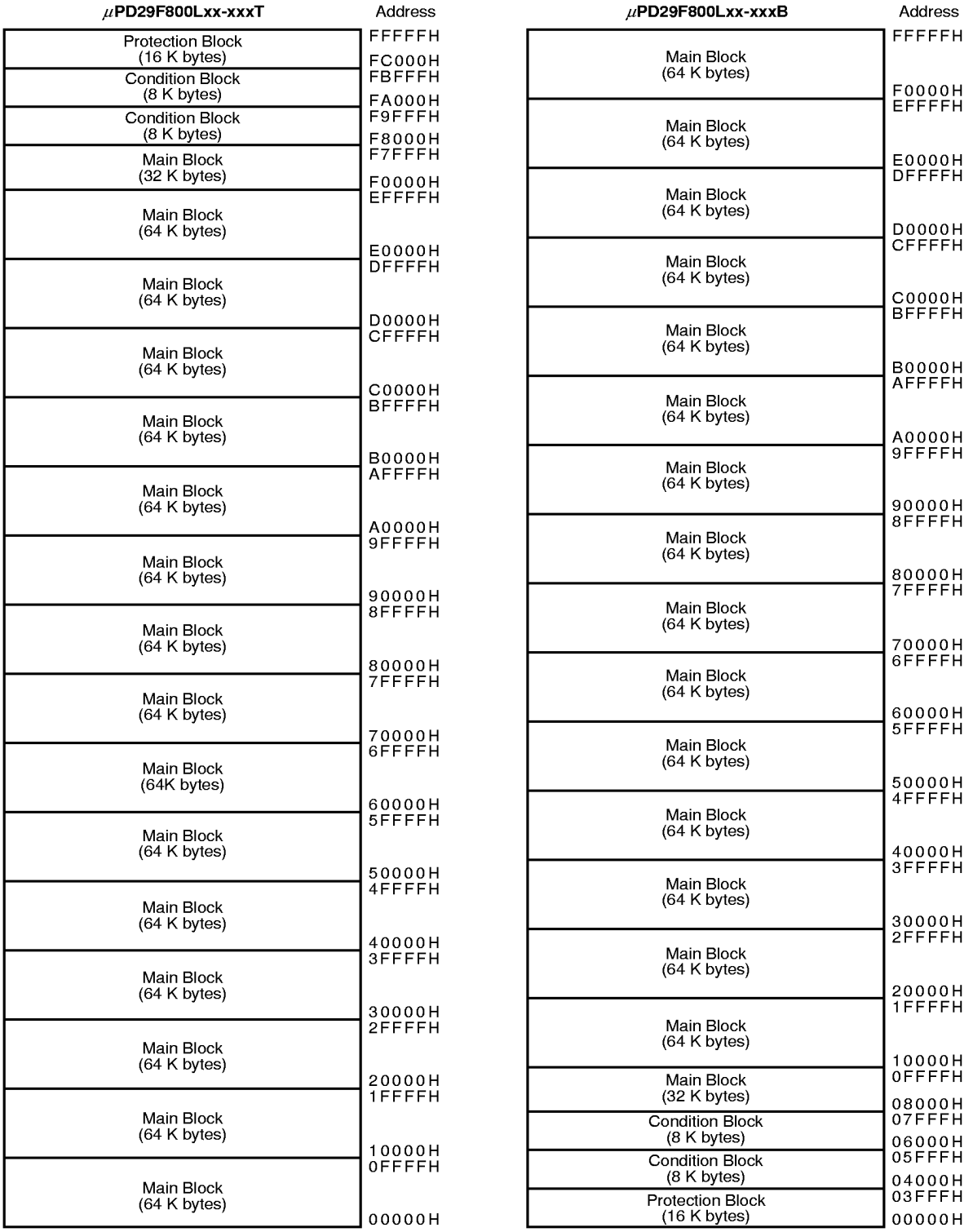
μPD29F800LGZ-xxxB-MKH



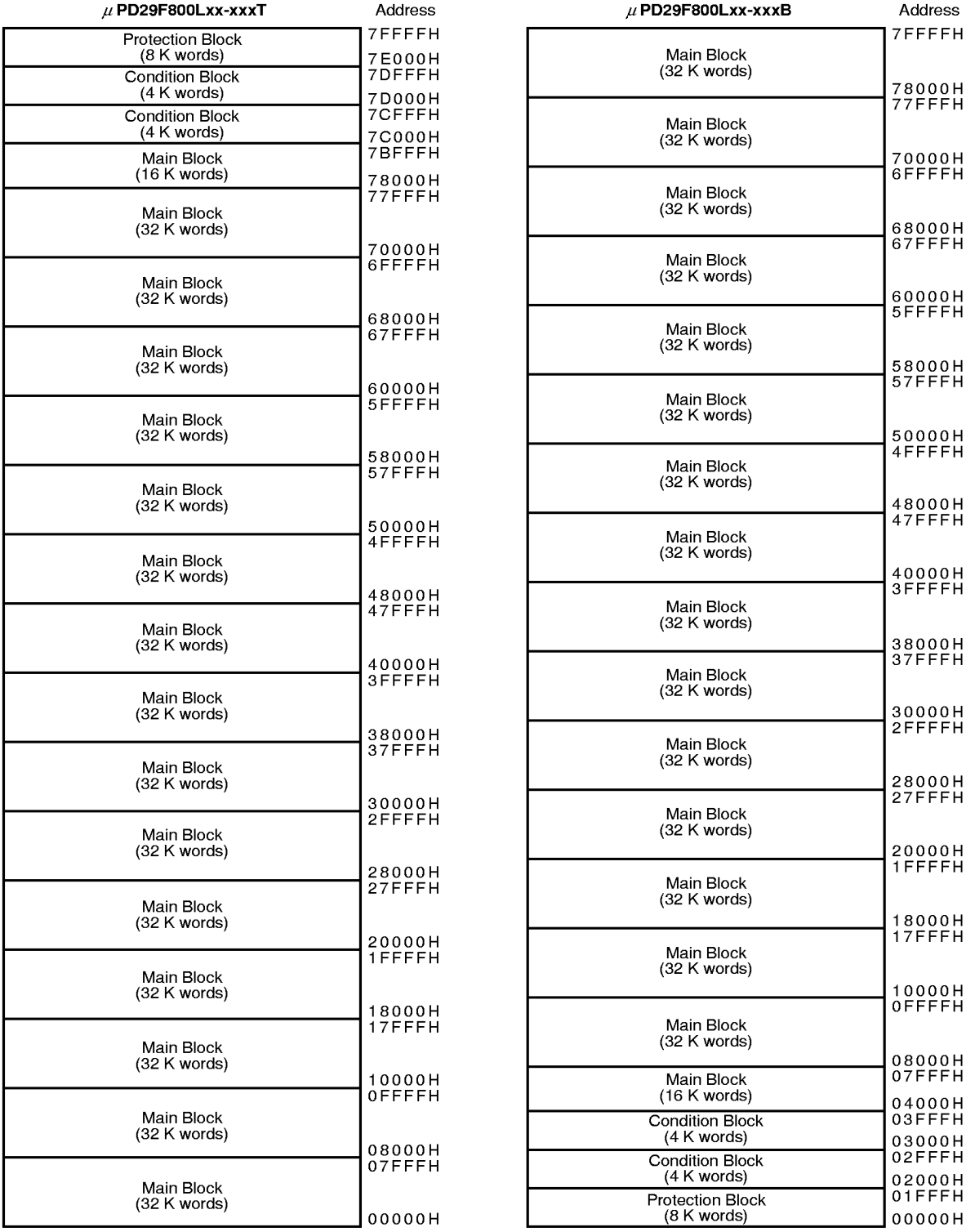
Input/Output Pin Functions

Pin Name	Inout/Output	Function
A0-A18	Input	Address inputs. Word Mode: 19 bit address input. Byte Mode: 19 bit of the top address input of 20 bit address (A-1 (The bottom address) is I/O15).
A9	Input	Address input. When A9 is at 11.5 V to 12.5 V, the signature mode is accessed. During this mode A0 decodes between the manufacturer and device IDs. A0 = "L": Manufacturer ID, A0 = "H": Device ID.
I/O0-I/O15	Input/Output	Data inputs/outputs. Word Mode: 16 bit data input/output. Byte Mode: I/O0-7 is 8 bit data input/output (I/O15 is A-1 (The bottom address)). I/O8-14 are disabled.
/CE	Input	Chip enable signal. High level input: Standby mode
/OE	Input	Output enable sinal. High level input: Output disable mode
/WE	Input	Write enable signal. Low level input: Block Erase/Program and Command input
/RESET	Input	Hardware reset input. Low level input: Reset mode
/BYTE	Input	The pin for switching word mode and byte mode. High level input: Word mode (512 K × 16 bit) Low level input: Byte mode (1 M × 8 bit)
RY (/BY)	Output	The pin for indicating that automatic erase (or automatic program) operation is either in progress or have been completed. This pin is an open-drain output pin. Low level output: The device is busy with automatic erase (or automatic program) operation. High level output: The device is ready for new operations, in the erase suspend mode or in reset mode.
V_{CC}	–	Supply voltage
GND	–	Ground
NC	–	No connecton: Not internally connected. (The signal can be connected.)

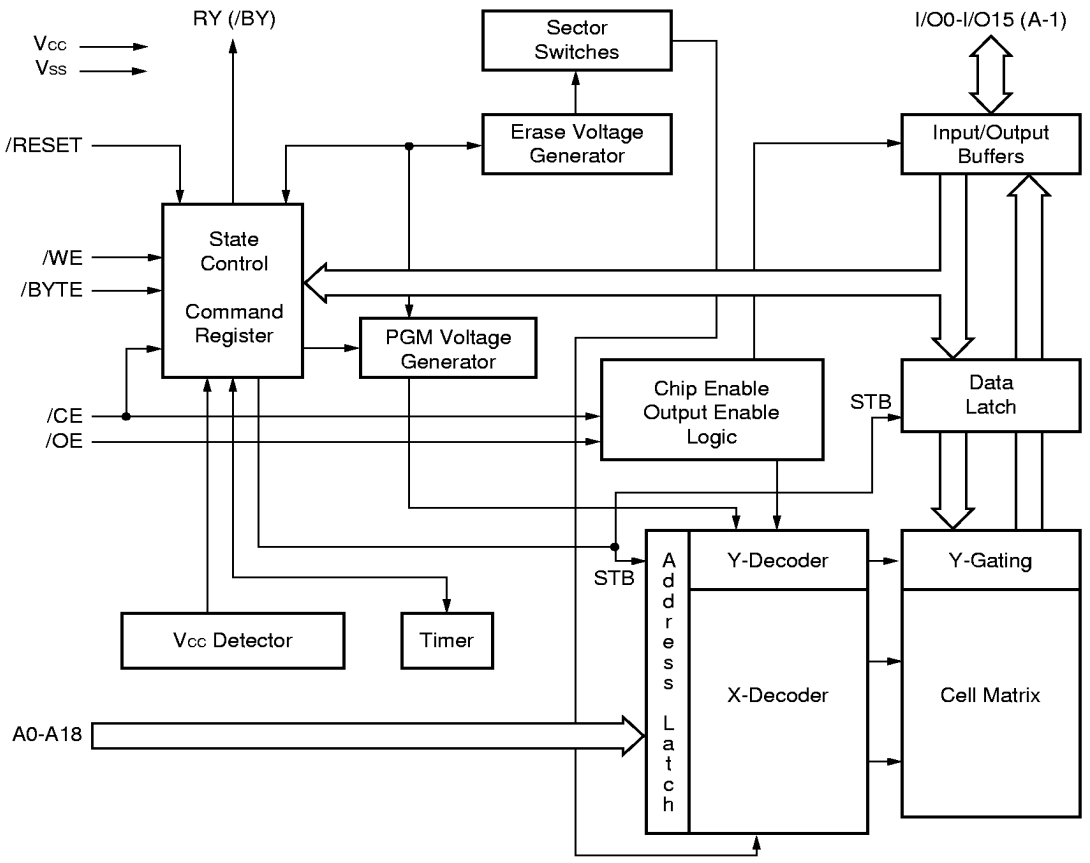
Erase Block Layout (Byte Mode)



Erase Block Layout (Word Mode)



Block Diagram



Operation Mode

Word Mode (Byte pin = V_{IH})

Mode \ Pin Name	/RESET	/CE	/OE	/WE	A9	A6	A1	A0	I/O0-I/O15
Product ID code, Manufacturer code Note	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_H	V_{IL}	V_{IL}	V_{IL}	ID
Product ID code, Device code Note	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_H	V_{IL}	V_{IL}	V_{IH}	ID
Read	V_{IH}	V_{IL}	V_{IL}	V_{IH}	A9	A6	A1	A0	Data output
Standby	V_{IH}	V_{IH}	×	×	×	×	×	×	Hi-Z
Output disable	V_{IH}	V_{IL}	V_{IH}	V_{IH}	×	×	×	×	Hi-Z
Write	V_{IH}	V_{IL}	V_{IH}	V_{IL}	A9	A6	A1	A0	Data input
Enable sector protect	V_{IH}	V_{IL}	V_H	Pulse/V_{IH}	V_H	V_{IL}	V_{IH}	V_{IL}	Code
Verify sector protect	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_H	V_{IL}	V_{IH}	V_{IL}	Code
Temporary sector unprotect	V_H	×	×	×	×	×	×	×	×
Reset	V_{IL}	×	×	×	×	×	×	×	Hi-Z

Note Manufacturer and device codes may also be accessed via a command register write sequence. Please refer to Command Definition.

Remark V_H = 12.0 V ± 0.5 V
× : Don't care (V_{IH} or V_{IL})
See DC characteristics for voltage levels.

ID = Data Read from Location address during Device Identification.
0010H : Manufacturer code
22DAH : Device code for Type T
225BH : Device code for a Type B

Byte Mode (Byte pin = V_{IL})

Mode \ Pin Name	/RESET	/CE	/OE	/WE	A9	A6	A1	A0	A-1	I/O0-I/O7	I/O8-I/O15
Product ID code, Manufacturer code Note	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_H	V_{IL}	V_{IL}	V_{IL}	×	ID	Hi-Z
Product ID code, Device code Note	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_H	V_{IL}	V_{IL}	V_{IH}	×	ID	Hi-Z
Read	V_{IH}	V_{IL}	V_{IL}	V_{IH}	A9	A6	A1	A0	×	Data output	Hi-Z
Standby	V_{IH}	V_{IH}	×	×	×	×	×	×	×	Hi-Z	Hi-Z
Output disable	V_{IH}	V_{IL}	V_{IH}	V_{IH}	×	×	×	×	×	Hi-Z	Hi-Z
Write	V_{IH}	V_{IL}	V_{IH}	V_{IL}	A9	A6	A1	A0	×	Data input	Hi-Z
Enable sector protect	V_{IH}	V_{IL}	V_H	Pulse/V_{IH}	V_H	V_{IL}	V_{IH}	V_{IL}	×	Code	Hi-Z
Verify sector protect	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_H	V_{IL}	V_{IH}	V_{IL}	×	Code	Hi-Z
Temporary sector unprotect	V_H	×	×	×	×	×	×	×	×	×	Hi-Z
Reset	V_{IL}	×	×	×	×	×	×	×	×	Hi-Z	Hi-Z

Note Manufacturer and device codes may also be accessed via a command register write sequence. Please refer to Command Definition.

Remark V_H = 12.0 V ± 0.5 V
× : Don't care (V_{IH} or V_{IL})
See DC characteristics for voltage levels.

ID = Data Read from Location address during Device Identification.
10H : Manufacturer code
DAH : Device code for a Type T
5BH : Device code for a Type B

Operation Mode (Command Mode)

Command Sequence		Bus Cycles	First bus Write cycle		Second bus write cycle		Third bus write cycle		Fourth bus write cycle		Fifth bus write cycle		Sixth bus write cycle	
			Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Reset/Read		1	xxxxH	F0H	–	–	–	–	–	–	–	–	–	–
Read product ID code	Word	4	5555H	AAH	2AAAH	55H	5555H	90H	IA	ID	–	–	–	–
	Byte		AAAAH		5555H		AAAAH							
Program	Word	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD	–	–	–	–
	Byte		AAAAH		5555H		AAAAH							
Chip erase	Word	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
	Byte		AAAAH		5555H		AAAAH		AAAAH		5555H		AAAAH	
Sector erase	Word	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	EA	30H
	Byte		AAAAH		5555H		AAAAH		AAAAH		5555H			
Sector erase suspend	Word/ Byte	1	xxxxH	B0H	–	–	–	–	–	—	–	–	–	–
Sector erase Resume	Word/ Byte	1	xxxxH	30H	–	–	–	–	–	–	–	–	–	–

Remark x: V_{IL} or V_{IH}

EA = Block Address of Memory Location to be erased.
PA = Address of Memory Location to be programmed.
PD = Data to be programmed at Location PA.
IA = Identifier Address
ID = Identifier Data

(Word mode)
0010H : Manufacturer code
22DAH : Device code for a Type T
225BH : Device code for a Type B

(Byte mode)
10H : Manufacturer code
DAH : Device code for a Type T
5BH : Device code for a Type B

Hardware Sequence Flags

	Status		I/O7	I/O6	I/O5	I/O3	I/O2	RY(/BY)
In progress	Programming		/I/O7	Toggle	0	0	1	0
	Auto erase		0	Toggle	0	1	Toggle	0
	Erase suspend	Erase sector	1	1	0	0	Toggle	1
		Non erase sector	DATA	DATA	DATA	DATA	DATA	1
	Program in suspend		/I/O7	Toggle	0	0	1	0
Exceeded time limits	Programming		/I/O7	Toggle	1	0	1	0
	Auto erase		0	Toggle	1	1	N/A	0
	Program in erase suspend		/I/O7	Toggle	1	0	N/A	0

/DATA Polling (I/O7)

/DATA Polling supports system software by indicating the precise end of write or erase cycles.
On this support, the next write or erase cycle can be started as soon as previous cycle has completed.

• How to use /DATA Polling

<Write Operation>

(1) After writing data by write operation, fix /WE = "H".
(See /DATA polling During Program or Erase Operation Timing Chart.)

(2) Compare the read data from I/O7 with just before written data.

(3) In coincidence with the both data, μPD29F800L will complete its write cycle. Then start the next cycle. In case of still in progress, the data on I/O7 is inverted just before written data.

<Erase Operation>

(1) After setting erase command by write operation, fix /WE = "H".
(See /DATA polling During Program or Erase Operation Timing Chart.)

(2) If the read data on I/O7 is "1", μPD29F800L has completed its erase cycle, and the other means erase cycle is in progress.

Toggle Bit Function (I/O6)

Toggle bit function supports system software by indicating the precise end of write or erase cycles, too.

• How to use Toggle bit function

(1) After writing data by command write operation, fix /WE = "H".
(See Toggle Bit During Program /Erase Algorithm Operation Timing Chart.)

(2) Watch the read data on I/O6.

(3) If the write or erase operation is in progress, the read data from I/O6 will toggle on every reading. And if the operation has completed, the read data will stop toggling.

Exceed Timing Limit (I/O5)

Exceed timing limit function supports system software by indicating the write or erase time has exceeded the specific limits.

• How to use Exceed Timing Limit function

(1) After writing data by command write operation, fix /WE = "H".

(2) Watch the read data on I/O5.

(3) If the write or erase operation has not successfully completed, I/O5 will indicate "1".

Sector Erase Timer (I/O3)

Sector erase timer function supports system software by indicating the acceptance of sequential sector erase command write.

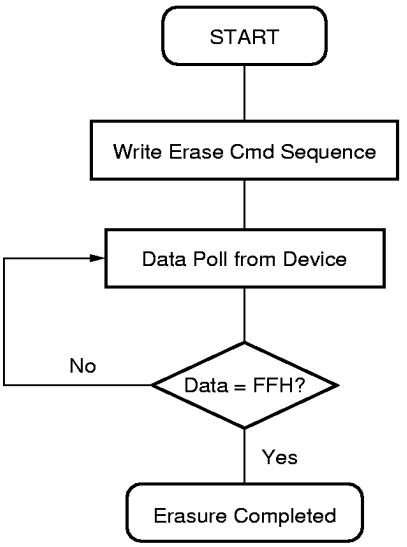
• How to use Sector Erase Timer function

(1) After writing initial sector erase command sequence, watch the data on I/O3.

(2) If the data on I/O3 is "1", μPD29F800L will not accept subsequent command until the erase operation is completed as indicated by Data Polling (I/O7) or Toggle Bit (I/O6).

(3) And if the data on I/O3 is "0", μPD29F800L will be able to accept subsequent command.

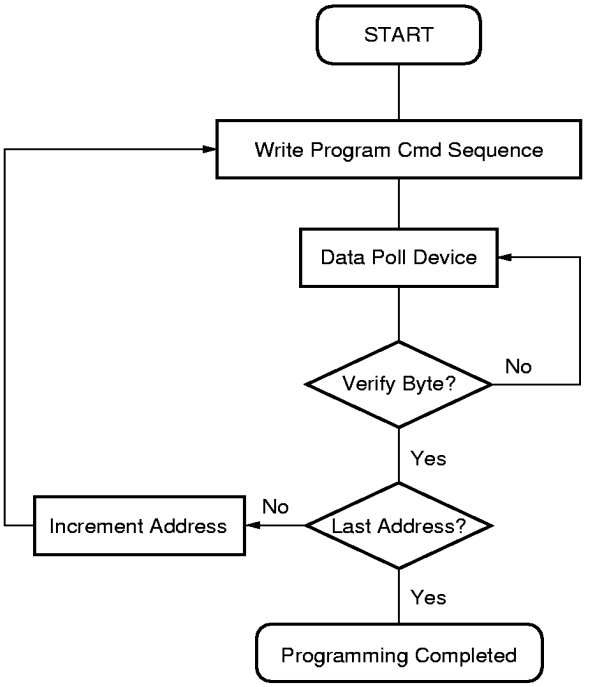
Erase Flowchart



Erase Algorithm

Bus operation	Command sequence	Comments
Standby		
Write	Erase	
Read		/DATA polling to verify erasure
Standby		Compare output to FFH.

Program Flowchart



Program Algorithm

Bus operation	Command sequence	Comments
Standby[Note]		
Write	Program	Valid address/data
Read		/DATA polling to verify programming
Standby[Note]		Compare data output to data expected

Note Device is either powered-down, erase inhibit, or program inhibit.

Electrical Characteristics (Preliminary)

Absolute Maximum Ratings

Parameter	Symbol	Test conditions	Ratings	Unit
Supply voltage	V_{CC}	with respect to GND	–0.5 to +5.5	V
Input voltage	V_I	with respect to GND	–0.5[Note] to +5.5	V
	V_I	with respect to GND, A9, /RESET, /OE	–0.5[Note] to +13.5	
Output voltage	V_O	with respect to GND	–0.5[Note] to +5.5	V
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–65 to +125	°C
Storage temperature (under Bias)	T_{bias}		0 to +70	°C

Note V_I, V_O = –2.0 V (MIN.) for pulse width ≤ 20 ns.

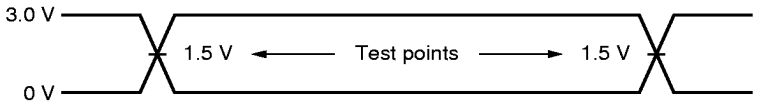
Caution Exposing the device to stress above those listed in absolute maximum ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this characteristics. Exposure to absoulte maximum rating conditions for extended periods may affect device reliability.

Capacitance (T_A = 25 °C, f = 1 MHz)

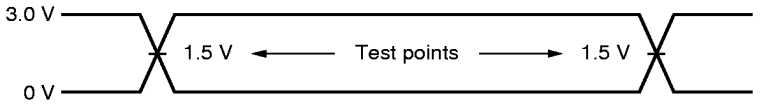
Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	V_{IN} = 0 V		6.0	7.5	pF
Output capacitance	C_O	V_{OUT} = 0 V		8.5	12.0	pF

AC Test Conditions

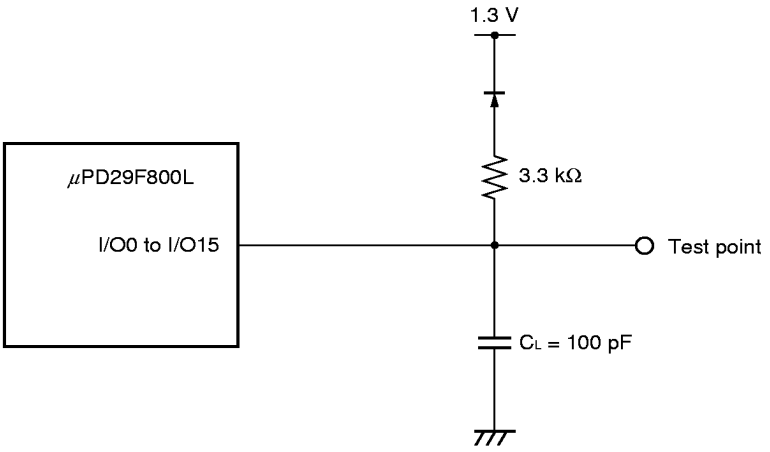
Input Waveform (Rise/Fall time ≤ 10 ns)



Output Waveform



Output Load



Remark C_L includes capacitances of the probe and jig, and stray capacitances.

Read Operation

Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	2.7	3.0	3.6	V
High level input voltage	V_{IH}	2.0		V_{CC} +0.5 Note1	V
Low level input voltage	V_{IL}	–0.5 Note2		+0.8	V
Operating ambient temperature	T_A	0		+70	°C

Notes **1.** $V_{IH} = V_{CC}$ +1.0 V (MAX.) for pulse width ≤ 20 ns

2. V_{IL} = –1.0 V (MIN.) for pulse width ≤ 20 ns

DC Characteristics (Recommended operating conditions unless otherwise noted)

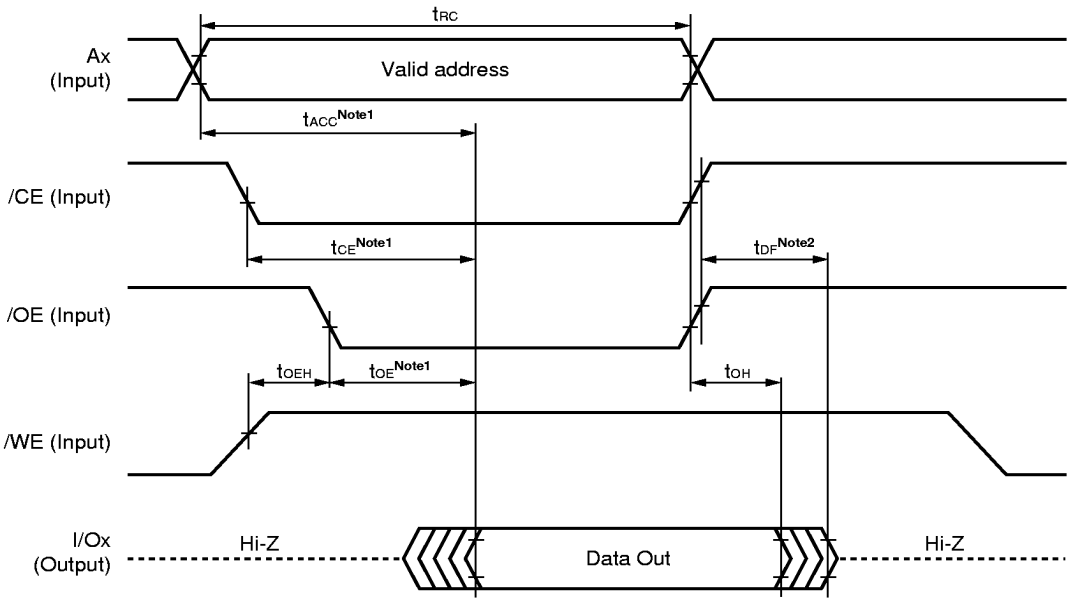
Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
High level output voltage	V_{OH1}	I_{OH} = –2.0 mA, $V_{CC} = V_{CC}$ (MIN.)	2.4			V
	V_{OH2}	I_{OH} = –2.0 mA, $V_{CC} = V_{CC}$ (MIN.)	0.85 V_{CC}			V
		I_{OH} = –100 μA, $V_{CC} = V_{CC}$ (MIN.)	V_{CC}–0.4			
Low level output voltage	V_{OL1}	I_{OL} = 4.0 mA, $V_{CC} = V_{CC}$ (MIN.)			0.45	V
	V_{OL2}	I_{OL} = 5.8 mA, $V_{CC} = V_{CC}$ (MIN.)			0.45	
Output leakage current	I_{LO}	v_{OUT} = 0 V to V_{CC}, /OE = V_{IH}	–1.0		+1.0	μA
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}	–1.0		+1.0	μA
V_{CC} supply current	I_{CCA1}	V_{IN} = V_{IH}/V_{IL} fixed			35	mA
	I_{CCA2}	I_{OUT} = 0 mA, /CE = V_{IL}, minimum cycle time			45	mA
V_{CC} standby current	I_{CCS1}	/CE = /RESET = V_{IH}, $V_{CC} = V_{CC}$ (MAX.)			250	μA
	I_{CCS2}	/CE ≥ V_{CC} – 0.2 V			5	μA
Reset supply current	I_{CCSLP}	/RESET = GND ± 0.2 V			5	μA

AC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test condition	μPD29F800L-B12		μPD29F800L-B15		Unit
			MIN.	MAX.	MIN.	MAX.	
Address to output delay	t_{ACC}	/CE = /OE = V_{IL}		120		150	ns
/CE to output delay	t_{CE}	/OE = V_{IL}		120		150	ns
/OE to output delay	t_{OE}	/CE = V_{IL}		50		55	ns
/OE or /CE output float delay	t_{DF}	/CE = V_{IL} or /OE = V_{IL}		30		40	ns
Address to output hold	t_{OH}	/CE = /OE = V_{IL}	0		0		ns

Remark t_{DF} is the time from inactivation of /CE or /OE to high-impedance state output.

Read Mode Timing Chart



Notes 1. For read operation, the definition of access time is as follows.

Access time definition	/CE input condition	/OE input conditon
t_{ACC}	before stabilizing address	before (t_{ACC} – t_{OE})
t_{OE}		after (t_{ACC} – t_{OE})
t_{CE}	after stabilizing address	before (t_{CE} – t_{OE})
t_{OE}		after (t_{CE}– t_{OE})

2. t_{DF} is the time from inactivation of /CE or /OE to high-impedance state output.

Program and Erase Operation

Recommended Operating Conditions

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	2.7	3.0	3.6	V
High level input voltage 1	V_{IH}	2.0		V_{CC} +0.5 Note1	V
High level input voltage 2	V_{IH}	11.5		12.5	V
Low level input voltage	V_{IL}	–0.3 Note2		+0.8	V
Operating ambient temperature	T_A	0		+70	°C

Notes 1. $V_{IH} = V_{CC}$ +0.6 V (MAX.) for pulse width ≤ 20 ns

2. V_{IL} = –0.6 V (MIN.) for pulse width ≤ 20 ns

DC Characteristics (Recommended operating conditions unless otherwise noted)

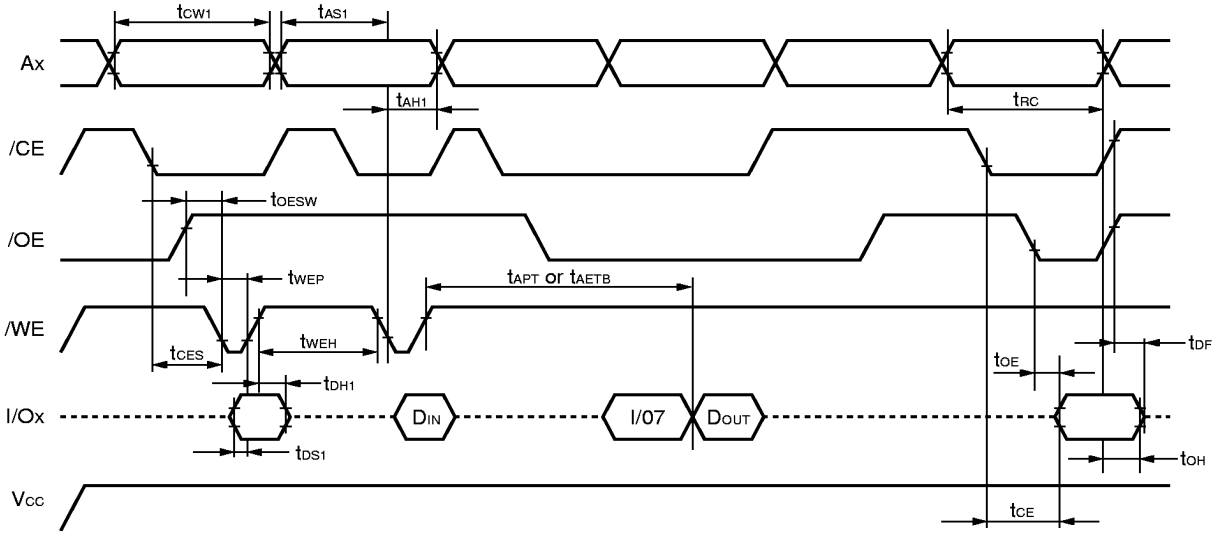
Parameter		Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
High level output voltage		V_{OH1}	I_{OH} = –2.0 mA	2.4			V
		V_{OH2}	I_{OH} = –2.0 mA	0.85 V_{CC}			V
			I_{OH} = –100 μA	V_{CC}–0.4			
Low level output voltage		V_{OL1}	I_{OL} = 4.0 mA, V_{CC} = V_{CC} (MIN.)			0.45	V
		V_{OL2}	I_{OL} = 5.8 mA, V_{CC} = V_{CC} (MIN.)			0.45	
Output leakage current		I_{LO}	V_{OUT} = 0 V to V_{CC}, /OE = V_{IH}	–1.0		+1.0	μA
Input leakage current		I_{LI}	V_{IN} = 0 V to V_{CC}	–1.0		+1.0	μA
V_{CC} supply current	Standby	I_{CCS1}	/CE = /RESET = V_{IH}			250	μA
		I_{CCS2}	/CE = /RESET = V_{CC} ± 0.2 V			5	μA
	Reset	I_{CCSL}	/RESET = GND ± 0.2 V			5	μA
	Read	I_{CCA1}	I_{OUT} = 0 mA, /CE = V_{IL}, V_{IN} = V_{IH}/V_{IL} fixed			35	mA
		I_{CCA2}	I_{OUT} = 0 mA, /CE = V_{IL}, minimum cycle time			45	mA
	Program	I_{CCP}				35	mA
	Erase	I_{CCE}				35	mA
Low V_{CC} lock-out voltage		V_{LKO}		2.3		2.5	V

AC Characteristics (1) (/WE Control) (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	μPD29F800L-B12			μPD29F800L-B15			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Cycle time		t_{CW1}	120			150			ns
Address setup time 1		t_{AS1}	0			0			ns
Address hold time 1		t_{AH1}	50			65			ns
Data input setup time 1		t_{DS1}	50			65			ns
Data input hold time 1		t_{DH1}	0			0			ns
/OE setup time		t_{OES}	0			0			ns
/OE hold time	Read	t_{OEH}	0			0			ns
	Toggle and /DATA polling		10			10			ns
Read recovery time before write		t_{OEHC}	0			0			ns
/CE setup time		t_{CES}	0			0			ns
/CE hold time (V_{IL})		t_{CEL}	0			0			ns
Write pulse width		t_{WEP}	50			65			ns
/WE hold time		t_{WEH}	30			35			ns
Total program time	Word	t_{APT}		11			11		μs
	Byte			9			9		μs
Total erase time		t_{AETB}		1			1		s
V_{CC} setup time		t_{VCS}	50			50			μs
Write Recovery time from RY (/BY)		t_{RB}	0			0			ns
/RESET low time		t_{RL}	500			500			ns
/RESET high time before read		t_{PRHH}	50			50			ns
/RESET to sleep time		t_{SLP}	20			20			μs
Program/Erase valid to RY (/BY) delay		t_{BUSY}	90			90			ns
/CE to /BYTE switching low or high		t_{CBL}/t_{CBH}			5			5	ns
/BYTE switching low to output Hi-Z		t_{BF}	40			40			ns
/BYTE switching high to output valid		t_{BH}	40			40			ns

Remark Duration of the program or erase operation is variable and is calculated in the internal algorithms.

Write Operation Timing Chart

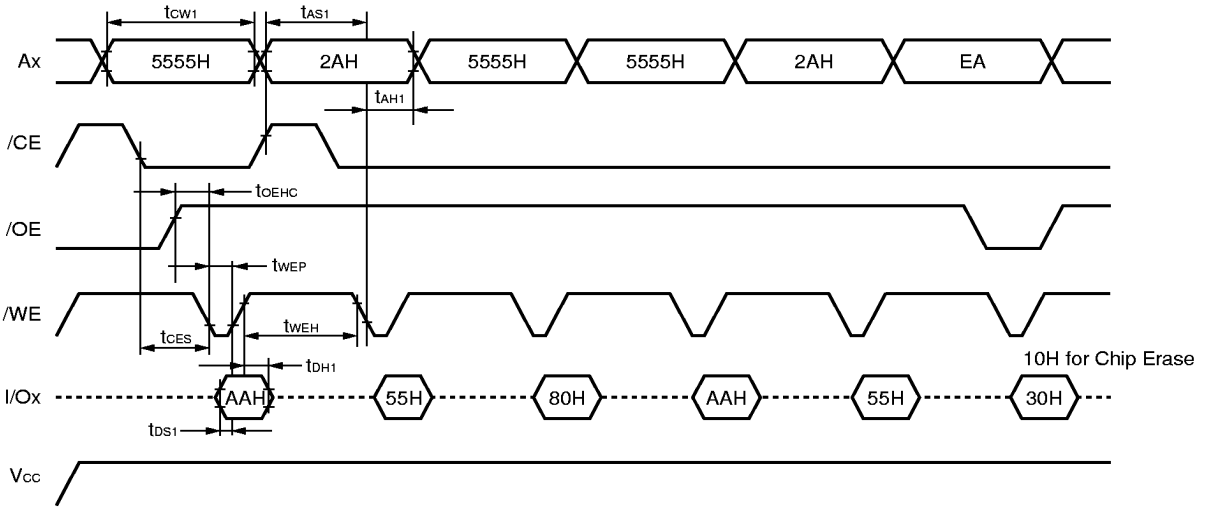


Remarks 1. D_{IN} is DATA input to the device.

2. I/O7 is the output of the complement of the data written to the device.

3. D_{OUT} is the output of the data written to the device.

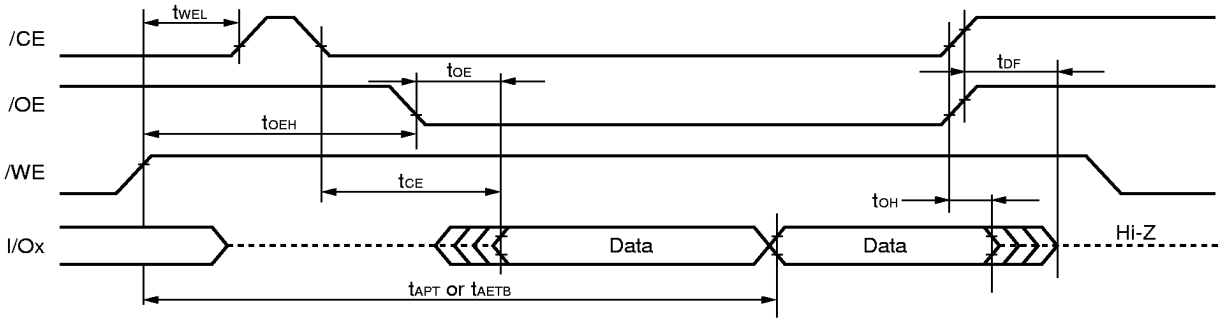
Chip/Sector Erase Operation Timing Chart



Remarks 1. EA is the sector address for Sector Erase. Addresses = Don't care for Chip Erase.

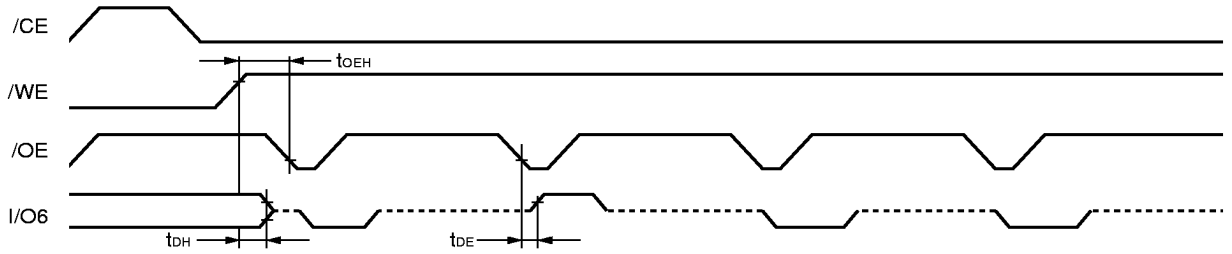
2. These waveforms are for the word mode.

/DATA Polling During Program or Erase Operation Timing Chart



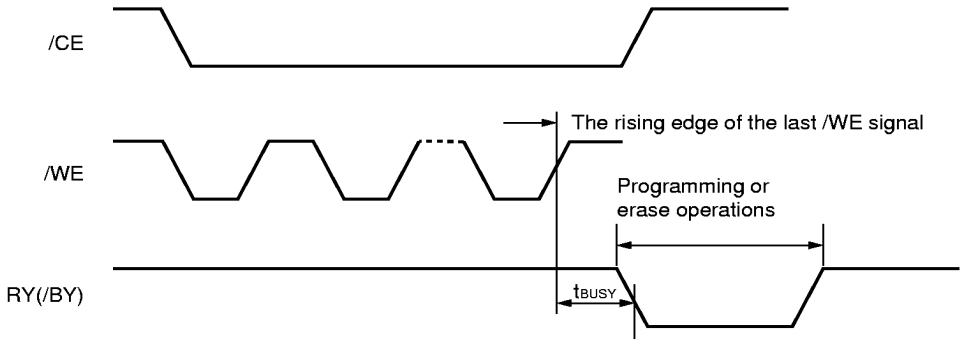
Remark I/O7 = Valid Data (The device has completed the Program or Erase operation).

Toggle Bit During Program/Erase Algorithm Operation Timing Chart

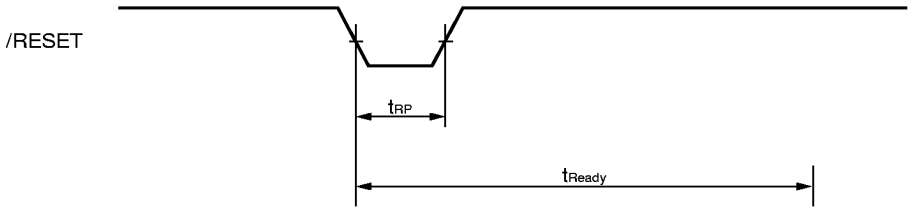


Remark I/O6 stops toggling (The device has completed the Program or Erase operation).

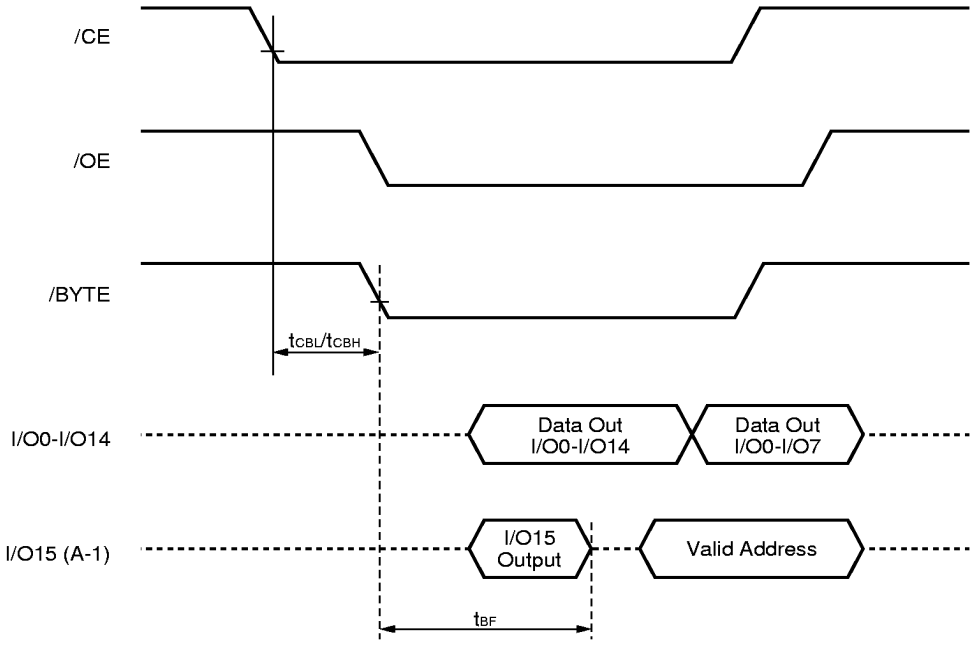
RY (/BY) Timing Chart Program/Erase Operation



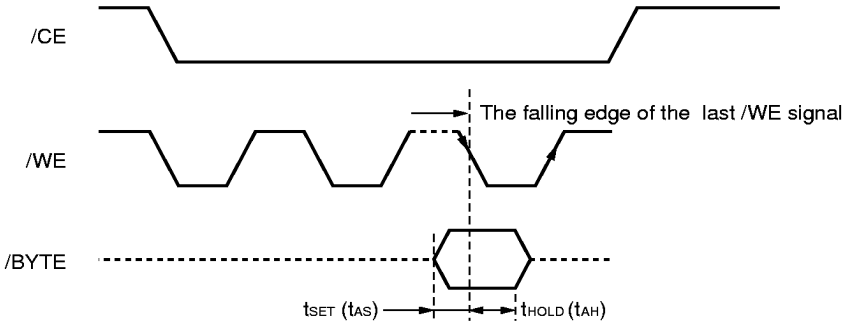
/RESET Timing Chart



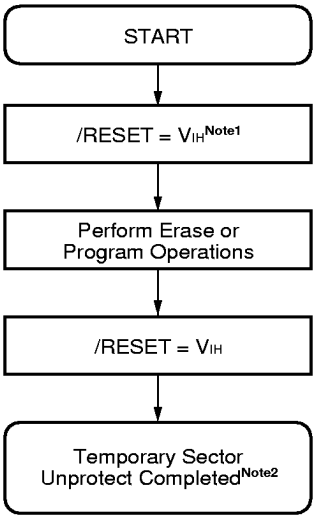
/BYTE Timing Chart for Read Operation



/BYTE Timing Chart for Write Operation



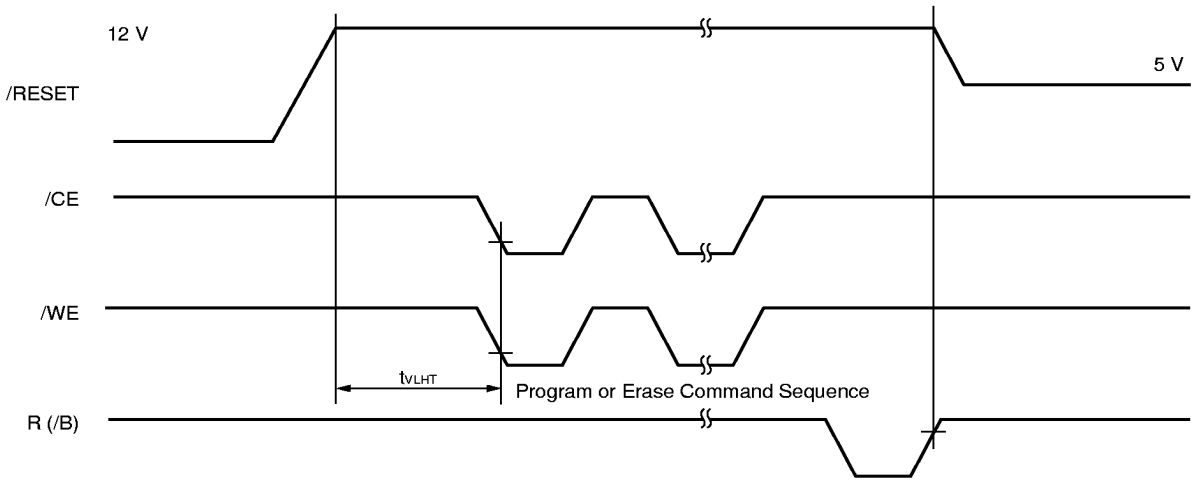
Temporary Sector Unprotect Flowchart



Notes 1. All protected sectors unprotected.

2. All previously protected sectors are protected once again.

Temporary Sector Unprotect Timing Chart

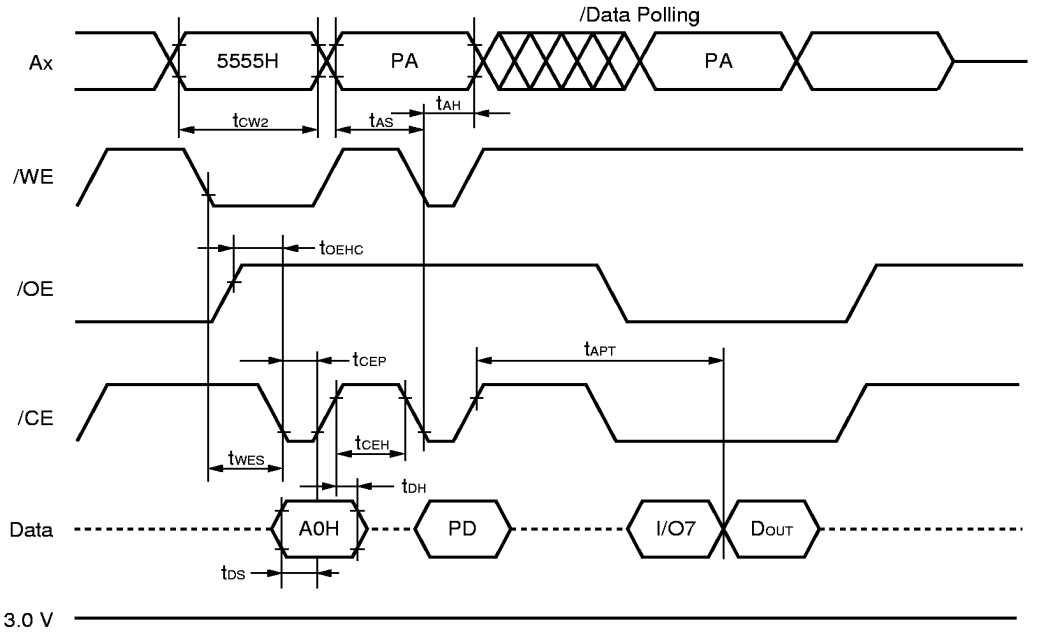


AC Characteristics (2) (/CE Control) (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	μPD29F800L-B12			μPD29F800L-B15			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Write cycle time		t_{CW2}	120			150			ns
Address setup time 2		t_{AS2}	0			0			ns
Address hold time 2		t_{AH2}	50			50			ns
Data input setup time 2		t_{DS2}	50			50			ns
Data input hold time 2		t_{DH2}	0			0			ns
/OE setup time		t_{OES}	0			0			ns
/OE hold time	Read	t_{OEH}	0			0			ns
	Toggle and /DATA polling		10			10			ns
Read recovery time before write		t_{OEHC}	0			0			ns
/WE setup time		t_{WES}	0			0			ns
/WE hold time (V_{IL})		t_{WEL}	0			0			ns
/CE pulse width		t_{CEP}	50			50			ns
/CE pulse width high		t_{CEH}	20			20			ns
Total program time	Word	t_{APT}		11			11		μs
	Byte			9			9		μs
Total erase time[Note]		t_{AETB}		1	10		1	10	s
/BYTE switching low to output Hi-Z		t_{BF}			30			30	ns

Note This does not include the preprogramming time.

Alternate /CE Controlled Write Operation Timing Chart



Remarks 1. PA is address of the memory location to be programmed.

2. PD is data to be programmed at byte address.

3. I/O7 is the output of the complement of the data written to the device.

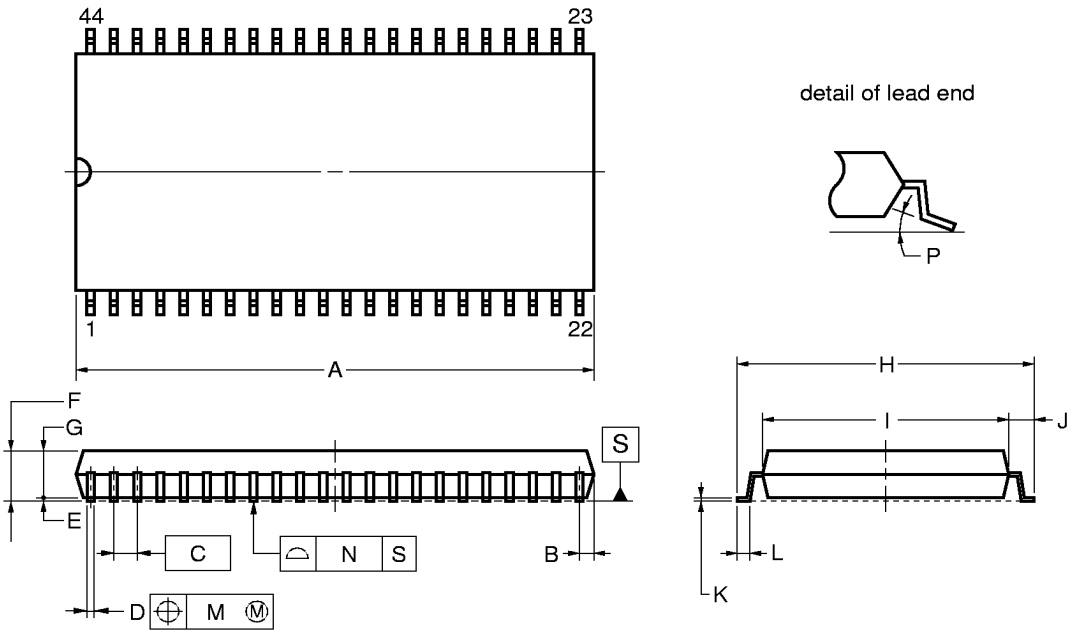
4. D_{OUT} is the output of the data written to the device.

5. Figure indicates last two bus cycles of four bus cycle sequence.

6. These waveforms are for the word mode.

Package Drawings

★ **44 PIN PLASTIC SOP (600 mil)**



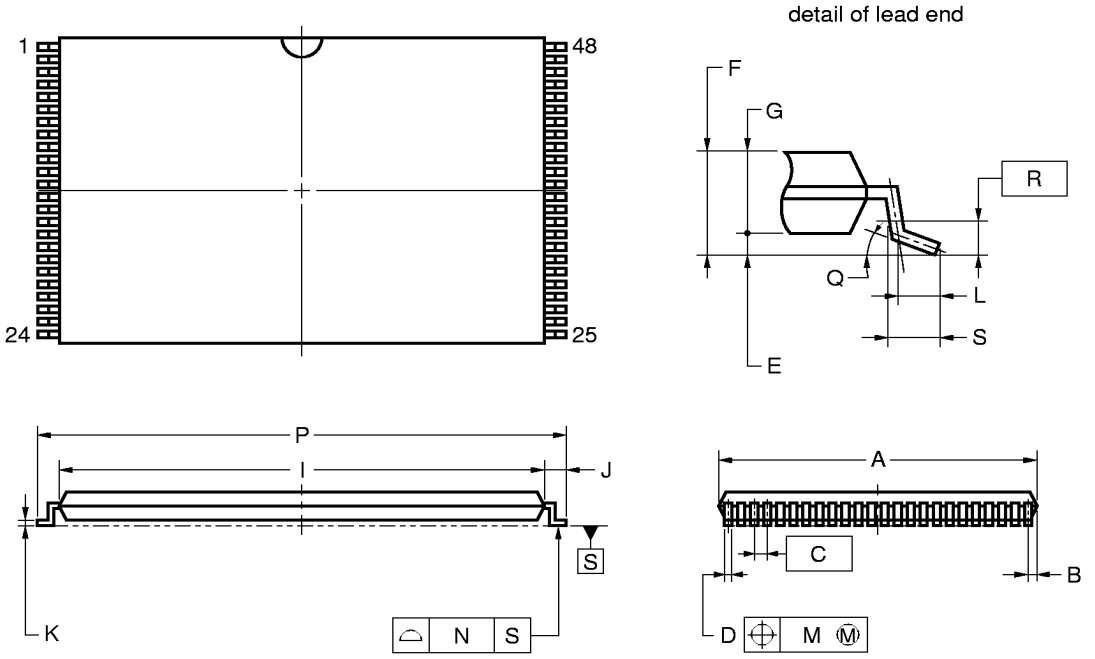
NOTE

1. Controlling dimension — millimeter.
2. Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$27.83^{+0.4}_{-0.05}$	$1.096^{+0.016}_{-0.003}$
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	$0.017^{+0.003}_{-0.004}$
E	0.15±0.1	0.006±0.004
F	3.0 MAX.	0.119 MAX.
G	2.7±0.05	$0.106^{+0.003}_{-0.002}$
H	16.04±0.3	$0.631^{+0.013}_{-0.012}$
I	13.24±0.1	$0.521^{+0.005}_{-0.004}$
J	1.4±0.2	0.055±0.008
K	$0.22^{+0.08}_{-0.07}$	$0.009^{+0.003}_{-0.004}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005
N	0.10	0.004
P	$3^{\circ+7^{\circ}}_{-3^{\circ}}$	$3^{\circ+7^{\circ}}_{-3^{\circ}}$

P44GX-50-600A-3

★ 48 PIN PLASTIC TSOP (I) (12×20)



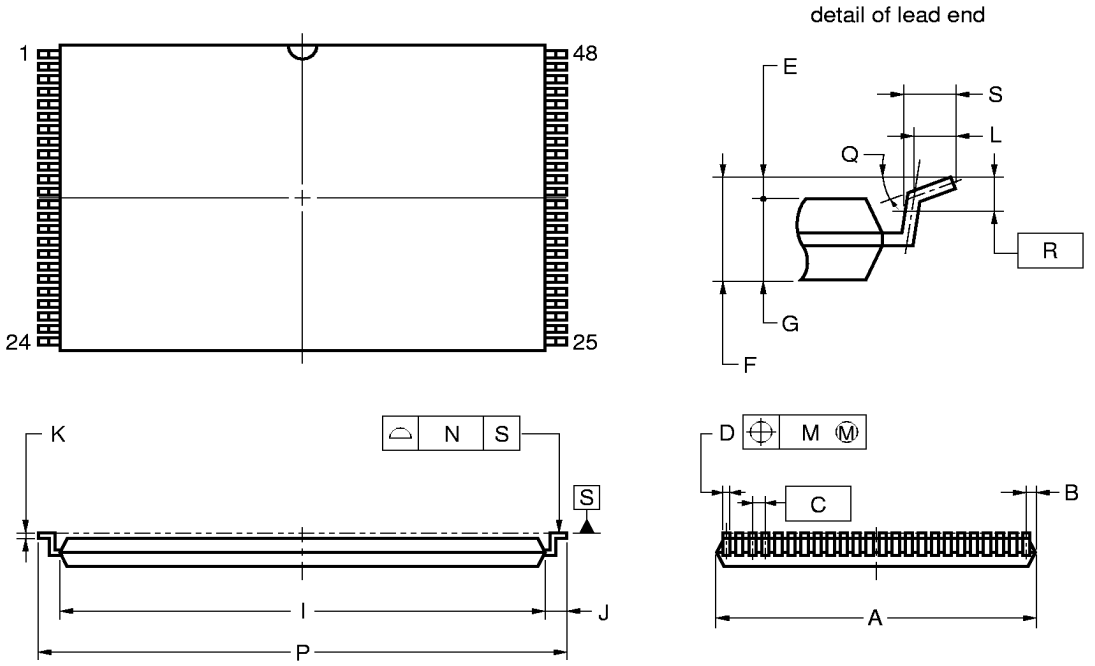
NOTES

1) Controlling dimension —— Millimeter.
2) Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.
3) "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX. <0.489 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	12.0±0.1	$0.472^{+0.005}_{-0.004}$
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.22±0.05	$0.009^{+0.002}_{-0.003}$
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	1.0±0.05	$0.039^{+0.003}_{-0.002}$
I	18.4±0.1	$0.724^{+0.005}_{-0.004}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	0.145±0.05	$0.006^{+0.002}_{-0.003}$
L	0.5	0.020
M	0.10	0.004
N	0.10	0.004
P	20.0±0.2	$0.787^{+0.009}_{-0.008}$
Q	$3°^{+5°}_{-3°}$	$3^{+5°}_{-3°}$
R	0.25	0.010
S	0.60±0.15	$0.024^{+0.006}_{-0.007}$

S48GZ-50-MJH

★ 48 PIN PLASTIC TSOP (I) (12×20)



NOTES

1) Controlling dimension —— Millimeter.

2) Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

3) "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX. <0.489 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	12.0±0.1	$0.472^{+0.005}_{-0.004}$
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.22±0.05	$0.009^{+0.002}_{-0.003}$
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	1.0±0.05	$0.039^{+0.003}_{-0.002}$
I	18.4±0.1	$0.724^{+0.005}_{-0.004}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	0.145±0.05	$0.006^{+0.002}_{-0.003}$
L	0.5	0.020
M	0.10	0.004
N	0.10	0.004
P	20.0±0.2	$0.787^{+0.009}_{-0.008}$
Q	$3°^{+5°}_{-3°}$	$3°^{+5°}_{-3°}$
R	0.25	0.010
S	0.60±0.15	$0.024^{+0.006}_{-0.007}$

S48GZ-50-MKH