


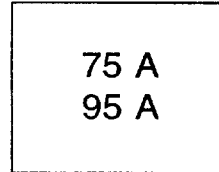
IRK.71, .91 SERIES

THYRISTOR/ DIODE and THYRISTOR/ THYRISTOR

NEWADD-A-pak™ Power Modules

Features

- Electrically isolated: DBC base plate
- 3500 V_{RMS} Isolating voltage
- Standard JEDEC package
- Simplified mechanical designs, rapid assembly
- Auxiliary cathode terminals for wiring convenience
- High surge capability
- Wide choice of circuit configurations
- Large creepage distances
- ULE78996 approved 



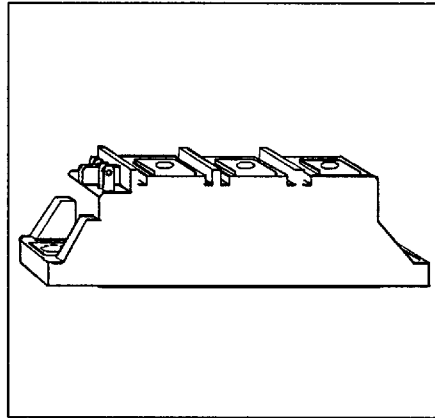
Description

These IRK series of NEW ADD-A-paks use power diodes and thyristors in a variety of circuit configurations. The semiconductor chips are electrically isolated from the base plate, allowing common heatsinks and compact assemblies to be built. They can be interconnected to form single phase or three phase bridges or AC controllers. These modules are intended for general purpose high voltage applications such as high voltage regulated power supplies, lighting circuits, and temperature and motor speed control circuits.

Major Ratings and Characteristics

Parameters	IRK.71	IRK.91	Units
$I_{T(AV)}$ OR $I_{F(AV)}$ @ 85°C	75	95	A
$I_{O(RMS)}$ (*)	165	210	A
I_{TSM} @ 50Hz	1665	1785	A
I_{FSM} @ 60Hz	1740	1870	A
I^2t @ 50Hz	13.86	15.91	KA ² s
@ 60Hz	12.56	14.52	KA ² s
$I^2\sqrt{t}$	138.6	159.1	KA ² /s
V _{RRM} range	400 to 1600		V
T _{STG}	-40 to 125		°C
T _J	-40 to 125		°C

(*) As AC switch.



IRK.71, .91 Series

Bulletin I27132 rev. D 09/97

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ELECTRICAL SPECIFICATIONS

Voltage Ratings

Type number	Voltage Code	V _{RRM} , maximum repetitive peak reverse voltage V	V _{FSM} , maximum non-repetitive peak reverse voltage V	V _{ORM} , max. repetitive peak off-state voltage, gate open circuit V	I _{DRM} 125°C mA
IRK.71/.91	04	400	500	400	15
	06	600	700	600	
	08	800	900	800	
	10	1000	1100	1000	
	12	1200	1300	1200	
	16	1600	1700	1600	

On-state Conduction

Parameters	IRK.71	IRK.91	Units	Conditions	
I _{T(AV)} Max. average on-state current (Thyristors)	75	95	A	180° conduction, half sine wave, T _c = 85°C	
I _{F(AV)} Max. average forward current (Diodes)					
I _{O(RMS)} Max. continuous RMS on-state current. As AC switch	165	210			
I _{TSM} Max. peak, one cycle non-repetitive on-state or forward current	1665	1785			Sinusoidal half wave, Initial T _J = T _J max. T _J = 25°C, no voltage reapplied
I _{FSM}	1740	1870		t=10ms No voltage reapplied	
	1400	1500		t=8.3ms 100% V _{RRM} reapplied	
	1470	1570	t=10ms 100% V _{RRM} reapplied		
	1850	2000	t=8.3ms 100% V _{RRM} reapplied		
I ² t Max. I ² t for fusing	13.86	15.91	KA ² s	t=10ms No voltage reapplied	
	12.56	14.52		t=8.3ms 100% V _{RRM} reapplied	
	9.80	11.25		t=10ms 100% V _{RRM} reapplied	
	8.96	10.27		t=8.3ms 100% V _{RRM} reapplied	
	17.11	20.00		t=10ms T _J = 25°C, no voltage reapplied	
15.60	18.30	t=8.3ms T _J = 25°C, no voltage reapplied			
I ² √t Max. I ² √t for fusing (1)	138.6	159.1	KA ² √s	t=0.1 to 10ms, no voltage reapplied	
V _{T(TO)} Max. value of threshold voltage (2)	0.82	0.80	V	Low level (3)	
	0.85	0.85		High level (4)	
r _t Max. value of on-state slope resistance (2)	3.00	2.40	mΩ	Low level (3)	
	2.90	2.25		High level (4)	
V _{TM} Max. peak on-state or forward voltage	1.59	1.58	V	I _{TM} = π × I _{T(AV)}	
V _{FM}				I _{FM} = π × I _{F(AV)}	
dI/dt Max. non-repetitive rate of rise of turned on current	150		A/μs	T _J = 25°C, from 0.67 V _{DRM} I _{TM} = π × I _{T(AV)} , I _g = 500mA, t _r < 0.5 μs, t _p > 6 μs	
I _H Max. holding current	200		mA	T _J = 25°C, anode supply = 6V, resistive load, gate open circuit	
I _L Max. latching current	400			T _J = 25°C, anode supply = 6V, resistive load	

(1) I²t for time t_x = I²t_x × √t_x (2) Average power = V_{T(TO)} × I_{T(AV)} + r_t × (I_{T(RMS)})² (3) 16.7% × π × I_{AV} < I < π × I_{AV}
 (4) I > π × I_{AV}

Triggering

Parameters	IRK.71	IRK.91	Units	Conditions	
P_{GM} Max. peak gate power	12	12	W		
$P_{G(AV)}$ Max. average gate power	3.0	3.0			
I_{GM} Max. peak gate current	3.0	3.0	A		
$-V_{GM}$ Max. peak negative gate voltage	10		V	Anode supply = 6V resistive load	
V_{GT} Max. gate voltage required to trigger	4.0				$T_J = -40^\circ\text{C}$
	2.5				$T_J = 25^\circ\text{C}$
	1.7		$T_J = 125^\circ\text{C}$		
I_{GT} Max. gate current required to trigger	270		mA	Anode supply = 6V resistive load	
	150				$T_J = 25^\circ\text{C}$
	80				$T_J = 125^\circ\text{C}$
V_{GD} Max. gate voltage that will not trigger	0.25		V	$T_J = 125^\circ\text{C}$, rated V_{DRM} applied	
I_{GD} Max. gate current that will not trigger	6		mA	$T_J = 125^\circ\text{C}$, rated V_{DRM} applied	

Blocking

Parameters	IRK.71	IRK.91	Units	Conditions
I_{RRM} Max. peak reverse and off-state leakage current at V_{RRM} , V_{DRM}	15		mA	$T_J = 125^\circ\text{C}$, gate open circuit
V_{INS} RMS isolation voltage	2500 (1 min) 3500 (1 sec)		V	50 Hz, circuit to base, all terminals shorted
dv/dt Max. critical rate of rise of off-state voltage (5)	500		V/ μs	$T_J = 125^\circ\text{C}$, linear to $0.67 V_{DRM}$, gate open circuit

(5) Available with dv/dt = 1000V/ μs , to complete code add S90 i.e. IRKT91/16 S90.

Thermal and Mechanical Specifications

Parameters	IRK.71	IRK.91	Units	Conditions
T_J Junction operating temperature range	- 40 to 125		°C	
T_{stg} Storage temp. range	- 40 to 125			
R_{thJC} Max. internal thermal resistance, junction to case	0.165	0.135	K/W	Per module, DC operation
R_{thCS} Typical thermal resistance case to heatsink	0.1			Mounting surface flat, smooth and greased. Flatness <0.03mm; roughness <0.02mm
T Mounting torque $\pm 10\%$ to heatsink busbar	5		Nm	A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound
	3			
wt Approximate weight	83 (3)		g (oz)	
Case style	TO-240AA		JEDEC	

IRK.71, .91 Series

Bulletin I27132 rev. D 09/97

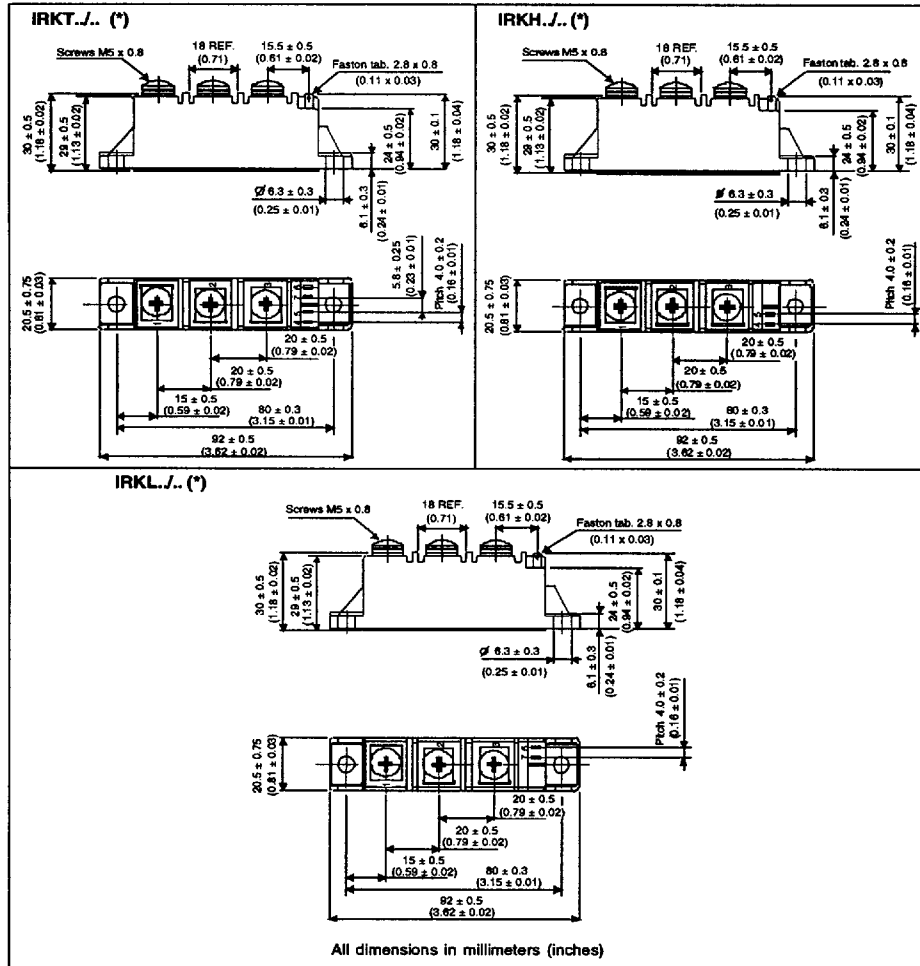
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ΔR Conduction (per Junction)

(The following table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC)

Devices	Sine half wave conduction					Rect. wave conduction					Units
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
IRK.71	0.06	0.07	0.09	0.12	0.18	0.04	0.08	0.10	0.13	0.18	°C/W
IRK.91	0.04	0.05	0.06	0.08	0.12	0.03	0.05	0.06	0.08	0.12	

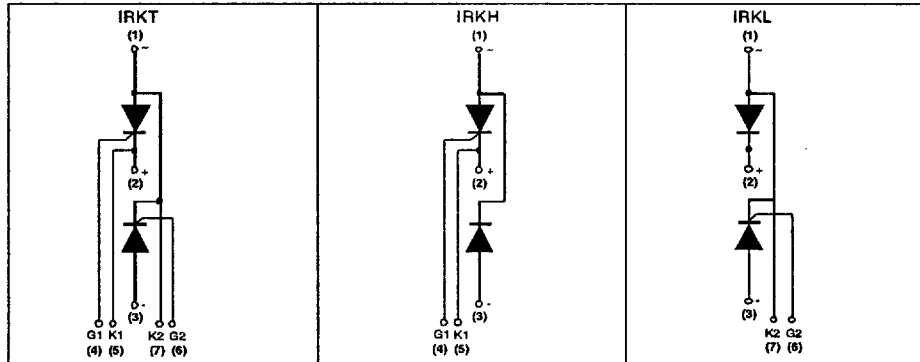
Outlines Table



(*) For terminals connections, see Circuit configurations Table

NOTE: To order the Optional Hardware see Bulletin I27900

Circuit Configurations Table



Ordering Information Table

Device Code

IRK	T	91	/	16	S90
①	②	③		④	⑤

- 1 - Module type
- 2 - Circuit configuration (See Circuit Configuration table)
- 3 - Current code **
- 4 - Voltage code (See Voltage Ratings table)
- 5 - dv/dt code: S90 = dv/dt 1000 V/μs
No letter = dv/dt 500 V/μs

IRK.92 types
With no auxiliary cathode

** Available with no auxiliary cathode.
To specify change: 71 to 72
91 to 92
e.g. : IRKT92/16 etc.

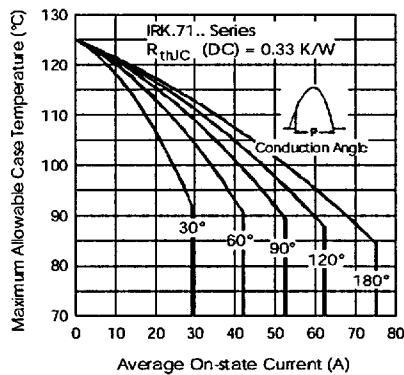


Fig. 1 - Current Ratings Characteristics

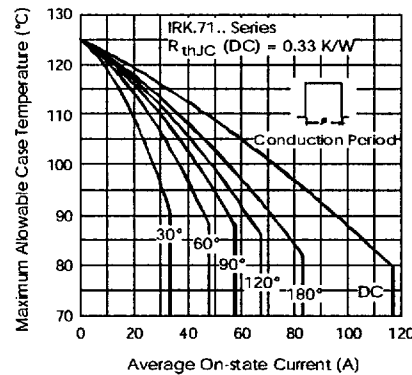


Fig. 2 - Current Ratings Characteristics

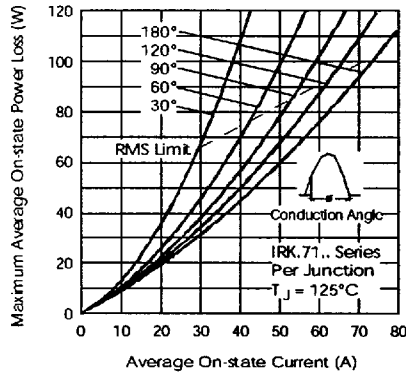


Fig. 3 - On-state Power Loss Characteristics

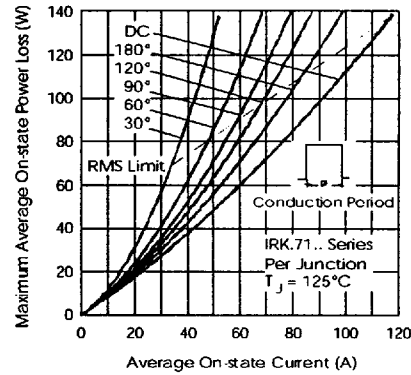


Fig. 4 - On-state Power Loss Characteristics

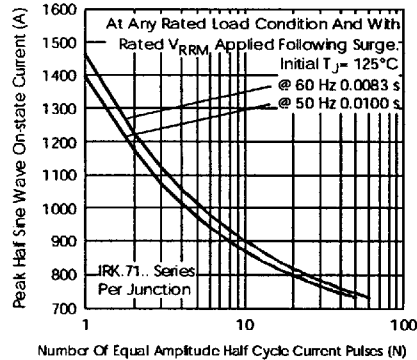


Fig. 5 - Maximum Non-Repetitive Surge Current

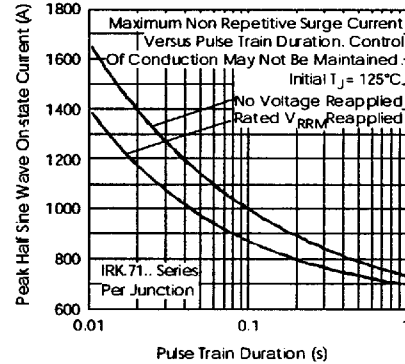


Fig. 6 - Maximum Non-Repetitive Surge Current

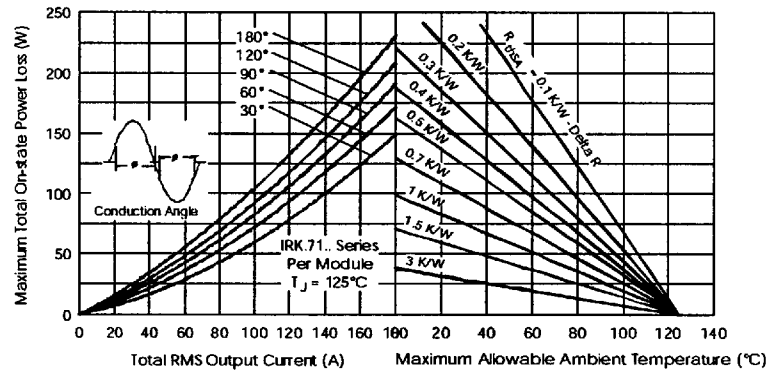


Fig. 7 - On-state Power Loss Characteristics

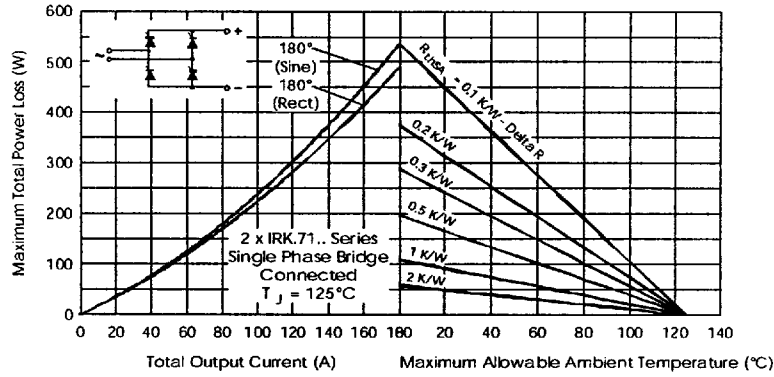


Fig. 8 - On-state Power Loss Characteristics

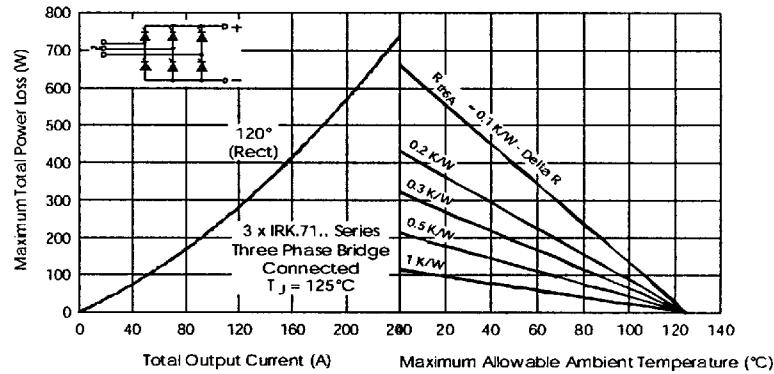


Fig. 9 - On-state Power Loss Characteristics

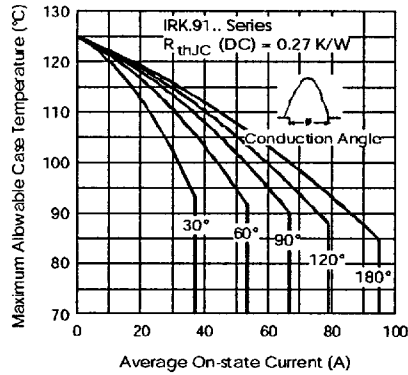


Fig. 10 - Current Ratings Characteristics

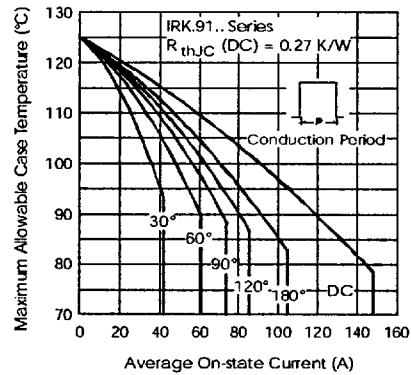


Fig. 11 - Current Ratings Characteristics

IRK.71, .91 Series

Bulletin I27132 rev. D 09/97

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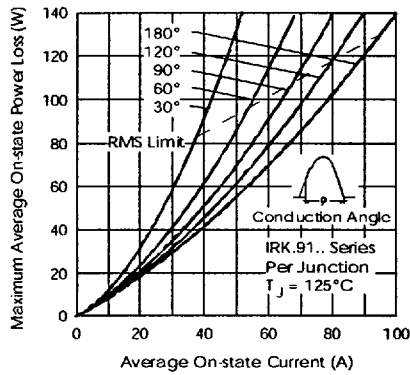


Fig. 12 - On-state Power Loss Characteristics

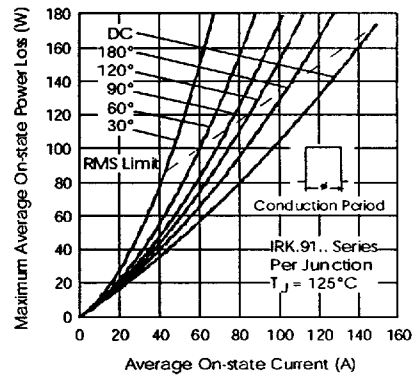


Fig. 13 - On-state Power Loss Characteristics

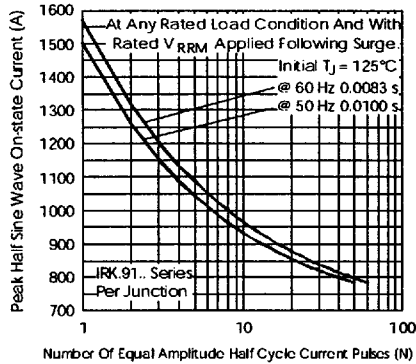


Fig. 14 - Maximum Non-Repetitive Surge Current

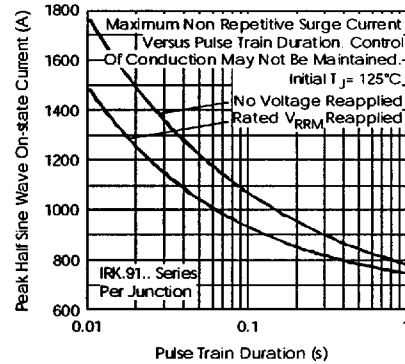


Fig. 15 - Maximum Non-Repetitive Surge Current

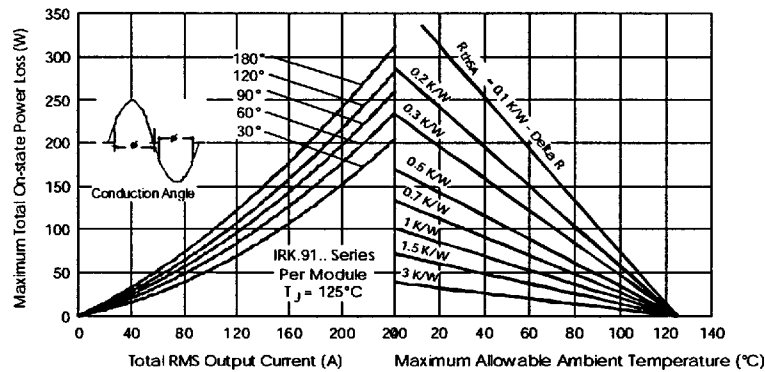


Fig. 16 - On-state Power Loss Characteristics

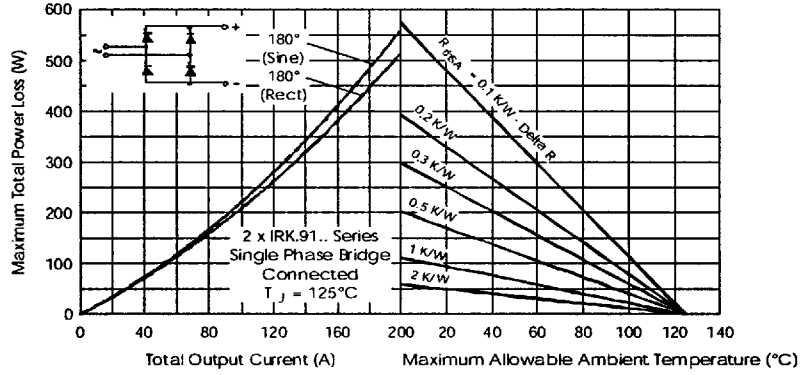


Fig. 17 - On-state Power Loss Characteristics

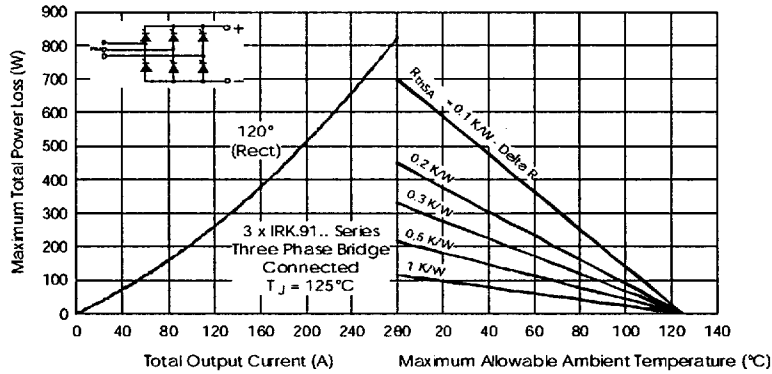


Fig. 18 - On-state Power Loss Characteristics

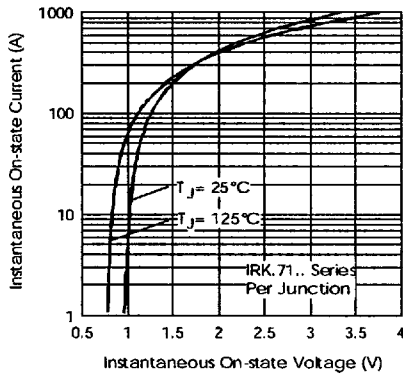


Fig. 19 - On-state Voltage Drop Characteristics

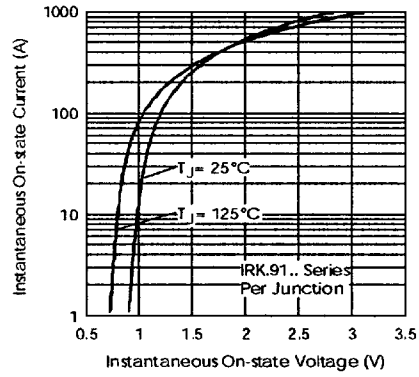


Fig. 20 - On-state Voltage Drop Characteristics

IRK.71, .91 Series

Bulletin I27132 rev. D 09/97

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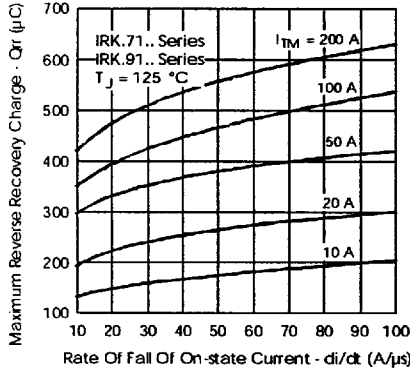


Fig. 21 - Recovery Charge Characteristics

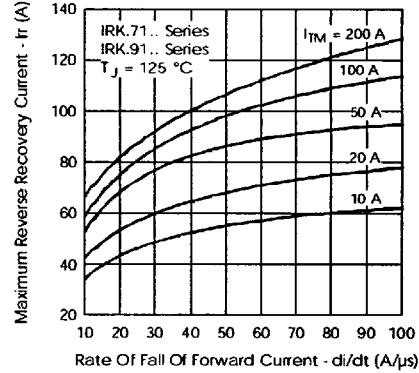


Fig. 22 - Recovery Current Characteristics

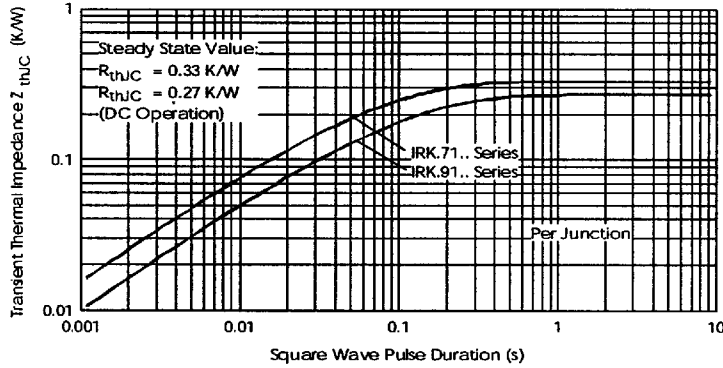


Fig. 23 - Thermal Impedance Z_{thJC} Characteristics

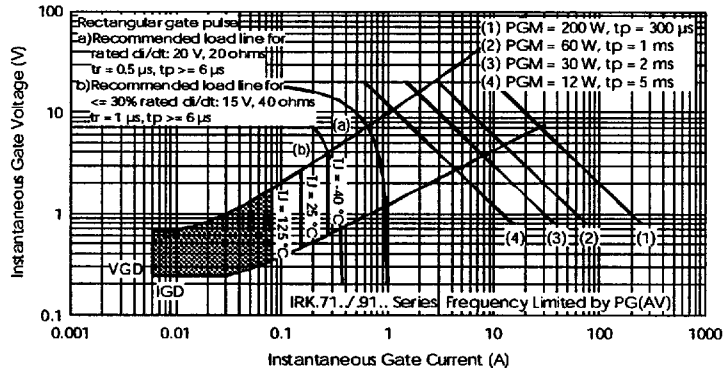


Fig. 24 - Gate Characteristics