CY2081A

Three-PLL Clock Generator

Features

- **Factory-EPROM configurable for quick availability and prototyping.**
- **General purpose clock synthesizer for all applications such as: modems, disk drives, CD-ROM drives, Video CD players, games, set-top boxes, data/telecommunications, etc.**
- **Three independent configurable clock outputs**
- **Outputs ranging from 500 kHz to 100 MHz (5V) and up to 80 MHz for 3.3V operation**
- **Configurable output control pin (pin 8) can be used as an output enable, power-down, suspend or select line.**
- **Phase-locked loop oscillator input derived from external crystal (10 MHz to 25 MHz) or external reference clock (1 MHz to 30 MHz)**
- **3.3V or 5V operation (factory configured)**
- **8-pin 150-mil packaging achieves minimum footprint for space-critical applications**
- **Sophisticated internal loop filter requires no external components or manufacturing tweaks as commonly required with external filters**

Functional Description

The CY2081A is a general-purpose clock synthesizer designed for use in applications such as modems, disk drives, CD-ROM drives, Video CD players, games, set-top boxes and data/telecommunications. This devices offers three configurable clock outputs in an 8-pin 150-mil SOIC package and can be configured to operate off either a 3.3V or 5V power supply. The on-chip reference oscillator is designed for 10 MHz to 25 MHz crystals. Alternatively, a reference clock between 1 MHz and 30 MHz can be used.

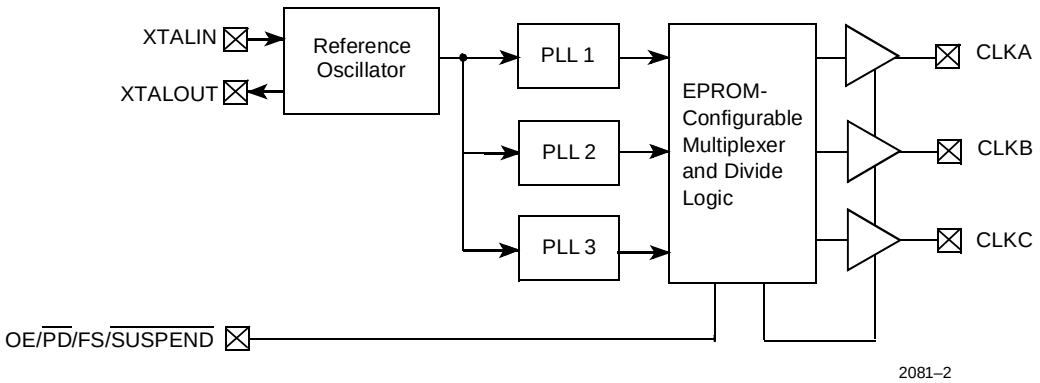
The CY2081A also features an output control pin (pin 8) which can be configured as an output enable, power down, frequency select, or suspend input. This gives the user the ability to three-state the output, power down the device, change the CLKA output frequency during operation, or suspend any of the outputs. Asserting the $\overline{PD}$ input will result in all the PLLs and the outputs being shut down. The PLLs will have to re-lock when the $\overline{PD}$ input is deasserted.

The CY2081A outputs three clocks: CLKA, CLKB, and CLKC, whose frequencies can possess any value within the specified range. Additionally, the reference frequency can be obtained on any output. Custom configurations with user-defined features and frequencies can be obtained by filling out the custom configuration form located at the back of this data sheet and contacting your local Cypress representative.

The CY2081A can replace multiple Metal Can Oscillators (MCO) in a synchronous system, providing cost and board space savings to manufacturers. Hence, this device is ideally suited for applications that require multiple, accurate, and stable clocks synthesized from low-cost generators in small packages. A hard disk drive is an example of such an application. In this case, CLKA drives the PLL in the Read Controller, while CLKB and CLKC drive the MCU and associated sequencers.

Consider using the CY2291, CY2292, or CY2907 for applications that require more than three output clocks.

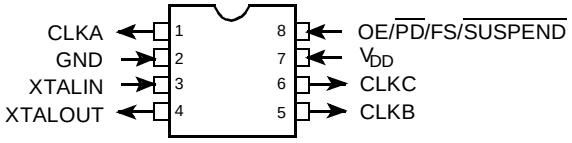
Logic Block Diagram



2081–2

Pin Configuration

SOIC
Top View



2081–1

Pin Summary

Name	Number	Description
CLKA	1	Configurable clock output
GND	2	Ground
XTALIN[1]	3	Reference Crystal Input or External Reference Clock Input
XTALOUT[1, 2]	4	Reference Crystal Feedback
CLKB	5	Configurable clock output
CLKC	6	Configurable clock output
V_{DD}	7	Voltage Supply
OE / $\overline{PD}$ / FS / $\overline{SUSPEND}$	8	Output control pin; either active-HIGH Output Enable, active-LOW power down, CLKA Frequency Select, or active-LOW Suspend input

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to V_{DD}+0.5V

Storage Temperature ..... –65°C to +150°C

Max. Soldering Temperature (10 sec.) .....260°C

Junction Temperature .....150°C

Static Discharge Voltage ..... >2000V (per MIL-STD-883, Method 3015)

Operating Conditions[3]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	4.5 (3.0)	5.5 (3.6)	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Max. Load Capacitance per output		25 (15)	pF
f_{REF}	External Reference Crystal	10.0	25.0	MHz
f_{REF}	External Reference Clock[4, 5]	1.0	30.0	MHz

Electrical Characteristics V_{DD} = 5V (3.3V) ±10%, T_A = 0°C to +70°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{OH}	HIGH-Level Output Voltage	I_{OH} = –4.0 mA	2.4			V
V_{OL}	LOW-Level Output Voltage	I_{OL} = 4.0 mA			0.4	V
V_{IH}	HIGH-Level Input Voltage[6]	Except Crystal Pins	2.0			V
V_{IL}	LOW-Level Output Voltage[6]	Except Crystal Pins			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD} – 0.5V		<100	150	µA
I_{IL}	Input LOW Current	V_{IN} = 0.5V		<100	150	µA
I_{OZ}	Output Leakage Current	Three State Outputs			250	µA
I_{DD}	V_{DD} Supply Current[7]	V_{DD} = V_{DD} max. 5V (3.3V) operation, C_L = 25 pF (15 pF)		40 (24)	60 (40)	mA
I_{DDS}	V_{DD} Power Supply Current in Powerdown Mode	Powerdown Active, 5V Operation		100	200	µA

Notes:

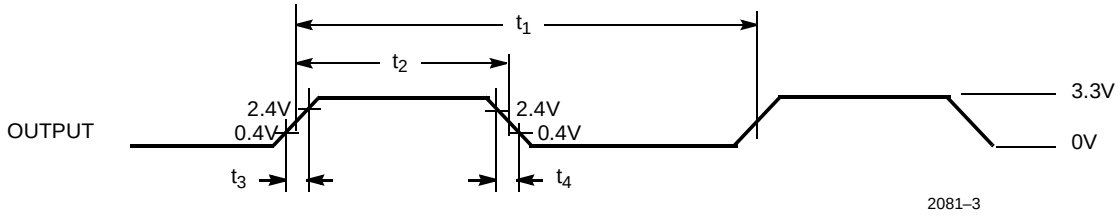
1. For best accuracy, use a parallel-resonant crystal, C_L=17 pF.
2. Float XTALOUT pin if XTALIN is driven by reference clock (as opposed to an external crystal).
3. Electrical parameters are guaranteed with these operating conditions. Values for 3.3V operation are shown in parentheses.
4. External input reference clock must have a duty cycle between 40% and 60%, measured at V_{DD}/2.
5. Please refer to application note “Crystal Oscillator Topics” for information on AC-coupling the external input reference clock.
6. Xtal inputs have CMOS thresholds.
7. Load = max, typical configuration, f_{REF} = 14.318 MHz. Specific configurations may vary.

Switching Characteristics[8]

Parameter	Name	Description	Min.	Typ.	Max.	Unit
t_1	Output Period	Clock output range, 5V operation	10 [100 MHz]		2000 [500 KHz]	ns
t_1	Output Period	Clock output range, 3.3V operation	12.5 [80 MHz]		2000 [500 KHz]	ns
t_{1A}	Clock Jitter[9]	Peak-to-peak period jitter, % of clock period ($f_{OUT} \le 4$ MHz)		<0.5	1	%
t_{1B}	Clock Jitter[9]	Peak-to-peak period jitter (4 MHz $\le f_{OUT} \le$ 16 MHz)		<0.7	1	ns
t_{1C}	Clock Jitter[9]	Peak-to-peak period jitter (16 MHz $< f_{OUT} \le$ 50 MHz)		<400	500	ps
t_{1D}	Clock Jitter[9]	Peak-to-peak period jitter ($f_{OUT} >$ 50 MHz)		<250	350	ps
	Output Duty Cycle[10]	Duty cycle for outputs, defined as $t_2 \div t_1$[11] $f_{OUT} >$ 66.67 MHz	40%	50%	60%	
		Duty cycle for outputs, defined as $t_2 \div t_1$[11] $f_{OUT} \le$ 66.67 MHz	45%	50%	55%	
t_3	Rise time	Output clock rise time[12] at C_L=25 pF (15 pF at 3.3V operation)		3	5	ns
t_4	Fall time	Output clock fall time[12] at C_L=25 pF (15 pF at 3.3V operation)		2.5	4	ns
t_5	Frequency Slew Rate	Rate of change of frequency of CLKA	1	5	40	MHz/ ms
t_6	Power Up Stabilization Time	Output clock stable time after power up		< 25	50	ms

Switching Waveforms

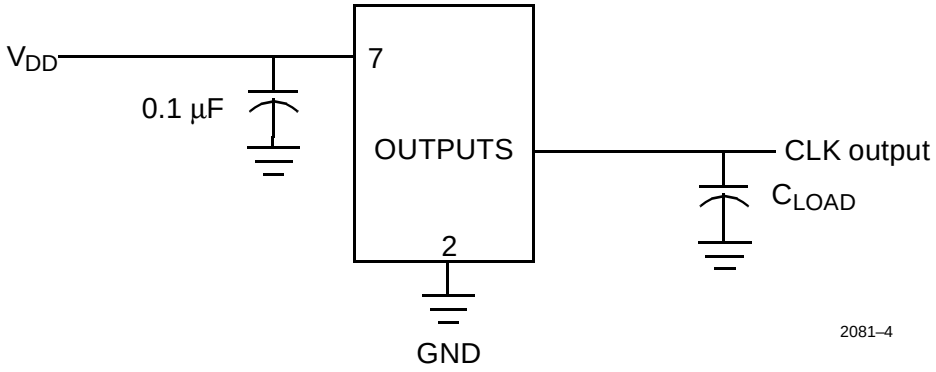
All Outputs Duty Cycle and Rise/Fall Time



Notes:

8. Guaranteed by design, not 100% tested.
9. Jitter varies with configuration. All standard configurations sample tested at the factory conform to this limit. For more information on jitter, please refer to the application note: “Jitter in PLL-Based Systems.”
10. Reference Output duty cycle depends on XTALIN duty cycle.
11. Measured at 1.4V.
12. Measured between 0.4V and 2.4V.

Test Circuit



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2081ASC–XXX	S8	8-Pin (150-Mil) SOIC	5.0V, Commercial[13]
CY2081ASL–XXX	S8	8-Pin (150-Mil) SOIC	3.3V, Commercial[13]

Note:
13. 0°C to +70°C

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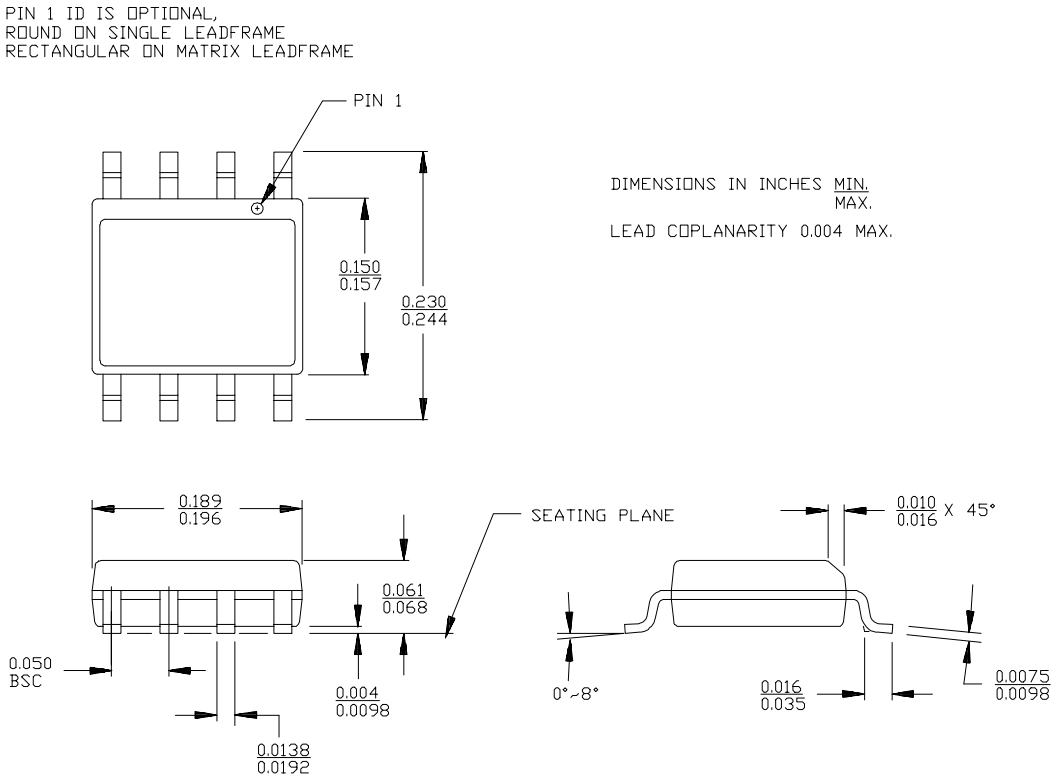
Package Diagrams

8-Lead (150-Mil) SOIC S8



CY2081A CONFIGURATION REQUEST FORM

Customer _____ Engineer _____ FAE/Sales _____
Phone # _____ Fax # _____ Date _____

1. OPERATING VOLTAGE (circle one) **3.3V** **5.0V**

2. INPUT REFERENCE FREQUENCY (Circle one) **Crystal** **External Clock**

Default reference = 14.318 MHz. If a different reference is desired, specify the frequency in the box to the right (must be between 10 MHz and 25 MHz for crystal, 1 MHz and 30 MHz for external clock):

3. OUTPUT CONTROL PIN (PIN 8) CONFIGURATION (Circle one)

OE (Default) **$\overline{PD}$** **FS** **$\overline{SUSPEND}$**

If the Suspend option is desired, please circle what outputs must be suspended

CLKA **CLKB** **CLKC**

4. OUTPUT CONFIGURATION

Fill in the desired frequencies, specifying kHz or MHz, for each output. Please adhere to the notes at the right. Contact your local Cypress representative for assistance. After configuration, please fax the form to your local Cypress representative.

CLKA (FS=0) _____
CLKA (FS=1) _____
CLKB _____
CLKC _____

Notes:

- If pin 8 is OE, $\overline{PD}$ or $\overline{SUSPEND}$, fill in only one value for **CLKA**
- Buffered reference clock is available on all outputs.
- **CLKA, CLKB and CLKC**, outputs can range from 500 kHz to 100 MHz (80 MHz at 3.3V)

5. FOR CYPRESS USE ONLY

Customer Configuration	Marking
Date	Quantity