Data Sheet
May 1995

AT&T Microelectronics

ATT21C505/504: 32-Bit Interface RAMDACs *PrecisionDAC*™ Technology

Features

- Speed grades:
  — ATT21C505: 200/170/150/135/110 MHz
  — ATT21C504: 110/85 MHz
- 16M, 256K, 64K, 32K, 256 on-screen colors
- Ten software selectable color modes:
  — 24-, 16-, 15-bit true-color bypass
  — 24, 16, 15, 8, 4, 1 bit(s) through CLUT
  — 8-bit pseudocolor
- Output current accuracy better than ±3% typical
- 1:1, 2:1, 4:1, 8:1, and 32:1 pixel multiplexing
- Hardware cursor: 32 x 32 x 2 (504), 64 x 64 x 2 (505)
- 2x clock multiplier (analog PLL)
- Separate SVGA port
- Nibble swap for 4 bits per pixel
- SCLK inversion with control register bit
- Programmable sync on green (red and blue DACs have no sync current option)
- Software identification
- Shift clock for VRAM support
- Powers down to 3 mA typ while updating MPU port
  — Update to control register in P. D.
- Power dissipation: 1.0 W typ at 135 MHz
- Three 256 x 8 color RAMs, 3 x 24 cursor color RAM, and 1 x 24 overscan RAM
- In-circuit test signature analysis registers
- 84-pin PLCC package
- ISO 9000 certified

Applications

- Screen resolutions (noninterlaced)
  — ATT21C505: 1600 x 1280, 60 Hz, 64K colors
  — ATT21C505/504: 1280 x 1024, 60 Hz,1 6M colors
- True-color desktop, PC add-in card
- *X-Windows** terminals

Description

The ATT21C505/504 32-Bit Interface supports true-color and SVGA graphics in a *Windows*† environment. On the 505, an internal analog PLL 2x clock multiplier doubles the pixel output rate for a high-resolution, color display. Both devices support 24-bit non-multiplexed and 16-, 15-, 8-, 4-, and 1-bit multiplexed operation. SVGA graphics can be input through an 8-bit port.

The ATT21C505 adds functionality to the ATT20C505. The ATT21C505 includes a bit to invert the SCLK signal before driving the SCLK pin.

The ATT21C505 has a 32-bit wide port and can be programmed to support 1, 4, 8, 15, 16, or 24 bits per pixel. The ATT21C505 port supports a 64 x 64 x 2 or a 32 x 32 x 2 cursor. The ATT21C504 supports a 32 x 32 x 2 cursor.

Table 1. Comparison of ATT21C505/504 vs. ATT20C505/504

Feature	ATT21C505/504	ATT20C505/504
SLCK invert CR3[5]	Yes	No
Sync current on red and blue DACs	No	Yes
V_{REF} link-trimmed for ±3% current accuracy	Yes	No

Both devices feature three 8-bit DACs with antisparkle circuitry. On-chip comparators detect connection to a monitor. Each device is link-trimmed to ensure an on-chip voltage reference is accurate to ±3% typical. The device is offered in an 84-pin PLCC package.

* *X-Windows* is a registered trademark of Massachusetts Institute of Technology.
† *Windows* is a registered trademark of Microsoft Corporation.

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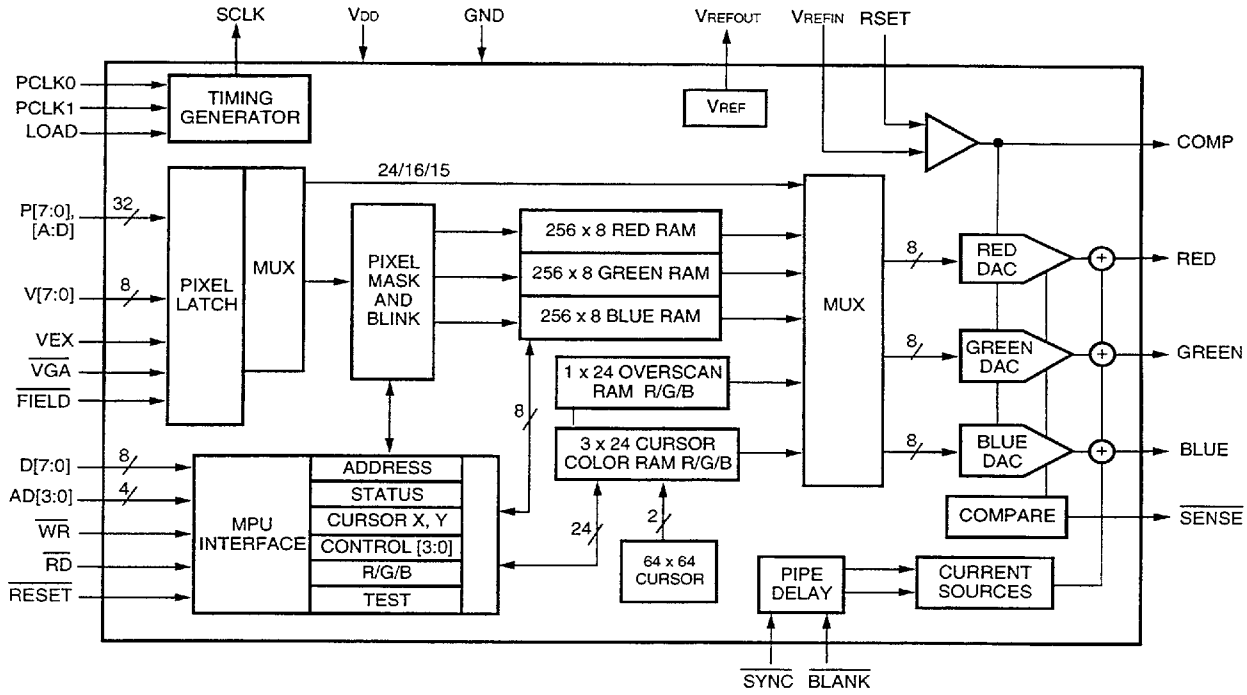


Figure 1. Block Diagram

Pin Information

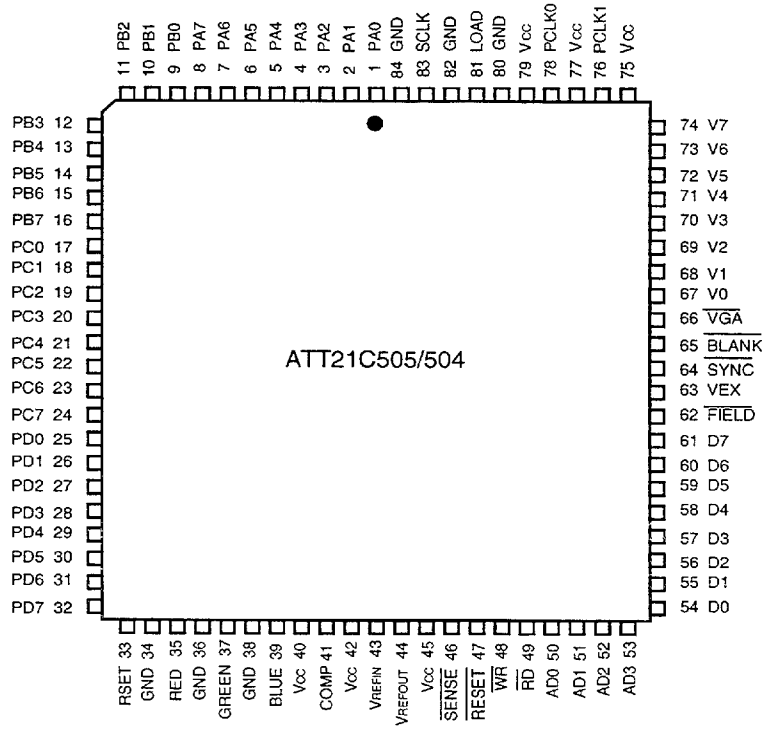


Figure 2. 84-Pin PLCC Pin Diagram

Pin Information (continued)

Table 2. Pin Descriptions

ATT21C505/504 Pin #	Symbol	Type	Name/Function
1—32	P[A:D] [7:0]	I	**Pixels.** TTL compatible. These pins are latched on the rising edge of LOAD. Pixels can be presented to the DACs as color data (bypass modes), or used as addresses to look up color data in the color RAM. These pixel inputs are selected if VGA is a logic 1, and CR2[5] does not mask out the pixel inputs. Pixels can be multiplexed at 1:1, 2:1, 4:1, 8:1, or 32:1. Unused inputs should be connected to GND.
33	RSET	I	**Reference Resistor.** An external resistor (RSET) is connected between the RSET pin and GND to control the magnitude of the full-scale current. Refer to DAC Gain section under Functional Description.
34, 36, 38, 80, 82, 84	GND	—	**Ground.**
35, 37, 39	RED GREEN BLUE	O	**Color Signals.** These pins are analog outputs. High-impedance current sources are capable of driving a double-terminated 75 Ω coaxial cable.
40, 42, 45, 75, 77, 79	V_{CC}	—	**Power.**
41	COMP	—	**Compensation Pin.** Bypass this pin with an external 0.1 µF capacitor to V_{CC}.
43	V_{REFIN}	I	**Voltage Reference In.** If an external voltage is used, it must supply this input with a 1.235 V reference. Connect this pin to V_{REFOUT} to use the internal voltage reference. This pin is disabled during powerdown.
44	V_{REFOUT}	O	**Voltage Reference Out.** Connect this pin to V_{REFIN} if using the on-chip voltage reference. This output can drive up to four V_{REFIN} pins. This pin can be left floating if an external voltage reference is used.
46	$\overline{SENSE}$	O	$\overline{SENSE}$ **(Active-Low).** TTL compatible. Monitor detect signal. $\overline{SENSE}$ is a logic 0 if one or more of the red, green, or blue outputs have exceeded the internal voltage reference level of 340 mV. $\overline{SENSE}$ cannot be stable while SYNC is toggling.
47	$\overline{RESET}$	I	$\overline{RESET}$ **(Active-Low).** TTL compatible. Resets the control register bits to 0 and places the device in VGA mode. The read mask register is not initialized when $\overline{RESET}$ goes low.
48	$\overline{WR}$	I	**Write (Active-Low).** TTL compatible. $\overline{WR}$ controls the data transfer from the data bus to the selected internal register. D[7:0] data is latched at the rising edge of $\overline{WR}$, and AD[3:0] data is latched at the falling edge of $\overline{WR}$.
49	$\overline{RD}$	I	**Read (Active-Low).** TTL compatible. When $\overline{RD}$ is low, data transfers from the selected internal register to the data bus. AD[3:0] is latched on the falling edge of $\overline{RD}$.
50—53	AD[3:0]	I	**Register Address.** TTL compatible. These inputs are sampled on the falling edge of the $\overline{RD}$ or $\overline{WR}$ to determine which one of the internal registers is to be accessed.

Pin Information (continued)

Table 2. Pin Descriptions (continued)

ATT21C505/504 Pin #	Symbol	Type	Name/Function
54—61	D[7:0]	I/O	**Data Bus.** TTL compatible. Data is transferred between the data bus and the internal registers under control of the RD and WR signals. In an MPU write operation, D[7:0] is latched on the rising edge of WR . To read data D[7:0] from the device, RD must be in an active-low state. The rising edge of the RD signal indicates the end of a read cycle. Following the read cycle, the data bus will go into a high-impedance state. **Note**: For 6-bit operation, color data is contained in the lower 6 bits of the data bus. D0 is the least significant bit (LSB), and D5 is the most significant bit (MSB). When the MPU writes color data, D6 and D7 are ignored. During MPU read cycles, D6 and D7 are a logic 0.
62	FIELD	I	**Interlace Field.** TTL compatible. The interlaced field is either odd or even depending on whether the odd or even scan lines are being traced. A logic 1 on this input indicates an odd field scan, and a logic 0 indicates an even field scan. This input is for proper operation of the on-chip cursor. This pin is ignored if noninterlaced operation is selected. This signal should be changed only during vertical blanking periods.
63	VEX	I	**Video Enable Switch.** This signal is latched on the rising edge of LOAD and controls whether pixel, cursor, overscan, or blank data are displayed. If overscanning is not used, tie this pin to BLANK . See Functional Description for further information on this pin.
64	$\overline{\text{SYNC}}$	I	**$\overline{\text{SYNC}}$ (Active-Low).** TTL compatible. This signal is latched on the rising edge of LOAD. Sync removes a 7.62 mA (RS-343A) current source from the RGB outputs programmed to have sync. For SYNC to operate properly, it should be asserted only during blanking. For systems having a sync signal separate from the RAMDAC, CR0[4:2] should be programmed to a logic 000 to turn off the sync current sources. SYNC may be either positive or negative polarity. See Positive or Negative SYNC under Functional Description.
65	$\overline{\text{BLANK}}$	I	**$\overline{\text{BLANK}}$ (Active-Low).** TTL compatible. $\overline{\text{BLANK}}$ is latched on the rising edge of LOAD. When BLANK is low, the 1.44 mA current source on the analog outputs will be turned off. The DACs ignore digital input from memory. The pixel, cursor, and overscan color memories can be updated during blanking. BLANK latches the SYNC polarity. See Positive or Negative SYNC under Functional Description.

Pin Information (continued)

Table 2. Pin Descriptions (continued)

ATT21C505/504 Pin #	Symbol	Type	Name/Function
66	$\overline{\text{VGA}}$	I	**Pixel Input Select.** TTL compatible. A logic low enables the device to accept pixels on the V[7:0] SVGA inputs. When a logic high, pixels will be accepted on the P[A:D], [7:0] inputs if CR2[5] is also a logic high. This pin switches between the pixel and SVGA inputs on a pixel-by-pixel basis when in the 1:1 MUX modes. In 2:1, 4:1, 8:1, and 32:1 modes, this pin can be used to switch pixel inputs frame by frame (see Table 16).
67—74	V[7:0]	I	**VGA Pixels.** TTL compatible. Super VGA pixel inputs. These pins are enabled by $\overline{\text{VGA}}$. These pins are latched on the rising edge of LOAD. Pixels are used as addresses to look up color data in the color RAM. These pixel inputs are selected if $\overline{\text{VGA}}$ is a logic 0. Pixels are 1:1 multiplex mode only, and V0 is the LSB. Unused inputs should be connected to GND.
76	PCLK1	I	**Pixel Clock 1.** TTL compatible. Selected by CR2[4] = 1; PCLK1 or PCLK0, whichever is selected, clocks the video pipeline in 32:1, 8:1, 4:1, and 2:1 MUX modes.
78	PCLK0	I	**Pixel Clock 0.** TTL compatible. Selected by CR2[4] = 0; PCLK0 or PCLK1, whichever is selected, clocks the video pipeline in 32:1, 8:1, 4:1, and 2:1 MUX modes.
81	LOAD	I	**Load Clock.** TTL compatible. The rising edge of LOAD clock latches V[7:0], P[7:0][A:D], $\overline{\text{BLANK}}$, $\overline{\text{SYNC}}$, VEX, and $\overline{\text{VGA}}$. See the ac characteristics tables under Electrical Characteristics. LOAD equals the selected pixel clock divided by the programmed multiplexing rate (1 for 1:1, 2 for 2:1, 4 for 4:1, and 8 for 8:1). In 1:1 MUX mode, LOAD clocks the video pipeline.
83	SCLK	O	**VRAM Shift Clock.** TTL compatible. This clock output is equal to the pixel rate divided by the multiplexing rate. If the clock doubler is selected (CR3[3]), this clock will be double the pixel clock divided by the multiplexing rate (SCLK = pixel clock/MUX rate). SCLK is phase delayed from PCLK0 or PCLK1. In 1:1 MUX mode, PCLK0 or PCLK1 must be clocked for SCLK to provide an output signal. See the ac characteristics tables under Electrical Characteristics.

Internal Registers

The following table shows the internal registers of the ATT21C505/504. Control register 3 and the test registers are accessed indirectly (see Table 6).

Table 3. Register Map

AD[3:0]	Register Name	Addressed by MPU
0000	WR1	Address register; write pixel color or cursor pattern RAM
0001	—	Pixel color RAM
0010	RMR	Pixel read mask register
0011	RD1	Address register; read pixel color or cursor pattern RAM
0100	WR2	Address register; write cursor or overscan color RAM (See Table 4.)
0101	—	Overscan and cursor color RAM
0110	CR0	Control register 0
0111	RD2	Address register; read cursor or overscan color RAM (See Table 4.)
1000	CR1	Control register 1
1001	CR2	Control register 2
1010	ST	Status register* (read only)
1011	—	Cursor pattern RAM (See Table 20.)
1100	X-low	Cursor position X-low
1101	X-high	Cursor position X-high
1110	Y-low	Cursor position Y-low
1111	Y-high	Cursor position Y-high
†	CR3	Control register 3
†	TEST	Red, green, blue test registers

* The status register can be accessed indirectly (see Table 6).
† See extended registers (Table 6) for access to CR3 and RGB test registers.

Table 4. Mapping of Overscan, Cursor, and Pixel Color RAM

WR1[7:0]	AD[3:0]	Addressed by MPU
$FF—$00	0001	Pixel color RAM

WR2[1:0]	AD[3:0]	Addressed by MPU
$0	0101	Overscan color RAM
$1	0101	Cursor color RAM 1
$2	0101	Cursor color RAM 2
$3	0101	Cursor color RAM 3

Internal Registers (continued)

Table 5. ATT21C505 and ATT21C504 Device Differences

The following table shows the difference between the ATT21C505 and the ATT21C504 RAMDACs. Both of the devices have the same pinout and are similar in functionality; however, the ATT21C505 has additional capability.

Difference	ATT21C505	ATT21C504
Cursor	64 x 64 x 2	32 x 32 x 2
Clock Doubler	Yes	No
Identification	ST[7] = 1	ST[7] = 0
Device Type	ST[6:4] = 101	ST[6:4] = 100
Maximum Speed (MHz)	200	110

Table 6. Extended Register Map (Indexed Addressing)

The following table shows the extended internal registers of the ATT21C505/504. Control register 3 and the R, G, and B test registers are accessed indirectly, while the status register may be read directly or indirectly. When indirectly addressing the registers listed in the table below, WR1 does not autoincrement.

AD[3:0]	CR0[7]	WR1	Register Name	Addressed by MPU
1010	1	$00	ST	Status register (read only)
1010	1	$01	CR3	Control register 3
1010	1	$02	—	Reserved
1010	1	$03	TEST	R, G, and B test registers

To access the extended registers, perform the following sequence:

1. Set CR0[7] = 1.
2. Set AD[3:0] to 0000.
3. Write WR1 with the hex value for the desired register. (For CR3, WR1[7:0] = $01.)
4. Set AD[3:0] to 1010.
5. Write (or read) the desired register.

Pixel Read Mask Register

The read mask register operates in all CLUT modes. The register is not initialized and must be set to 1 during initialization for transparent operation. A write to the 8-bit pixel read mask register masks the address for all three (red, green, and blue) RAMs in true-color modes. The read mask register is bit-wise logically ANDed with the pixel addresses. In bypass modes, this register is not active. A logic 1 stored in a data bit of the read mask register leaves the corresponding bit in the pixel unchanged. A logic 0 in the read mask register sets the pixel bit to 0. Bit D0 of the pixel read mask register corresponds to pixel bit P[A:D]0 or V0.

Internal Registers (continued)

Address Register Descriptions

The address registers are operational on powerup. They can be read or written to by the MPU at any time and are not initialized. $\overline{\text{RESET}}$ does not affect these registers.

Table 7. Register WR1 and RD1 Pixel Color or Cursor Pattern RAM

Bit	Name/Description
WR1[7:0]	**Address Register, Write #1.** These bits address locations in the pixel color or cursor pattern RAM during a write operation. WR1[7] is the MSB and corresponds to MPU data bit D7.
RD1[7:0]	**Address Register, Read #1.** These bits address locations in the pixel color or cursor pattern RAM during a read operation. RD1[7] is the MSB and corresponds to MPU data bit D7.

Table 8. Register WR2 and RD2 Cursor or Overscan Color RAM

Bit	Name/Description
WR2[7:0]	**Address Register, Write #2.** These bits address locations in the cursor or overscan color RAMs during a write operation. WR2[7] is the MSB and corresponds to MPU data bit D7.
RD2[7:0]	**Address Register, Read #2.** These bits address locations in the cursor or overscan color RAMs during a read operation. RD2[7] is the MSB and corresponds to MPU data bit D7.

The internal address registers in the ATT21C505/504 are listed in Tables 7 and 8. The address registers consist of a single register decoded four ways. Toggling the address lines AD[3:0] to 0000, 0011, 0100, or 0111 will replace any value in the address register. The device was designed to support enhanced features in an SVGA compatible architecture. In a typical SVGA system, only AD[1:0] register select signals are provided allowing access to just four registers. In order to provide the enhanced features, additional register locations have been added.

Register WR1 holds an 8-bit value used as an address when writing the pixel color or cursor pattern RAMs. This register autoincrements and wraps around from $FF to $00.

Register RD1 holds an 8-bit value used as an address when reading the pixel color or cursor pattern RAMs. This register autoincrements and wraps around from $FF to $00.

Register WR2 holds an 8-bit value used as an address when writing the cursor or overscan color RAMs. This register autoincrements for the cursor color and wraps around from $FF to $00, but only the two LSBs are used for addressing the cursor or overscan color RAMs.

Register RD2 holds an 8-bit value used as an address when reading the cursor or overscan color RAMs. This register autoincrements for the cursor color and wraps around from $FF to $00, but only the two LSBs are used for addressing the cursor or overscan color RAMs. For further information, see the MPU Interface section under Functional Description.

Internal Registers (continued)

Register Descriptions

Table 9. Control Register 0

This register is operational on powerup. It can be read or written to by the MPU at any time and is not initialized. This register may be written by using AD[3:0] = 0110. All bits are set to 0 upon asserting RESET .

Bit	Name/Description
CR0[7]	**Extended Register Access.** Logic 0: Extended register access disable. Logic 1: Extended register access enable. A logic 1 enables the extended registers to be accessed. The extended registers are mapped into the register space at AD[3:0] = 1010 (see Table 6).
CR0[6]	**SCLK Disable During Sleep.** Logic 0: Enable SCLK during sleep, CR0[0] = 0. Logic 1: Disable SCLK during sleep, CR0[0] = 1. A logic 1 written to this bit disables SCLK output while the device is asleep. A logic 0 written to this bit enables SCLK output while the device is asleep. Bit CR2[7] 3-states the SCLK output.
CR0[5]	**Blank Pedestal Enable.** Logic 0: No blank pedestal. Logic 1: Blank pedestal enabled. This pin controls whether the BLANK pin shuts off a 7.5 IRE current source on R, G, and B when blanking is asserted. For VGA compatibility, write a 0 to this bit.
CR0[4]	**Reserved.** This bit may be read and will return the value written, but will not affect the function of the device.
CR0[3]	**Sync Enable on Green DAC.** Logic 0: Sync disabled. Logic 1: Sync enabled. This bit specifies whether the green output will have sync offset current. A logic 1 specifies sync current. The sync currents enabled by CR0[3] are controlled by the SYNC pin. For noncomposite sync, program CR0[3] to a logic 0.
CR0[2]	**Reserved.** This bit may be read and will return the value written, but will not affect the function of the device.
CR0[1]	**8-/6-Bit Select.** Logic 0: 6-bit. Logic 1: 8-bit. A logic 1 specifies 8-bit color operation (16M possible colors). A logic 0 specifies 6-bit color operation (256K possible colors). CR0[1] controls whether 8 or 6 bits of color information are being passed over the D[7:0] port and whether the DACs are 8 or 6 bits.
CR0[0]	**Sleep Enable.** Logic 0: Normal operation. Logic 1: Sleep mode. If this bit is logic 0, the device will be in normal operation. If this bit is logic 1, the DACs are turned off and the pixel, cursor, overscan color RAMs, and cursor pattern RAM are powered down. The RAM retains data for all clock speeds. The RAM will wake up to accept inputs from the MPU port only up to 50 MHz in sleep mode. After accepting MPU data, the RAM returns to the sleep state. During this process, the device tracks color changes to the color look-up table while utilizing minimum power. After programming the device for normal operation, valid data will appear at the DAC outputs in about one second.

Internal Registers (continued)

Register Descriptions (continued)

Table 10. Control Register 1

This register is operational on powerup. It can be read or written to by the MPU at any time and is not initialized. All bits are set to 0 upon asserting RESET .

Bit	Name/Description
CR1[7:5]	**Select Bits per Pixel.** Logic 000: One 24-bit pixel. Logic 001: One or two 16-, 15-bit pixel(s). Logic 010: Four 8-bit pixels. Logic 011: Eight 4-bit pixels. Logic 100: Thirty-two 1-bit pixels. These bits select the number of bits per pixel. The 16, 15 bits per pixel multiplexing rates are set by CR1[2].
CR1[4]	**True-Color Bypass Enable.** Logic 0: Use pixels as addresses for CLUT (gamma correction mode). Logic 1: Bypass CLUT. This bit controls CLUT bypass for 16-, 15-, and 24-bit modes. When a logic 1, the pixel data is input directly to the DACs. When a logic 0, the true-color data is used as an address to the R, G, B color RAMs. In this case, the value in the color RAMs may be the gamma-corrected color.
CR1[3]	**16-, 15-Bit Color Format.** Logic 0: 5-5-5 red, green, blue. Logic 1: 5-6-5 red, green, blue. This sets the color format in 16-bit per pixel modes (see Tables 17 and 18 for a description of each mode).
CR1[2]	**16-, 15-Bit Multiplexing Ratio.** Logic 0: 2:1 Multiplexing. Logic 1: 1:1 Multiplexing. This bit sets the multiplexing rate in the 16-, 15-bit modes.
CR1[1]	**16-Bit Pixel Switch Control.** Logic 0: CR1[0] controls selection (nonreal time). Logic 1: PD7 controls selection (real time). This bit specifies the control for pixel-by-pixel switching between P[7:0][A:B] and P[7:0][C:D]. This bit is active when 1:1 multiplexing is enabled (CR1[2] = 1) and 16-bit 5-5-5 color (CR1[3] = 0) is specified.
CR1[0]	**16-Bit Pixel Multiplex Select.** Logic 0: Multiplex [A:B] port for 16-bit pixel operation. Logic 1: Multiplex [C:D] port for 16-bit pixel operation. This bit specifies which 16-, 15-bit word is selected at the pixel inputs. This control bit is not a real-time switch.

Internal Registers (continued)

Register Descriptions (continued)

Table 11. Control Register 2

This register is operational on powerup. It can be read or written to by the MPU at any time and is not initialized. All bits are set to 0 upon asserting RESET .

Bit	Name/Description
CR2[7]	**SCLK Control.** Logic 0: SCLK enabled. Logic 1: SCLK disabled. A logic 0 enables the SCLK output. A logic 1 3-states the SCLK output. Refer to bit CR0[6] when CR2[7] is enabled.
CR2[6]	**Test Path Select.** Logic 0: Signature analysis registers (R, G, B). Logic 1: DAC inputs (R, G, B). This bit selects which test data will be read over the MPU bus. When this bit is a logic 0, the test registers accumulate red, green, and blue signatures. When this bit is a logic 1, the test registers hold red, green, and blue DAC input data. The MPU test path will not operate at pixel speed when CR2[6] is a logic 1. See Test Registers section.
CR2[5]	**Pixel Input Gate.** Logic 0: V[7:0] inputs enabled, cannot switch to P[7:0] [A:D] pixel inputs. Logic 1: V[7:0] or P[7:0] [A:D] This bit controls whether the pixel inputs P[7:0] [A:D] can be turned on. When a logic 0, the pixel inputs are gated off; when a logic 1, the pixel inputs can be selected depending on the value of the VGA pin.
CR2[4]	**Pixel Clock Select.** Logic 0: PCLK 0. Logic 1: PCLK1. This bit determines whether pixel clock 0 or pixel clock 1 is selected.
CR2[3]	**Interlace Select.** Logic 0: Noninterlaced. Logic 1: Interlaced. This bit controls the operation of the on-chip cursor. Set this bit to logic 1 for interlace operation.
CR2[2]	**16-, 15-Bit per Pixel CLUT Addressing.** Logic 0: Set bits to MSBs for addressing CLUT (spaced). Logic 1: Set bits to LSBs for addressing CLUT (packed). This bit determines whether the 5- or 6-bit address will address the lower portion of color RAM memory (packed), or will index evenly throughout the color RAM (spaced).
CR2[1:0]	**Cursor Type Select.** Logic 00: Disable cursor. Logic 01: Three-color cursor. Logic 10: Two-color cursor with reverse video. Logic 11: Two-color *X-Windows* cursor. These bits select the type and operation of the on-chip cursor.

Internal Registers (continued)

Register Descriptions (continued)

Table 12. Control Register 3

This register is operational on powerup. It can be read or written to by the MPU at any time and is not initialized. All bits are set to 0 upon asserting RESET. To read or write to this register, set bit CR0[7] to a logic 1 and AD[3:0] to 1010 (see Table 6).

Bit	Name/Description
CR3[7:6]	**Reserved.** Logic 0: Does not affect operation. Logic 1: Does not affect operation. These bits may be read and will return the value written, but will not affect the function of the device.
CR3[5]	**SCLK Invert** Logic 0: Does not affect operation of SCLK (relative to rising edge). Logic 1: Inverts the SCLK output (relative to falling edge). This bit inverts the SCLK output when equal to one, and the dead zone will start relative to the falling edge of SCLK. When equal to zero, the dead zone will start relative to the rising edge of SCLK. This increases compatibility with graphics controllers by easing time constraints.
CR3[4]	**Nibble Swap for 4-Bit Pixel Operation.** Logic 0: Most significant nibble first. Logic 1: Least significant nibble first. These bits set the nibble order for the 4-bit per pixel mode. A logic 0 causes the four high-order bits to be multiplexed before the four low-order bits. A logic 1 causes the four low-order bits to be multiplexed before the four high-order bits (see Table 16).
CR3[3]	**Internal Clock Doubler (ATT21C505 only).** Logic 0: Disable. Logic 1: Enable. A logic 1 enables the clock doubler, allowing the internal circuitry of the RAMDAC to run at twice the input pixel clock speed. The 2x clock doubler must be used for pixel clock inputs above 110 MHz.
CR3[2]	**Cursor Size.** Logic 0: 32 x 32 x 2 (ATT20C504 default cursor size). Logic 1: 64 x 64 x 2 (ATT21C505/504 only). If this bit is logic 0, the ATT21C505/504 will have a 32 x 32 x 2 cursor. For a logic 1, the ATT21C505/504 will have a 64 x 64 x 2 cursor.
CR3[1:0]	**MSBs for 10-Bit Address Counter (ATT21C505 only).** CR3[1]: ADDR9. CR3[0]: ADDR8. These bits are the high-order address bits of the address register specifically for use when writing the 64 x 64 cursor pattern RAM. These bits will autoincrement when WR1/RD1 or WR2/RD2 = $FF. (The full 10-bit address counter autoincrements.)

Internal Registers (continued)

Register Descriptions (continued)

Table 13. Status Register (AD[3:0] = 1010)

The status register is read only. This register is accessed directly with AD[3:0] = 1010 and CR0[7] = 0 or indirectly with CR0[7] = 1 (see Tables 3 and 6).

Bit	Name/Description
ST[7:4]	**Identification and Device Type.** ST[7:4] = 1101: ATT21C505. ST[7:4] = 0100: ATT20C504. These bits indicate the device type.
ST[3]	**Sense.** ST[3] = 0: One or more outputs greater than internal reference level. ST[3] = 1: Outputs are less than internal reference level. A logic low on this bit indicates whether one or more of the R, G, B outputs have exceeded the internal voltage reference level of 340 mV (see dc characteristics tables under Electrical Characteristics for tolerance specs). This is used to determine the presence of an external monitor (see Figure 3).
ST[2]	**MPU Cycle Status.** ST[2] = 0: Write cycle. ST[2] = 1: Read cycle. This bit indicates whether an MPU read or an MPU write cycle is taking place when accessing the address register. When address registers $0 or $4 have been written, ST[2] will be logic 0. When address registers $3 or $7 have been written, ST[2] will be a logic 1.
ST[1:0]	**Modulo 3 Counter State.** ST[1:0] = 00: Write red. ST[1:0] = 01: Write green. ST[1:0] = 10: Write blue. The modulo three counter state indicates which of the R, G, and B color values are being written to the color, overlay, or overscan RAMs.

Internal Registers (continued)

Register Descriptions (continued)

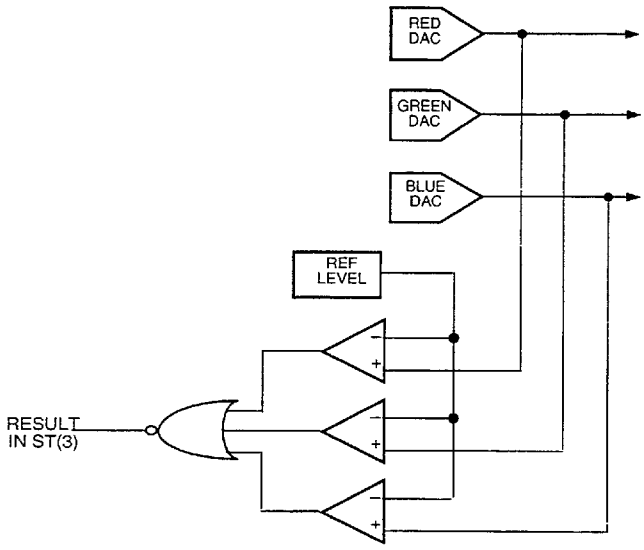


Figure 3. DAC Output Comparison Circuitry

Cursor Position Registers

The cursor position registers are made up of four registers. The X position register has a low byte, X-low, and a high byte, X-high. The Y position register has a low byte, Y-low, and a high byte, Y-high. Each byte of the X, Y position registers has a unique address in the register address map (see Table 3). The registers can be accessed at any time and are not initialized upon powerup or reset.

The two X position bytes form a 12-bit address allowing cursor positioning at 4096 pixels. This is sufficient pixel space to allow positioning the cursor off the screen in the X direction. The two Y position bytes form a 12-bit address allowing cursor positioning at 4096 lines. This is a sufficient number of lines to allow positioning the cursor off the screen in the Y direction. The upper nibble of both the X-high and Y-high position registers is ignored (see Table 14).

Placing the Cursor

The cursor is referenced to the upper left corner of the screen (see Figure 7). The cursor origin (position X = 0, Y = 0) is referenced to VEX deactivating. The cursor reference point is in the bottom right corner of the cursor. This allows the cursor to be positioned off the screen when the position is X = 0, Y = 0. The position registers move the cursor by increasing or decreasing the X and Y distances from the cursor origin to the cursor reference point. To place a 64 x 64 cursor in the upper left corner of the screen, program X = 64 and Y = 64 into the X and Y position registers. To place a 32 x 32 cursor in the upper left corner of the screen, program X = 32 and Y = 32 into the X and Y position registers.

To place the top left corner of the cursor, the size of the cursor must be subtracted. For a 64 x 64 cursor, 64 must be subtracted from the X direction and 64 must be subtracted from the Y direction. For a 32 x 32 cursor, 32 must be subtracted from the X direction and 32 must be subtracted from the Y direction (see Figure 7).

- $X' = X - (64 \text{ or } 32)$
- $Y' = Y - (64 \text{ or } 32)$

Use the equations above to position the top left corner of the cursor where X′ and Y′ are the coordinates of the top left corner of the cursor.

Table 14. X, Y Cursor Position Registers

This table shows the mapping of MPU port bits to the cursor X and Y position registers. Each location, X-low, X-high, Y-low, and Y-high, has a unique address in the register map.

	X-High								X-Low							
MPU	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Value	—	—	—	—	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
	Y-High								**Y-Low**							
MPU	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Value	—	—	—	—	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

Internal Registers (continued)

Test Registers

The red, green, and blue test registers allow two test operations. The test registers will analyze red, green, or blue signatures by using linear feedback shift registers (LFSRs). The test registers will also read the red, green, and blue DAC inputs.

Control bit CR2[6] = 0 sets the test registers for signature analysis. During signature analysis, the R, G, and B data is sampled and compressed at the pixel clock frequency. The test register can be read or written only during the blanking interval. During active video, the signatures are being accumulated. The signature is accumulated based on the initial seed value. A new seed value is produced every pixel clock. On writing a seed value to the test register, the red, green, and blue test registers are all seeded with the same value. Reading the test register three times will produce the red, green, and blue signatures. The first value read is the red signature followed by the green and blue signatures.

Control bit CR2[6] = 1 sets the test registers for reading the DAC inputs. The test register, when set for the DAC inputs, is read in the same manner as when in the signature analysis mode. The first read to the test register results in the red DAC input, the second results in the green DAC input, and the third results in the blue DAC input. It should be noted that the MPU port will not operate at the high-speed pixel clock rate. The pixel clock must be slowed down or the MPU port synchronized with the pixel port.

The test register is read or written indirectly (see Table 6).

Functional Description

Color Modes

The ATT21C505/504 provides nine different color modes that are selectable by programming the device (see Table 15). The modes are programmed by the control register bits and by control pins on the device. All modes can use the color look-up tables (CLUTs). The 24-, 16-, and 15-bit modes can bypass the CLUT and present pixel data directly to the DACs. When multiple pixels are presented to the device in parallel, a latch and multiplexer will serialize them. An explanation of each mode follows.

Table 15. Multiplex Ratio vs. Bit Per Pixel

MUX Ratio*	Bits Per Pixel						
	True Color				Pseudocolor		
	24	18	16	15	8	4	1
1:1	X	X	X	X			
2:1			X	X			
4:1					X		
8:1						X	
32:1							X

* Pixels per load.

SVGA Input, 8 bpp: One 8-bit pixel is latched on the rising edge of LOAD. One pixel clock should occur for every LOAD clock. SCLK will be equal to the pixel clock. There are 256 simultaneous colors in this mode. This mode operates through the CLUT only. The pixel read mask register is active. If 6-bit DACs are programmed, there are 256 simultaneous colors out of 256K possible.

A logic 0 on $\overline{\text{VGA}}$ and a logic 1 in bit CR2[5] ensures that the SVGA inputs are selected. To switch between V[7:0] (SVGA) and the pixel inputs on a pixel-by-pixel basis, the device must be configured for 1:1 multiplexed operation, and the palette bypass must be enabled. The $\overline{\text{VGA}}$ pin controls the real-time switching. Frame-by-frame switching may be used in 2:1, 4:1, and 8:1 multiplexing modes.

32:1 Multiplex, 1 bpp: Thirty-two 1-bit pixels are latched on the rising edge of LOAD. Thirty-two pixel clocks should occur for every LOAD clock. SCLK will be the internal pixel clock divided by 32. There are two simultaneous colors out of 16M in this mode. This mode operates through the CLUT. The 1-bit pixel address selects between location 0 or location 1 in the pixel color RAM.

4:1 Multiplex, 8 bpp: Four 8-bit pixels are latched on the rising edge of LOAD. The division and sequencing of the 32 pixel inputs are outlined in Table 16. Four pixel clocks should occur for every LOAD clock. SCLK will be the internal pixel clock divided by four. There are 256 simultaneous colors out of 16M in this mode. This mode operates through the CLUT.

8:1 Multiplex, 4 bpp: Eight 4-bit pixels are latched on the rising edge of LOAD. The nibbles can be multiplexed in a little-endian or big-endian fashion. The division and sequencing of the 32 pixel inputs are shown in Table 16. Eight pixel clocks should occur for every LOAD clock. SCLK will be the internal pixel clock divided by eight. There are 16 simultaneous colors out of 16M in this mode. This mode operates through the CLUT.

Functional Description (continued)

Color Modes (continued)

2:1 Multiplex, 16 bpp: Two 16-bit pixels are latched on the rising edge of LOAD. Two pixel clocks should occur for every LOAD clock. SCLK will be equal to the internal pixel clock divided by two. There are 64K (5-6-5) or 32K (5-5-5) simultaneous colors in this mode. This mode operates through the CLUT or directly to the three DACs. In bypass operation, the pixel read mask register is also bypassed. If 6-bit DACs are programmed, this color mode is not affected.

When bypass is enabled, each DAC will receive 5 bits of color information in 5-5-5 mode. In 5-6-5 mode, the green DAC will receive 6 bits of color information and the red and blue DACs will receive 5 bits of color information. Control register bit CR1[4] controls whether the CLUT is bypassed. In CLUT mode, the pixel information is used as an address to look up 8 bits of information each for red, green, and blue DAC.

There are two addressing modes when in CLUT mode. In the first mode, the pixel addresses are shifted to the LSBs of address to the color RAM. In the second mode, the pixel addresses are shifted to the MSBs of address to the color RAM. The first mode is often referred to as packed because all address locations are sequential in the CLUT. The second mode is sometimes referred to as spaced because the locations in the CLUT are separated by the number of locations indicated by the LSBs. For example, a 5-5-5 mode would have three 0 LSBs and each CLUT value would be eight locations from the next. In 5-5-5 format, PD7 and PB7 are ignored.

In 2:1 multiplex mode, switching between the pixel inputs and V[7:0] on a pixel-by-pixel basis is not supported. In 5-5-5 format, bits CR1[1:0] and PD7 are disabled. In 5-6-5 format, CR1[1:0] are disabled and PD7 contains pixel data.

1:1 Multiplex, 16 bpp: One 16-bit pixel is latched on the rising edge of LOAD, and one pixel clock should occur for every LOAD clock. SCLK will be equal to the pixel clock. There are 64K (5-6-5) or 32K (5-5-5) simultaneous colors in this mode. This mode operates through the CLUT or directly to the three DACs. In bypass operation, the pixel read mask register is also bypassed. If 6-bit DACs are programmed, this color mode is not affected.

When bypass is enabled, each DAC will receive 5 bits of color information in 5-5-5 mode. In 5-6-5 mode, the green DAC will receive 6 bits of color information and the red and blue DACs will receive 5 bits of color information. Control register bit CR1[4] controls whether the CLUT is bypassed. In CLUT mode, the pixel information is used as an address to look up 8 bits of information each for red, green, and blue DAC.

There are two addressing modes when in CLUT mode. The first mode is packed colors, and the pixel addresses are shifted to the LSBs of the pixel color RAM address register. The second mode is spaced colors, and the pixel addresses are shifted to the MSBs of the pixel color RAM address register. The first mode is often referred to as packed because all address locations are sequential in the CLUT. The second mode is sometimes referred to as spaced because the locations in the CLUT are separated by the number of locations indicated by the LSBs. For example, a 5-5-5 mode would have three LSBs and each CLUT value would be eight locations from the next.

In 5-5-5 format, the pixel input can be switched on a real-time basis (pixel by pixel) between P[A:B] or P[C:D]. Switching on a real-time basis is controlled by PD7 and enabled by bit CR1[1] (see Figure 4). Real-time pixel input switching is not available in 5-6-5 format. In nonreal time, bit CR1[0] controls pixel input switching between P[A:B] [7:0] and P[C:D][7:0]. Bit CR1[0] is enabled by CR1[1]. In nonreal-time mode, switching between 5-5-5 and 5-6-5 formats is allowed. PB7 is ignored in 5-5-5 format.

Both 5-5-5 and 5-6-5 formats support switching pixel inputs between the SVGA inputs V[7:0] and the pixel inputs P[A:D] [7:0] on a pixel-by-pixel basis. When switching the V[7:0] inputs with the pixel inputs, CR2[5] must be high. The $\overline{VGA}$ input pin controls real-time switching in this case. If CR2[5] is low, then the V[7:0] inputs will be active and P[A:D], [7:0] will be gated off.

1:1 Multiplex, 24 bits per pixel (bpp): One 24-bit pixel is latched on the rising edge of LOAD. One pixel clock should occur for every LOAD clock. SCLK will be equal to the pixel clock. PCLK0 or PCLK1 must be active for SCLK to be active. There are 16 million simultaneous colors in this mode, and it operates through the CLUT or directly to the three DACs (see CR1[4]). Each DAC will receive a byte of color information (see Table 19 for RGB encoding). In bypass operation, the pixel read mask register is also bypassed. If 6-bit DACs are programmed, 256K simultaneous colors out of 16M will be displayed. The $\overline{VGA}$ pin allows real-time switching between the SVGA port and 24-bit pixels.

Functional Description (continued)

Color Modes (continued)

Table 16. Color and Multiplex Modes

The following table details the color and multiplex modes of the ATT21C505/504. These modes are set by bits in the control register and external pins.

Mode	Description		Port Enable	Port Switch	SW Control	SW Port		16-Bit MUX	16-Bit Form	Pixel Width	Nibble Swap
	Function		0 = VGA 1 = Both	LO = VGA HI = Wide	0 = CR1[0] 1 = PD7	0 = A:B 1 = C:D		0 = 2:1 1 = 1:1	0 = 555 1 = 565	000 = 24 001 = 16 010 = 8 011 = 4 100 = 1	
	MUX Ratio	Pins MUXed	CR2[5]	VGA	CR1[1]	CR1[0]	PD7	CR1[2]	CR1[3]	CR1[7:5]	CR3[4]
VGA	1:1	V[7:0]	0	X	X	X	X	X	X	XXX	X
VGA	1:1	V[7:0]	X	0	X	X	X	X	X	XXX	X
1 Bit Per Pixel	32:1	PA7 PA6 : PA0 PB7 : PD0	1	1	X	X	data	X	X	100	X
4 Bits Per Pixel Most Significant Nibble First	8:1	PA[7:4] PA[3:0] PB[7:4] PB[3:0] PC[7:4] PC[3:0] PD[7:4] PD[3:0]	1	1	X	X	data	X	X	011	0
4 Bits Per Pixel Least Significant Nibble First	8:1	PA[3:0] PA[7:4] PB[3:0] PB[7:4] PC[3:0] PC[7:4] PD[3:0] PD[7:4]	1	1	X	X	data	X	X	011	1
8 Bits Per Pixel	4:1	PA[7:0] PB[7:0] PC[7:0] PD[7:4]	1	1	X		data	X	X	010	X

Functional Description (continued)

Color Modes (continued)

Table 16. Color and Multiplex Modes (continued)

Mode	Description		Port Enable	Port Switch	SW Control	SW Port		16-Bit MUX	16-Bit Form	Pixel Width
	Function		0 = VGA 1 = Both	LO = VGA HI = Wide	0 = CR10 1 = PD7	0 = B:A 1 = D:C		0 = 2:1 1 = 1:1	0 = 555 1 = 565	000 = 24 001 = 16 010 = 8 011 = 4 100 = 1
	MUX Ratio	Pins MUXed	CR2[5]	VGA	CR1[1]	CR1[0]	PD7	CR1[2]	CR1[3]	CR1[7:5]
15 Bits Per Pixel (5-5-5) Multiplexed	2:1	P[A:B], [7:0] P[C:D], [7:0]	1	1	X	X	X	0	0	001
16 Bits Per Pixel (5-6-5) Multiplexed	2:1	P[A:B], [7:0] P[C:D], [7:0]	1	1	X	X	data	0	1	001
15 Bits Per Pixel (5-5-5) Nonreal-time Switch	1:1	P[A:B], [7:0]	1	1	0	0	X	1	0	001
15 Bits Per Pixel (5-5-5) Nonreal-time Switch	1:1	P[C:D], [7:0]	1	1	0	1	X	1	0	001
15 Bits Per Pixel (5-5-5) Real-time Switch	1:1	P[A:B], [7:0]	1	1	1	X	0	1	0	001
15 Bits Per Pixel (5-5-5) Real-time Switch	1:1	P[C:D], [7:0]	1	1	1	X	1	1	0	001
16 Bits Per Pixel (5-6-5) Nonreal-time Switch	1:1	P[A:B], [7:0]	1	1	X	0	data	1	1	001
16 Bits Per Pixel (5-6-5) Nonreal-time Switch	1:1	P[C:D], [7:0]	1	1	X	1	data	1	1	001
24 Bits Per Pixel	1:1	P[A:C], [7:0]	1	1	X	X	X	X	X	000

Functional Description (continued)

Color Modes (continued)

Table 17. Pixel Color Format for 16 Bits Per Pixel with RGB = 5-6-5

	5					6						5				
Port 1	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Pins	**PB7**	**PB6**	**PB5**	**PB4**	**PB3**	**PB2**	**PB1**	**PB0**	**PA7**	**PA6**	**PA5**	**PA4**	**PA3**	**PA2**	**PA1**	**PA0**
Pixel	R7	R6	R5	R4	R3	G7	G6	G5	G4	G3	G2	B7	B6	B5	B4	B3
Port 2	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17
Pins	**PD7**	**PD6**	**PD5**	**PD4**	**PD3**	**PD2**	**PD1**	**PD0**	**PC7**	**PC6**	**PC5**	**PC4**	**PC3**	**PC2**	**PC1**	**PC0**
Pixel	R7	R6	R5	R4	R3	G7	G6	G5	G4	G3	G2	B7	B6	B5	B4	B3

Table 18. Pixel Color Format for 16 Bits Per Pixel with RGB = 5-5-5

	Switch	5					5					5				
Port 1	**16**	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Pins	**PB7**	**PB6**	**PB5**	**PB4**	**PB3**	**PB2**	**PB1**	**PB0**	**PA7**	**PA6**	**PA5**	**PA4**	**PA3**	**PA2**	**PA1**	**PA0**
Pixel	X	R7	R6	R5	R4	R3	G7	G6	G5	G4	G3	B7	B6	B5	B4	B3
Port 2	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17
Pins	**PD7***	**PD6**	**PD5**	**PD4**	**PD3**	**PD2**	**PD1**	**PD0**	**PC7**	**PC6**	**PC5**	**PC4**	**PC3**	**PC2**	**PC1**	**PC0**
Pixel	SW	R7	R6	R5	R4	R3	G7	G6	G5	G4	G3	B7	B6	B5	B4	B3

* PD7 is an active switch between port A:B and port C:D when CR1[1] = 1.

Table 19. Pixel Color Format for 24 Bits Per Pixel

	Byte 1								Byte 0							
Port 1	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Pin #	**PB7**	**PB6**	**PB5**	**PB4**	**PB3**	**PB2**	**PB1**	**PB0**	**PA7**	**PA6**	**PA5**	**PA4**	**PA3**	**PA2**	**PA1**	**PA0**
G, B	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
	Byte 3								**Byte 2**							
Port 2	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17
Pin #	**PD7**	**PD6**	**PD5**	**PD4**	**PD3**	**PD2**	**PD1**	**PD0**	**PC7**	**PC6**	**PC5**	**PC4**	**PC3**	**PC2**	**PC1**	**PC0**
X, R	X	X	X	X	X	X	X	X	R7	R6	R5	R4	R3	R2	R1	R0

Functional Description (continued)

Color Modes (continued)

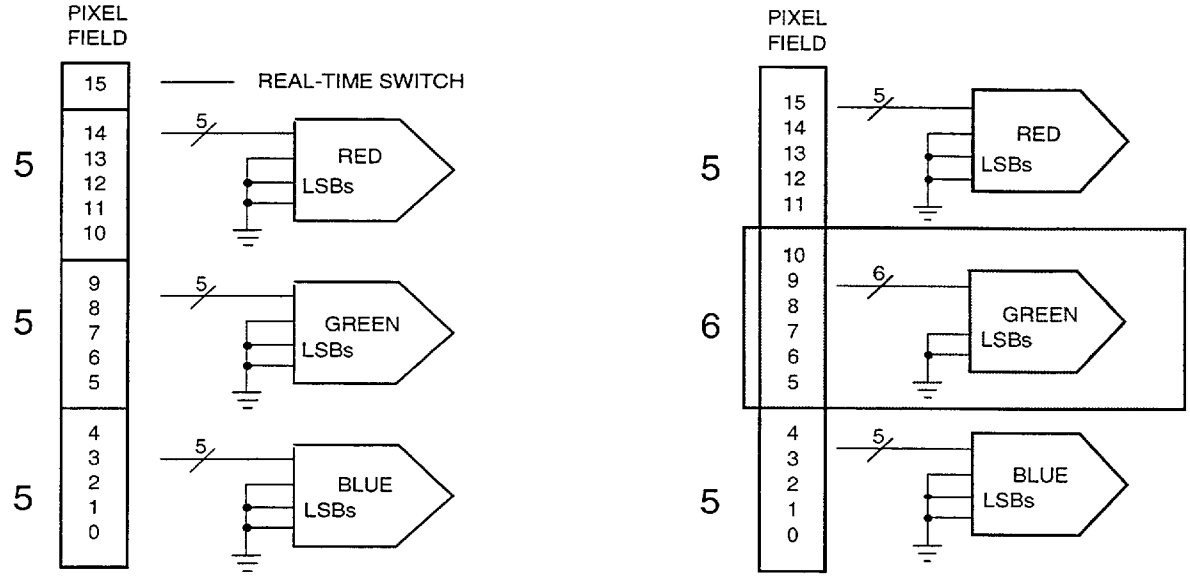


Figure 4. Field Split for 16-Bit 5-5-5 and 16-Bit 5-6-5 True-Color Modes

Hardware Cursor

The hardware cursor consists of a 64 x 64 x 2 pattern RAM, a 3 x 24 cursor color RAM, and X, Y coordinate registers. The cursor may be downsized to 32 x 32 x 2 by setting control bit CR3[2] = 0. The cursor pattern RAM is located in the register map at AD[3:0] = 1011. The addressing for this map location is indicated in Figures 5 and 6 and Table 20.

The cursor pattern is a planar format with 2 bits per cursor pixel. Plane 1 is the MSB, and plane 0 is the LSB. The cursor pattern is written by writing plane 0 first, and then plane 1. The first 4 bytes written to the 32 x 32 cursor are the first line of plane 0. Bit D7 of the MPU port corresponds to the MSB of the cursor pattern byte values (see Figure 5). Bytes 128 through 131 are the first line of plane 1. Address bit 7 functions as the plane select.

The 64 x 64 cursor pattern is a similar planar format with 2 bits per cursor pixel. Plane 1 is the MSB, and plane 0 is the LSB. The cursor is written by writing plane 0 first, and then plane 1. The first 8 bytes written to the 64 x 64 cursor are the first line of plane 0 (see Figure 6). Bytes 512—519 are the first line of plane 1. Address bit 9 functions as the plane select.

Address bit 8 (CR3[0]) and address bit 9 (CR3[1]) are accessed through control register 3. CR3[0] and CR3[1] are automatically updated by the auto-increment logic. Address bits CR3[0] and CR3[1] are ignored when the 32 x 32 cursor is selected (see Table 20).

The cursor is written by using the address register which increments after each write to the cursor pattern RAM. In this process, the 32 x 32 cursor or the 64 x 64 cursor can be written as blocks of data without updating the address register. The address register will autowrap the full 10-bit address counter, automatically updating CR3[1:0]. The address register autoincrement logic will not reset when read, but will reset when written. Note that the address register, ADDR1, is common to the pixel color and cursor pattern RAMs in the register map.

Cursor X, Y Positioning

The X, Y position registers determine the location of the cursor. The position registers are 12 bits, allowing programming up to a 4096 x 4096 screen resolution. Each X and Y consist of a high and low byte. The upper nibble of the high byte is ignored (see Table 14).

Functional Description (continued)

Hardware Cursor (continued)

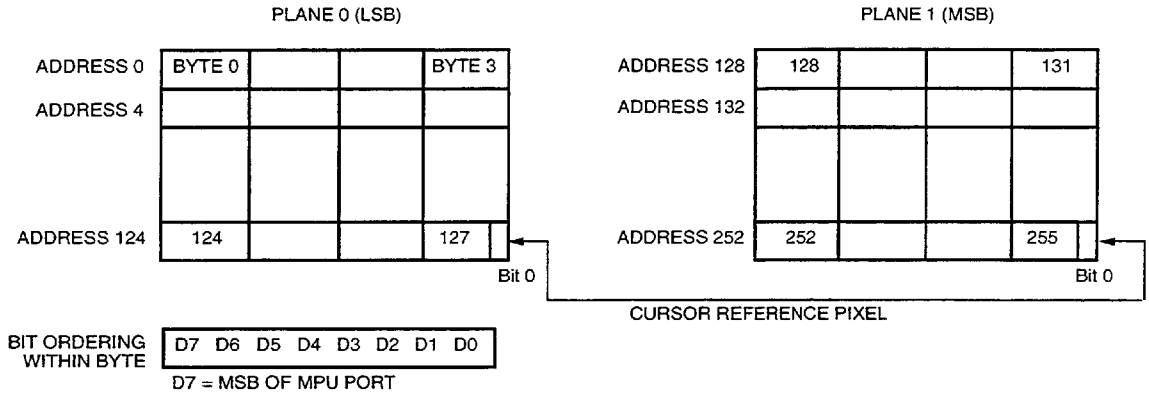


Figure 5. 32 x 32 Cursor Pattern RAM Memory Mapping

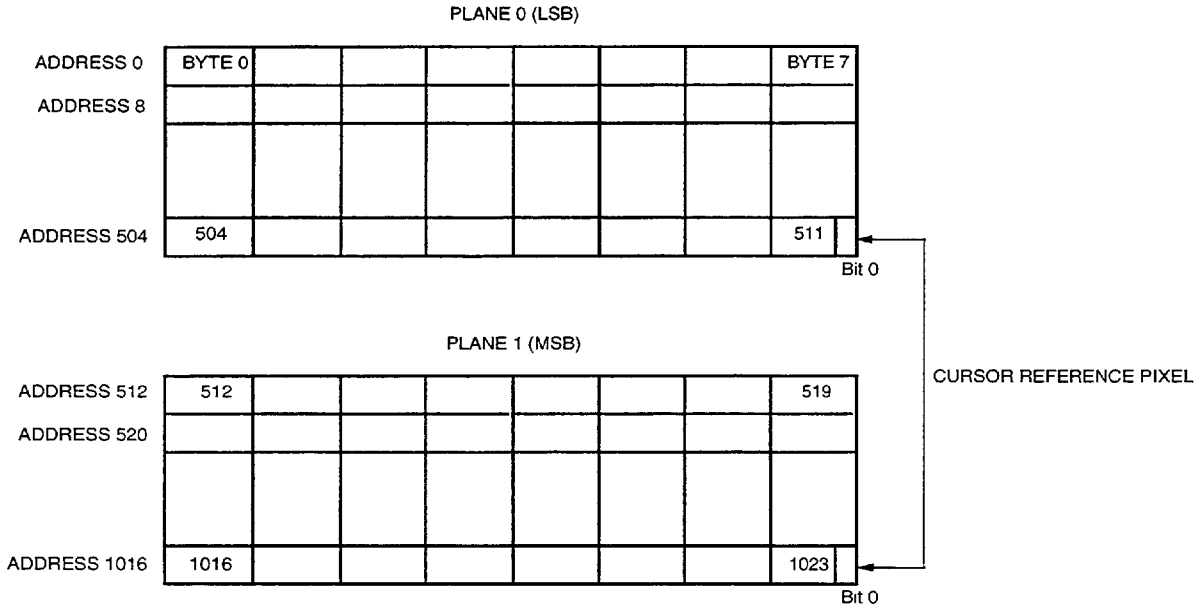


Figure 6. 64 x 64 Cursor Pattern RAM Memory Mapping

Table 20. Cursor Pattern RAM Addressing

CR3[1] ADDR9	CR3[0] ADDR8	WR[7:0] or RD[7:0]	Addressed by MPU
X	X	$00—$7F	Plane 0 (32 x 32 cursor)
X	X	$80—$FF	Plane 1 (32 x 32 cursor)
0	0	$00—$FF	Plane 0, first half (64 x 64 cursor)
0	1	$00—$FF	Plane 0, second half (64 x 64 cursor)
1	0	$00—$FF	Plane 1, first half (64 x 64 cursor)
1	1	$00—$FF	Plane 1, second half (64 x 64 cursor)

Functional Description (continued)

Hardware Cursor (continued)

The cursor position is updated only after the Y-high byte is written and a new frame has started. The cursor is displayed once per frame. If the Y-high position register is updated during cursor display, the new cursor position will be displayed during the following frame. The cursor position is determined by counting PCLKs in 32:1, 8:1, 4:1, or 2:1 modes and by counting LOAD in the 1:1 modes. The ATT21C505/504 determines a vertical blank period by counting PCLKs (or LOAD in 1:1 mode) while VEX is low. If VEX does not rise during 2048 PCLKs (or LOADs), the device determines it is in a vertical blanking period. The cursor position is gated by VEX going high and is relative to the first rising edge of LOAD. Cursor position is not dependent on BLANK .

The origin (X = 0, Y = 0) of the cursor is the bottom right cursor corner. The origin of pixels (pixel position X = 0, Y = 0) on the CRT screen is the upper left corner. Writing 0, 0 to the cursor position registers moves the cursor off screen. Writing 64, 64 (or 32, 32) to the cursor position registers prompts the entire cursor to fill the top left portion of the screen (see Figure 7).

Interlaced Systems

Interlaced systems are supported with control register bit CR2[3] and control pin FIELD . CR2[3] sets the cursor logic to display every other line of the cursor. The FIELD pin indicates whether the odd or even cursor lines are to be displayed.

The $\overline{\text{FIELD}}$ input is latched on the first rising edge of LOAD that is sampled high after the RAMDAC senses a vertical blanking interval (see Figure 8).

The $\overline{\text{FIELD}}$ input is latched with respect to the LOAD signal. The ac timing requirements for the FIELD input are 3 ns setup and 3 ns hold, with respect to the rising edge of the load input. When FIELD is sampled high, an odd line of the cursor will be presented. When FIELD is sampled low, an even line of the cursor is presented.

If the Y position is >64 ($0040) and ≤4095 ($0FFF), the first line of the cursor displayed depends on the value of FIELD and the value of the Y position. If the Y position is an even number, line 63 of the cursor (cursor pixel 64, 64) will be displayed during the even field starting at screen position X-64, Y-64. Every other line of the cursor will be displayed as the frame progresses. During the odd field, cursor line 62 (cursor pixel 63, 63) is displayed. Following line 62, every other line of the cursor is displayed (line 60, 58, 56, etc.).

If the Y position is an odd number, then line 63 of the cursor (cursor pixel 64, 64) will be displayed during the odd field starting at screen position X-64, Y-64. Every other line of the cursor will be displayed as the frame progresses. During the even field, cursor line 62 (cursor pixel 63, 63) is displayed. Following line 62, every other line of the cursor is displayed (line 60, 58, 56, etc.)

If the Y position is less than 64, but greater than 0, the cursor is displayed on scan line 0 for even frames. For odd frames, the cursor will be displayed on scan line 1 if the Y position is less than 65, but greater than 1. Every other line of the cursor is displayed until the end of the cursor pattern is reached. The 32 x 32 cursor operates in a similar fashion, but with all numbers changed to fit the smaller size cursor.

Functional Description (continued)

Hardware Cursor (continued)

Table 21. Cursor Type and Operation

2-Bit Address from Cursor Pattern RAM	CR2[1:0] = 00 Mode 0 Disable	CR2[1:0] = 01 Mode 1 3-Color	CR2[1:0] = 10 Mode 2 *Windows*	CR2[1:0] = 11 Mode 3 *X-Windows*
00	Disable	Palette data	Cursor color 1	Palette data
01	Disable	Cursor color 1	Cursor color 2	Palette data
10	Disable	Cursor color 2	Palette data	Cursor color 1
11	Disable	Cursor color 3	Complement	Cursor color 2

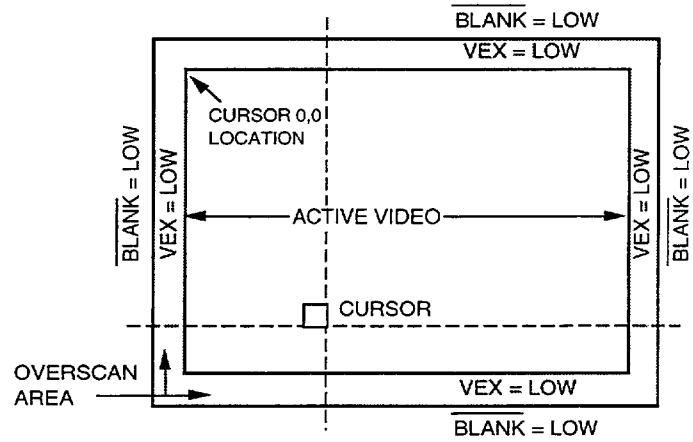


Figure 7. Cursor Positioning in Active Pixel Area

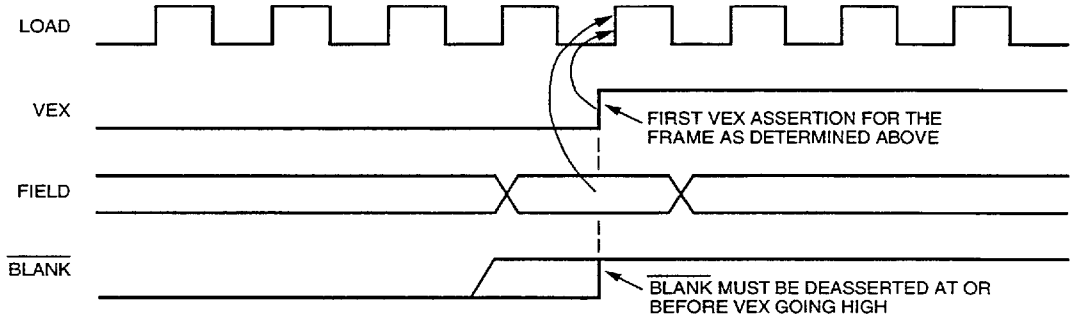


Figure 8. Sampling of the FIELD Pin Signal

Functional Description (continued)

Hardware Cursor (continued)

Cursor Color

The cursor pattern RAM provides a 2-bit address for the cursor color RAM. Only three colors are available; the cursor color 0 is reserved for the overscan color. The cursor address bits look up a 24-bit cursor color. This provides three colors out of 16.8 million.

The cursor type bits CR2[1:0] control whether the cursor is a *Windows*, *X-Window*, or three-color cursor. If CR2[1:0] = 00, the cursor is disabled (see Table 21). While in mode 2, the cursor pattern RAM address 11 causes logic to complement the data stored in the cursor color RAM. This is compatible with *Microsoft** *Windows*.

* *Microsoft* is a registered trademark of Microsoft Corporation.

Table 22. Pixel Input and Control Pins

Note: The $\overline{\text{VGA}}$ pin is ANDed with CR2[5].

Screen Contents	$\overline{\text{VGA}}$	VEX	$\overline{\text{BLANK}}$
Video Blanking	X	X	0
VGA Pixels	0	0	1
VGA Pixels or Cursor	0	1	1
Overscan	1	0	1
Pixel Inputs or Cursor	1	1	1

Graphics and Control Input Pins (Fast Port Interface)

The graphics and control input pins consist of the pixel inputs P[A:D][7:0], the SVGA pixel inputs V[7:0], and the $\overline{\text{VGA}}$, VEX, $\overline{\text{FIELD}}$, $\overline{\text{SYNC}}$, and $\overline{\text{BLANK}}$ control inputs. The $\overline{\text{VGA}}$ pin allows real-time switching between the V[7:0] (super VGA) pins and P[A:D][7:0] pixel input pins.

The VEX pin controls switching between overscan and active video. The VEX pin is enabled when using the pixel input pins P[A:D][7:0] and is disabled when operating in the SVGA mode. The cursor is referenced to the rising edge of VEX. Overscanning is allowed only in pixel mode when using the P[A:D][7:0] inputs (see Table 16).

The sequencing of P[A:D][7:0] depends on the multiplexing ratio. For example, in 4:1 multiplexing, 4 bytes are sequenced ABCD (see Table 16 for complete details on pixel sequencing and multiplexing). PD7 can be used to switch real time between pixel inputs P[A:B][7:0] and P[C:D][7:0] in 15-bit pixel format and 1:1 MUX mode.

Pixel Flow

To maintain synchronization, the rising edge of LOAD latches P[A:D][7:0], V[7:0], VEX, $\overline{\text{SYNC}}$, and $\overline{\text{BLANK}}$ inputs. The pixels are multiplexed and are sent to the DACs as color data (bypass mode) or sent to the pixel read mask registers as addresses and then to the color RAMs (see Table 16).

Color RAM Addressing

The color look-up tables (CLUTs) can be addressed two ways. The first method is packed addressing. When accessing the CLUTs by using packed addressing, the address bits are applied to the LSBs of the CLUT address. Only the lower locations of the CLUT are accessed. The second method is spaced addressing. When accessing the CLUTs by using spaced addressing, the address bits are applied to the MSBs of the CLUT address. The CLUT locations are evenly spaced from address $00 to address $FF with the locations between left unused.

Functional Description (continued)

Graphics and Control Input Pins (Fast Port Interface) (continued)

$\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ are pipelined with the pixel data and add appropriately weighted currents to the analog outputs to produce the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ pedestal currents (see Figures 12, 13, and 14 and Tables 25 and 26). The analog outputs are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable (see Figure 16).

Positive or Negative $\overline{\text{SYNC}}$

The $\overline{\text{SYNC}}$ signal may be a positive or negative pulse. The ATT21C505/504 samples and stores the logic value of $\overline{\text{SYNC}}$ every rising edge of LOAD. When $\overline{\text{BLANK}}$ falls, the logic value latched on the previous LOAD is determined to be the inactive state of $\overline{\text{SYNC}}$ (see Figure 9). When $\overline{\text{SYNC}}$ changes logic value, the $\overline{\text{SYNC}}$ current sources are turned off, sending the video signal to the $\overline{\text{SYNC}}$ level. For systems having $\overline{\text{SYNC}}$ signals separate from the RAMDAC, disable $\overline{\text{SYNC}}$ by programming CR0[4:2] = 000.

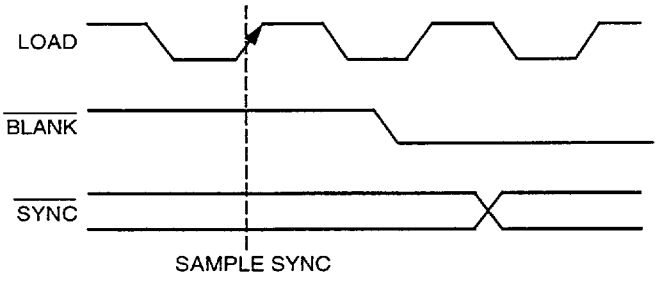


Figure 9. SYNC

Clocking

The ATT21C505/504 has four clock pins and an internal 2x clock doubler. Three of the clock pins, PCLK0, PCLK1, and LOAD, are inputs, and the SCLK pin is an output meant to drive the VRAM shift clock (see Figure 10).

Pixel clock PCLK0 or PCLK1 is selected by setting control register bit CR2[4]. The pixel clock controls the pixel rate. The LOAD clock latches in multiple pixels in parallel which are then serialized and clocked out at the pixel rate. The LOAD clock runs at the same pixel rate or at 1/2, 1/4, 1/8, or 1/32 of the pixel clock rate, depending on the multiplexing ratio. For a multiplexing ratio of 8:1, the LOAD clock must run at 1/8 the pixel clock. In 1:1 MUX mode, LOAD clocks the RAMDAC and PCLK0 or PCLK1 needs to be toggled only if the SCLK output is desired.

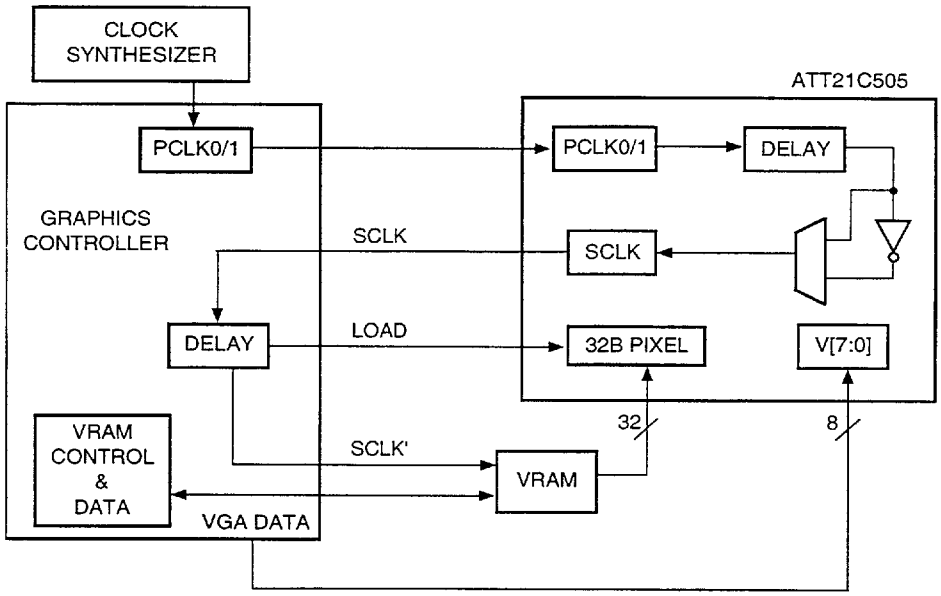
The VRAM shift clock, SCLK, is an output for clocking the VRAMs. SCLK will also correspond to the multiplexing ratio. For example, SCLK will be 1/8 the pixel clock for an 8:1 multiplex ratio. Refer to the ac characteristics tables under Electrical Characteristics for shift clock delays.

There is a time during the SCLK cycle in which LOAD must not rise (see Figure 11). If the rising edge of LOAD occurs before the forbidden time, the pixel and control inputs will be internally synchronized to the next rising edge of SCLK. If the rising edge of LOAD occurs after the forbidden time, the pixel and control inputs will be internally synchronized to the second rising edge of SCLK. Parameter 11 in Figure 11 is the LOAD rising edge setup to SCLK rising edge. Parameter 10 is LOAD rising edge hold-off to SCLK rising edge.

Control register bit CR3[3] = 1 enables the internal 2x clock doubler. Using this doubler is recommended whenever a pixel clock over 110 MHz is needed. The 2x clock doubler multiplies the incoming pixel clock by two. Either PCLK0 or PCLK1 is doubled when CR3[3] is a logic 1. This is useful for multiplexed pixel inputs and high-speed pixel output, to achieve high-resolution displays. For 135 MHz operation, the pixel clock will be 67.5 MHz. For 170 MHz operation, the pixel clock will be 85 MHz. The multiplex rate and doubler determine the LOAD rate. For a multiplex ratio of 2:1, the LOAD clock = pixel clock = SCLK = 67.5 MHz. For a multiplex ratio of 8:1, the pixel clock = 67.5 MHz, LOAD clock = SCLK = 16.9 MHz.

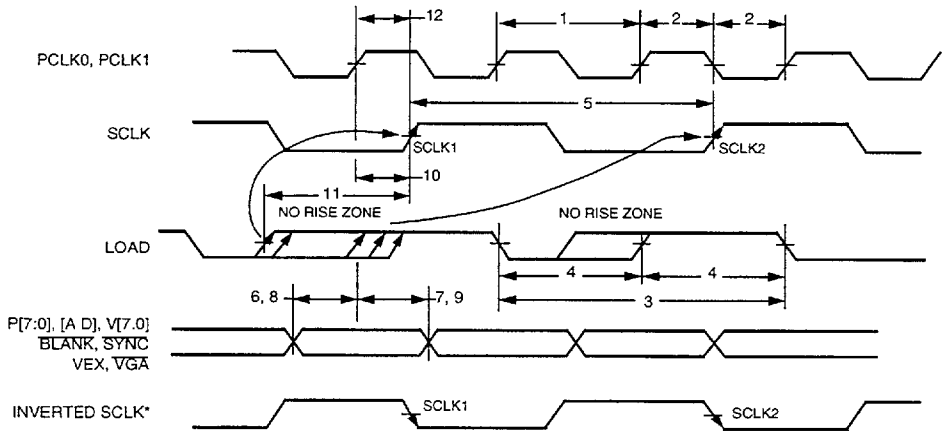
Functional Description (continued)

Clocking (continued)



Note: Control of LOAD clock to SCLK timing is critical.

Figure 10. System Block Diagram



* SCLK can be inverted by setting CR3[5] = 1. In this case, all references to the rising edge of SCLK are made to the falling edge of the inverted SCLK.

Notes:
LOAD rising edge must occur before parameter 11 in the figure above. The next LOAD rising edge must not occur until after parameter 10 (rising edge hold off time). If these conditions are met, the pixel latched by LOAD will be internally synchronized to label SCLK1. If LOAD rises after parameter 11 (setup) during the rising edge hold time, then the pixel data latched by LOAD may split between SCLK1 and SCLK2. Part of the pixels will be synchronized to label SCLK1 and part to SCLK2.

This diagram illustrates waveforms for the 2:1 multiplex mode. These restrictions on LOAD rising edge also occur in 4:1, 8:1, and 32:1 modes.

In 1:1 mode, LOAD clocks the device and there are no restrictions on the LOAD rising edge. PCLK0 and PCLK1 are used only to clock SCLK; if no SCLK is desired, no PCLK is needed.

Figure 11. Waveform for 2:1 MUX Mode with 2x Clock Enabled

Functional Description (continued)

MPU Interface

The ATT21C505/504 supports a standard MPU interface, allowing the MPU direct access to the RAMDAC registers or RAMs (see Table 3). The AD[3:0] inputs select which RAM or register will be accessed. Four 8-bit address registers indirectly address the RAMDAC RAMs. The address registers' bit 0 corresponds to D0 and is the least significant bit.

Writing RAMDAC Color RAMs

The MPU writes the address register (WR1 or WR2, see Table 3) with the address of the RAM location to be modified. To write pixel, cursor, or overscan colors, the MPU completes three continuous write cycles (6 or 8 bits each of red, green, and blue). Following the blue write cycle, the 3 bytes of color information are concatenated into an 18- or 24-bit word and written to the location specified by the address register. The address register advances to the next location which the MPU can modify by simply writing another sequence of red, green, and blue data. A block of color values in successive locations can be written to by writing the start address and performing continuous R, G, and B write cycles until the entire block has been written. To write the cursor pattern RAM, see the Hardware Cursor section.

Reading RAMDAC Color RAMs

The MPU writes the address register (RD1 or RD2, see Table 3) with the address of the RAM location to be read. The contents of the pixel, cursor, or overscan color RAM at the address specified by the address register are copied into an internal RGB register, and the address register advances to the next address. The MPU completes three continuous read cycles (6 or 8 bits each of red, green, and blue). A block of color values in successive locations can be read by writing the start address and performing continuous R, G, and B read cycles until the entire block has been read. To read the cursor pattern RAM, see Hardware Cursor section.

Additional Information

Following a blue read or write cycle (RD1 or WR1) to pixel color RAM or a read or write of the cursor pattern RAM location $FF, the WR1 or RD1 address register resets to $00. WR2 and RD2 are used while accessing the overscan color or cursor color RAM. RD2 and WR2 reset from $FF to $00, but only the two LSBs are used in decoding addresses.

Operation of the MPU interface occurs asynchronously to the pixel clock. Internal logic synchronizes data transfers between the RAMDAC RAMs, and the R, G, and B color subregister. The MPU transfers occur between pixel accesses in CLUT modes. As a result, the $\overline{WR}$ and $\overline{RD}$ signals must maintain a logic high for several clock cycles. See $\overline{RD}$ and $\overline{WR}$ high time in the ac timing characteristics tables in the section on Electrical Characteristics for further information. To eliminate sparkling on the CRT screen during MPU access to the RAMDAC RAMs, internal logic maintains the previous output color data on the analog outputs, while the transfer between look-up table RAMs and the RGB registers occurs.

To monitor the red, green, and blue read/write cycles, the address register has an internal modulo three counter (see Table 23). They are reset to 0 when the MPU writes to an address register and are not reset to 0 when the MPU reads an address register. The MPU can read register bits ST[1:0] to determine the state of the modulo counter.

The MPU can read the address register at any time without modifying its contents or the existing read/write mode. Note that the pixel clock must be active for MPU accesses to the RAMDAC RAM.

Functional Description (continued)

8-/6-Bit Color Resolution

The 8-/6-bit in the control register (CR0[1]) determines whether the MPU port reads and writes 8 bits or 6 bits of color data to the color look-up table RAMs. In the 6-bit mode, color data is on the lower 6 bits of the data bus, with D0 being the LSB and D5, the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be logic 0. Note that in the 6-bit mode, the full-scale output current will be about 1.5% lower than when in the 8-bit mode. This is a result of the two LSBs of each 8-bit DAC always being a logic 0 in the 6-bit mode. In the 8-bit color mode, bit D0 is the color data LSB and bit D7 is the MSB.

Table 23. Modulo Counter Operation

ST[1:0]	Addressed by MPU
00	Red value
01	Green value
10	Blue value

Powerdown

The SLEEP control bit, CR0[0], controls the powerdown. The device operates normally while the sleep bit is a logic 0. A logic 1 in the control register SLEEP bit turns off power to the DACs. The RAM retains data and can be read or written to if the external pixel clock is running. The pixel clock must be 50 MHz or less to ensure that the RAMDAC will wake up and accept updates through the MPU port. The clock to the RAM automatically turns on during MPU read/write cycles and shuts down when the MPU access is completed. During powerdown, all external voltage references are disabled. This prevents current from flowing into or out of the device. The internal reference disable circuitry eliminates the need for external disable logic and allows minimum power dissipation during sleep mode, regardless of the referencing scheme used. It is recommended to keep all inputs at 0 V or 5 V levels to minimize the I/O buffer leakage current.

Monitor Sense

The sense bit, ST[3], is a logic 0 if one or more of the red, green, or blue outputs have exceeded the internal voltage reference level (340 mV). This output is used to determine the presence of a CRT monitor, and, via diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The 340 mV reference has a ±70 mV tolerance. Note that $\overline{\text{SYNC}}$ should be a logic 0 for ST[3] to be stable.

DAC Gain

The device gain from the voltage reference to the DAC output current is shown below. To set the full-scale white current on the DACs while using an internal or external voltage reference, use the formula below.

V_{REF} is the voltage reference in volts, K is the gain constant, and RSET is the resistor connected between the RSET pin and ground. The recommended RSET for RS-343A compatibility applications (doubly terminated 75 Ω) is 147 Ω. The recommended RSET for *PS/2**applications (50 Ω) is 182 Ω.

I_{OUT} (mA) = [V_{REF} (V) * 1,000 * K] / RSET (Ω)

In this case, a voltage reference of 1.235 V, with RSET = 147 Ω and a K factor of 3.17, results in I_{OUT} = 26.63 mA. A 6-bit DAC with no sync or blank results in a K factor of 2.1 and I_{OUT} = 17.64 mA.

Table 24. Gain Factor (K) and I_{OUT} Current

SYNC	BLANK	K (8-Bit)	K (6-Bit)
Yes	Yes	3.195	3.17
Yes	No	3.17	3.0
No	Yes	2.28	2.26
No	No	2.12	2.1

* *PS/2* is a registered trademark of International Business Machines Corporation.

Functional Description (continued)

DAC Output Waveforms

NO $\overline{\text{SYNC}}$		$\overline{\text{SYNC}}$	
mA	V	mA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000

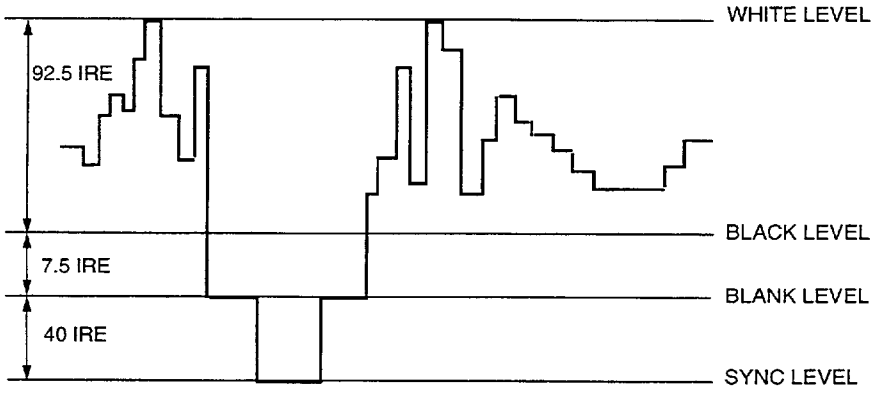


Figure 12. RS-343A Composite Video Output Waveforms

Table 25. RS-343A Video Output Truth Table (Blank Offset Current to Equal 7.5 IRE)

DAC Input Data	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	Output Level	IOUT (mA) $\overline{\text{SYNC}}$ Disabled	IOUT (mA) $\overline{\text{SYNC}}$ Enabled
$FF	1	1	WHITE	19.05	26.67
data	1	1	DATA	data + 1.44	data + 9.05
data	0	1	DATA- $\overline{\text{SYNC}}$	data + 1.44	data + 1.44
$00	1	1	BLACK	1.44	9.05
$00	0	1	BLACK- $\overline{\text{SYNC}}$	1.44	1.44
$XX	1	0	$\overline{\text{BLANK}}$	0	7.62
$XX	0	0	$\overline{\text{SYNC}}$	0	0

Note: 75 Ω doubly terminated load, SETUP = 7.5 IRE. VREF = internal, RSET = 147 Ω.

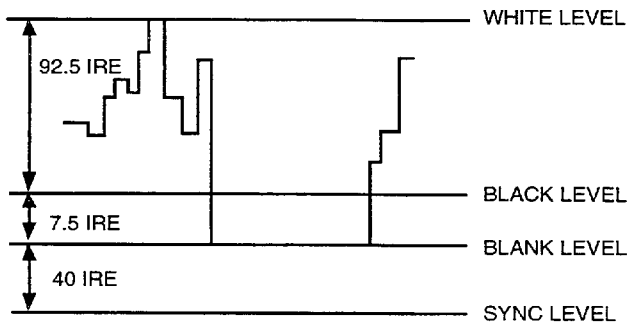


Figure 13. Red and Blue DACs: No Sync

Functional Description (continued)

DAC Output Waveforms (continued)

NO $\overline{\text{SYNC}}$		$\overline{\text{SYNC}}$	
mA	V	mA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000

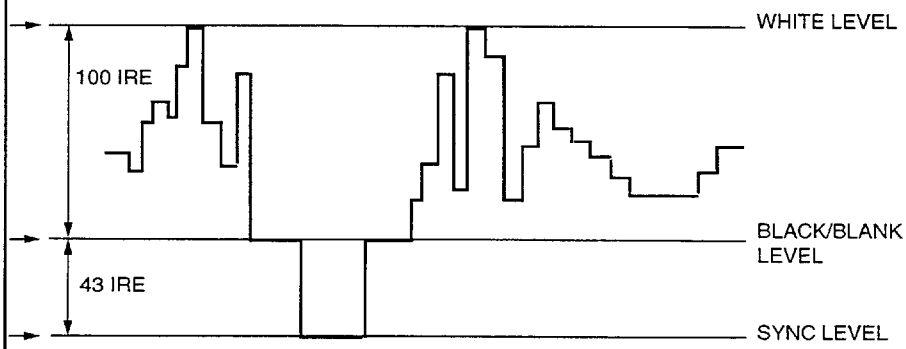


Figure 14. RS-343A Composite Video Output Waveforms

Table 26. RS-343A Video Output Truth Table (No Blank Offset Current)

DAC Input Data	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	Output Level	IOUT (mA) $\overline{\text{SYNC}}$ Disabled	IOUT (mA) $\overline{\text{SYNC}}$ Enabled
$FF	1	1	WHITE	17.62	25.24
data	1	1	DATA	data	data + 7.62
data	0	1	DATA- $\overline{\text{SYNC}}$	data	data
$00	1	1	BLACK	0	7.62
$00	0	1	BLACK- $\overline{\text{SYNC}}$	0	1.44
$XX	1	0	$\overline{\text{BLANK}}$	0	7.62
$XX	0	0	$\overline{\text{SYNC}}$	0	0

Note: 75 Ω doubly terminated load, SETUP = 0 IRE. V_{REF} = internal, RSET = 147 Ω.

Application Information

Board Layout

Careful configuration and placement of supply planes, components, and signal traces ensure a low-noise board. This also helps ensure proper functionality and low signal emissions in restricted frequency bands as mandated by regulatory agencies.

A four-layer PC board with separate power and ground planes will likely result in a board with quieter signals and supplies, as well as less spectral content in emitted frequency bands. Using a solid ground plane, the board should have signal layers 1 and 4 (outside layers) and supply layers 2 and 3 (inside layers).

The ATT21C505/504 should be placed close to the video output connector and between the video output connector and the edge card connector (see Figure 15). This will keep the high-speed DAC output traces short and minimize the amount of circuitry between the RAMDAC and the supply pins on the edge card connector.

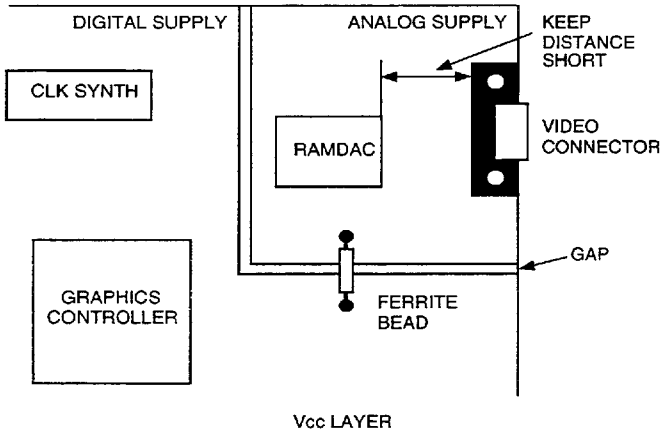


Figure 15. Digital and Analog Supply Plane Split

Power Distribution

Separate the power plane into digital and analog areas as illustrated in Figure 15. Place all digital components over the digital plane and all analog components over the analog plane. The analog components include the RAMDAC, reference circuitry, comparators, mixed-signal chips, and any passive support components for analog circuits.

The analog and digital power plane should be connected with at least one ferrite bead across the separation. This bead provides resistance to high-frequency currents. Select a ferrite bead with an impedance curve suitable for your design. The ferrite should have a resistance at a higher frequency than the maximum signal frequency on the board, but lower than the second harmonic (2x) of that frequency. The following beads provide resistances of approximately 75 Ω at 100 MHz: Ferroxcube VK20019-4B, Fair-Rite 2743001111, or Philips 431202036690.

Decoupling Capacitors

All decoupling capacitors should be located within 0.25 in. of the device to be decoupled. Chip capacitors are recommended, but radial and axial leads will work. Keep lead lengths as short as possible to reduce inductance and EMI. For leaded capacitors, use devices with a self-resonance above the pixel clock frequency.

For the ATT21C505/504, decouple Vcc pin groupings to ground with a 0.1 µF capacitor. For higher-frequency pixel clocks (>110 MHz), use a 0.001 µF capacitor in parallel with the 0.1 µF capacitor to shunt the higher-frequency noise to ground. Power supply noise should be less than 200 mV for a good design. About 10% of any noise below 1 MHz will be coupled onto the DAC outputs. As illustrated in Figure 17, the COMP pin should also be decoupled with a 0.1 µF capacitor. For designs showing ghosting or smearing, add a parallel COMP capacitance of 2.2 µF.

Application Information (continued)

Digital Signals

The digital inputs should not travel over the analog power plane if possible. The RAMDAC should be located over the analog plane close to the digital/analog supply separation. The RAMDAC may also be placed over the supply separation so the digital pixel inputs are over the digital supply plane. The digital inputs, especially the V[7:0] and P[A:D] [7:0] high-speed inputs, should be isolated from the analog outputs. Placing the digital inputs over the digital supply reduces coupling into the analog supply plane. High-speed signals (both analog and digital) should not be routed under the RAMDAC.

Avoid high slew rate edges since they can contribute to undershoot, overshoot, ringing, EMI, and noise feedthrough. Avoiding high slew rate pixel inputs is especially important with the ATT21C505/504 because the RAMDAC has 40 digital pixel inputs. The increased number of pixel inputs increases the noise that may be coupled to the DAC outputs through capacitive coupling into the substrate. Wherever possible, use slower edge rate (3 ns—5 ns) logic such as 74S or 74ALS devices. If this is not possible, edges can be slowed down by using series termination (75 Ω to 150 Ω). Edge noise will result if the digital signal propagates from an impedance mismatch while the signal rises. The reflection noise is particularly troublesome in the TTL threshold region. For a 2 ns edge, the trace length must be less than 4 in.

The clock signal trace should be as short as possible and should not run parallel to any high-speed signals. To ensure a quality clock signal without high-frequency noise components, decouple the supply pins on the clock driver. If necessary, transmission line techniques should be used on the clock by providing controlled-impedance striplines and parallel termination. The 2x clock doubler in the ATT21C505 will help to reduce signal quality problems and EMI radiations by reducing the frequency of the clock signal to the device.

Analog Signals

The load resistor should be as close as possible to the DAC outputs. The resistor should equal the destination termination which is usually a 75 Ω monitor. Unused analog outputs should be connected to ground. The DAC output traces should be as short as possible to minimize any impedance mismatch in the trace or video connector. Series ferrite beads can be added to the analog video signal to reduce high-frequency signals coupled onto the DAC outputs or reflected from the monitor.

To reduce the interaction of the analog video return current with board components, a separate video ground return trace can be added to the ground plane or signal layer. This trace connects directly to the ground of the edge card connector (see Figure 16).

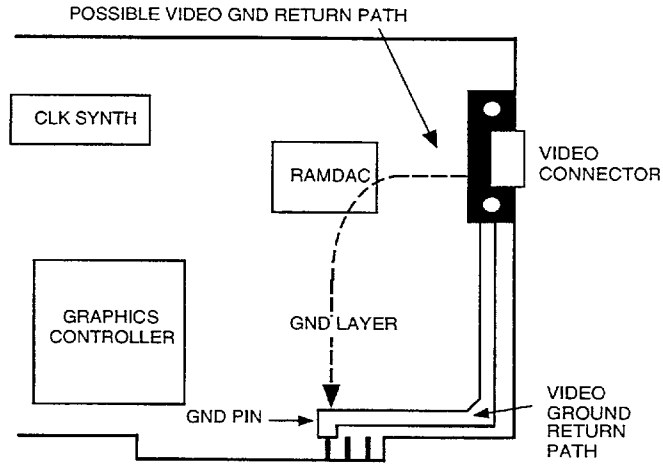


Figure 16. Video Ground Return Current Path

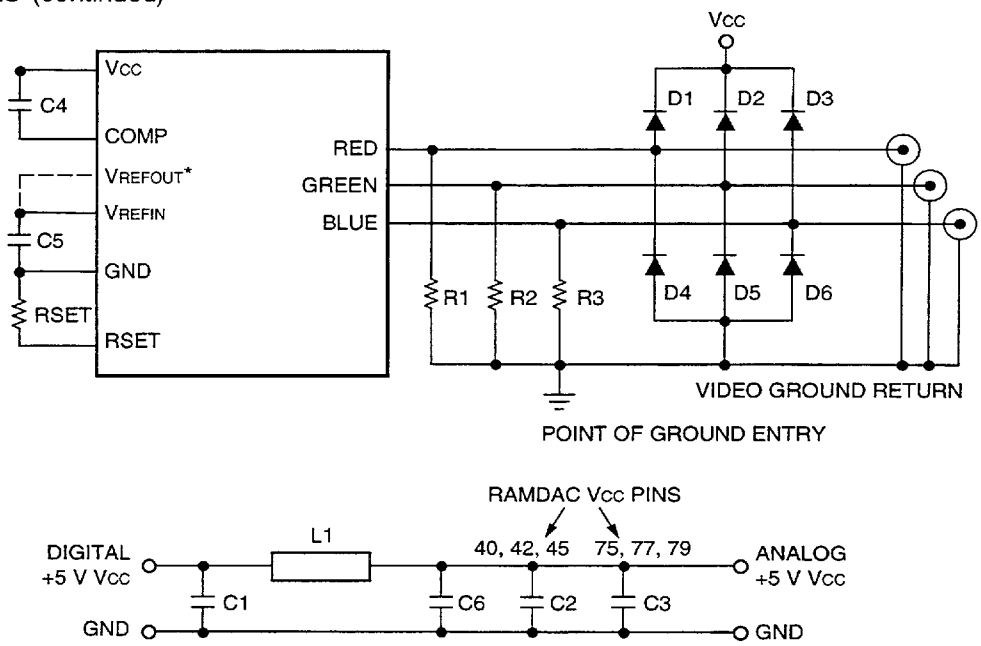
DAC Outputs

The ATT21C505/504 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching ac-coupled monitors.

The diode protection circuit shown in Figure 17 can prevent latch-up under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes.

Application Information (continued)

DAC Outputs (continued)



* Tie either VREFOUT or an external VREF to VREFIN.

Figure 17. Typical Connection Diagram (Use Internal Voltage Reference)

Table 27. External and Internal Voltage Reference Parts List

Location	Description
C1—C5	0.1 µF ceramic capacitor
C6	10 µF capacitor
L1	Ferrite bead
R1—R3	75 Ω, 1% metal film resistor
RSET	147 Ω, 1% metal film resistor
D1—D6	Fast-switching diodes

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} (measured to GND)	—	—	—	7.0	V
Voltage on Any Digital Pin	—	GND – 0.5	—	V_{CC} + 0.5	V
Analog Output Short Circuit: Duration to Any Power supply or Common	ISC	—	Indefinite	—	—
Ambient Operating Temperature	T_A	–55	—	125	°C
Storage Temperature	T_{stg}	–65	—	150	°C
Junction Temperature	T_J	—	—	150	°C
Vapor Phase Soldering (60 s)	TV_{SOL}	—	—	220	°C

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	V_{CC}	4.75	5.00	5.25	V
Ambient Operating Temperature	T_A	0	—	70	°C
Output Load	R_L	—	37.5	—	Ω
Reference Voltage (use internal reference voltage)	V_{REF}	—	Internal	—	V

Electrical Characteristics

Table 28. dc Characteristics 1

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operating condition for generating test signals is RSET = 147 Ω, internal V_{REF}, SETUP = 7.5 IRE. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

Parameter	Symbol	Min	Typ	Max	Unit
Digital Inputs:					
Input Voltage:					
Low	V_{IL}	GND – 0.5	—	0.8	V
High	V_{IH}	2.0	—	Vcc + 0.5	V
Input Current:				—	—
Low (V_{IN} = 0.4 V)	I_{IL}	—	—	–1	µA
High (V_{IN} = 2.4 V)	I_{IH}	—	—	1	µA
Capacitance (f = 1 MHz, V_{IN} = 2.4 V)	Cin	—	—	7	pF
Digital Outputs:					
Output Voltage:					
Low (I_{OL} = 4 mA)	V_{OL}	—	—	0.4	V
High (I_{OH} = –4 mA)	V_{OH}	2.4	—	—	V
SCLK Output:					
Low (I_{OL} = 12 mA)	V_{OL}	—	—	0.4	V
High (I_{OH} = –12 mA)	V_{OH}	2.4	—	—	V
3-State Current	Ioz	—	—	50	µA
Capacitance	C_{DOUT}	—	—	7	pF

Electrical Characteristics (continued)

Table 29. dc Characteristics 2

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operating condition for generating test signals is RSET = 147 Ω, internal V_{REF}, SETUP = 7.5 IRE. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

Parameter	Symbol	Min	Typ	Max	Unit
Resolution (each DAC):	—	8	8	8	bits
Accuracy (each DAC):					
Integral Linearity Error	IL	—	—	±1	LSB
Differential Linearity Error:	DL	—	—	±1	LSB
Gain Error	—	—	±3	±5	%
Monotonicity	—	—	Guaranteed	—	Scale
Coding	—	—	—	—	Binary
Analog Outputs:					
Gray Scale Current Range	Igray	—	—	20	mA
Output Current:					
White Level Relative to Black	Iwb	16.74	17.62	18.5	mA
Black Level Relative to Blank:	Ibb				
With Pedestal	—	0.95	1.44	1.90	mA
Without Pedestal	—	0	5	50	µA
Blank Level	Iblank	6.29	7.62	8.96	mA
Sync Level	Isync	0	5	50	µA
LSB Size	Ilsb	—	69.9	—	µA
DAC to DAC Matching	—	—	2	5	%
Output Compliance	V_{OC}	–0.5	—	1.5	V
Output Impedance	RA_{OUT}	—	10	—	kΩ
Output Capacitance (f = 1 MHz, I_{OUT} = 0 mA)	CA_{OUT}	—	—	30	pF
Internal Reference Output*	V_{REF}	—	1.235	—	V
SENSE Trip Level	V_{SEN}	270	340	410	mV
Power Supply Rejection Ratio:	PSRR	—	—	0.5	%/% ΔV_{CC}
(COMP = 0.1 F, f = 1 kHz)	—	—	—	–6	dB

* The internal voltage reference is trimmed to produce DAC output currents accurate to ±3% typical. See gain error and white level relative to black specs in Table 29 above.

Electrical Characteristics (continued)

Table 30. ac Characteristics — Clocks

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operating condition for generating test signals is RSET = 147 Ω, internal V_{REF}. TTL level input values are 0 V to 3 V, with input rise/fall times ≤3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Analog output load ≤10 pF, $\overline{SENSE}$, D[7:0] output load ≤50 pF. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

Note: 170 MHz ATT21C505/504 operates at speed in 4:1, 8:1, or 32:1 MUX modes only.

		200 MHz Devices		170 MHz Devices		150 MHz Devices		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Internal 2x Clock Rate (reference only)*	fmax	—	200	—	170	—	150	MHz
PCLK0, PCLK1 Rate, 2x Clock Enabled*	f2x	45	100	45	85	45	75	MHz
PCLK0, PCLK1 Rate, 2x Clock Disabled*	fmax	—	110	—	110	—	110	MHz
PCLK0, PCLK1 Cycle Time	1	9.09	—	9.09	—	9.09	—	ns
PCLK0, PCLK1 Pulse Width High or Low	2	4	—	4	—	4	—	ns
PCLK0, PCLK1 Duty Cycle, 2x Clock*	2xdc	40	60	40	60	40	60	%
$\overline{LOAD}$ Rate:	LDmax							
1:1 or VGA		—	110	—	110	—	110	MHz
2:1		—	100	—	85	—	75	MHz
4:1		—	50	—	42.5	—	37.5	MHz
8:1		—	25	—	22	—	18.75	MHz
32:1		—	6.25	—	5.31	—	4.7	MHz
$\overline{LOAD}$ Cycle Time:	3							
1:1 or VGA		9.09	—	9.09	—	9.09	—	ns
2:1		10	—	11.76	—	13.33	—	ns
4:1		20	—	23.5	—	26.7	—	ns
8:1		40	—	47	—	53.3	—	ns
32:1		160	—	188	—	214	—	ns
$\overline{LOAD}$ Pulse Width High or Low Time:	4							
1:1 or VGA		4	—	4	—	4	—	ns
2:1		4	—	4	—	4	—	ns
4:1		4	—	4	—	4	—	ns
8:1		4	—	4	—	4	—	ns
32:1		4	—	4	—	4	—	ns
SCLK Rates:	Smax							
1:1 or VGA		—	110	—	85	—	85	MHz
2:1		—	100	—	85	—	75	MHz
4:1		—	50	—	42.5	—	37.5	MHz
8:1		—	25	—	21	—	18.75	MHz
32:1		—	6.25	—	5.3	—	4.7	MHz
SCLK Cycle Time:	5							
1:1 or VGA		9.09	—	11.11	—	11.11	—	ns
2:1		10	—	11.76	—	13.33	—	ns
4:1		20	—	23.5	—	26.7	—	ns
8:1		40	—	47	—	53.3	—	ns
32:1		160	—	188	—	214	—	ns

* ATT21C505 only.

Electrical Characteristics (continued)

Table 31. ac Characteristics — Clocks (continued)

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operating condition for generating test signals is RSET = 147 Ω, internal V_{REF}. TTL level input values are 0 V to 3 V, with input rise/fall times ≤3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Analog output load ≤10 pF, $\overline{SENSE}$, D[7:0] output load ≤50 pF. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

		135 MHz Devices		110 MHz Devices		85 MHz Devices		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Internal 2x Clock Rate (reference only)*	fmax	—	135	—	110	—	NA	MHz
PCLK0, PCLK1 Rate, 2x Clock Enabled*	f2x	45	67.5	45	55	NA	NA	MHz
PCLK0, PCLK1 Rate, 2x Clock Disabled*	fmax	—	110	—	110	—	85	MHz
PCLK0, PCLK1 Cycle Time	1	9.09	—	9.09	—	11.8	—	ns
PCLK0, PCLK1 Pulse Width High or Low	2	4	—	4	—	5	—	ns
PCLK0, PCLK1 Duty Cycle, 2x Clock*	2xdc	40	60	40	60	NA	NA	%
$\overline{LOAD}$ Rate:	LDmax							
1:1 or VGA		—	110	—	90	—	85	MHz
2:1		—	67.5	—	55	—	42.5	MHz
4:1		—	33.8	—	27.5	—	21	MHz
8:1		—	16.9	—	13.75	—	10.5	MHz
32:1		—	4.23	—	3.44	—	2.7	MHz
$\overline{LOAD}$ Cycle Time:	3							
1:1 or VGA		9.09	—	11.11	—	11.8	—	ns
2:1		14.81	—	18.18	—	23.5	—	ns
4:1		29.58	—	36.36	—	47	—	ns
8:1		59.17	—	72.72	—	94	—	ns
32:1		237	—	291	—	376	—	ns
$\overline{LOAD}$ Pulse Width High or Low Time:	4							
1:1 or VGA		4	—	4	—	4	—	ns
2:1		4	—	4	—	4	—	ns
4:1		4	—	4	—	4	—	ns
8:1		4	—	4	—	4	—	ns
32:1		4	—	4	—	4	—	ns
SCLK Rates:	Smax							
1:1 or VGA		—	85	—	75	—	75	MHz
2:1		—	67.5	—	55	—	42.5	MHz
4:1		—	33.8	—	27.5	—	21	MHz
8:1		—	16.9	—	13.75	—	10.5	MHz
32:1		—	4.23	—	3.44	—	2.7	MHz
SCLK Cycle Time:	5							
1:1 or VGA		11.11	—	11.11	—	11.8	—	ns
2:1		14.81	—	18.18	—	23.5	—	ns
4:1		29.58	—	36.36	—	47	—	ns
8:1		59.17	—	72.72	—	94	—	ns
32:1		237	—	291	—	376	—	ns

* ATT21C505 only.

Electrical Characteristics (continued)

Table 32. ac Characteristics — DAC Performance, Supply Current, and Pipeline Delay

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operating condition for generating test signals is RSET = 147 Ω, internal V_{REF}. TTL level input values are 0 V to 3 V, with input rise/fall times ≤3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Analog output load ≤10 pF, $\overline{SENSE}$, D[7:0] output load ≤50 pF. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

		200, 170 MHz Devices			150, 135, 110, and 85 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DAC Performance:								
Analog Output Delay	23	—	—	30	—	—	30	ns
Analog Output Rise/Fall Time	24	—	2	—	—	3	—	ns
Analog Output Setting Time	—	—	11	—	—	13	—	ns
Clock and Data Feedthrough	—	—	–30	—	—	–30	—	dB
Glitch Energy	—	—	75	—	—	75	—	pV-s
SENSE Output Delay	25	—	1	—	—	1	—	ns
DAC to DAC Crosstalk	—	—	–23	—	—	–23	—	dB
Analog Output Skew	—	—	—	2	—	—	2	ns
Supply Current and Pipeline Delay								
Pipeline Delay*:	Pipe							
1:1 or VGA		8L	—	8L	8L	—	8L	clks
2:1		1L + 7P	—	1L + 8P	1L + 7P	—	1L + 8P	clks
4:1		1L + 7P	—	1L + 10P	1L + 7P	—	1L + 10P	clks
8:1		1L + 7P	—	1L + 14P	1L + 7P	—	1L + 14P	clks
32:1		1L + 7P	—	1L + 38P	1L + 7P	—	1L + 38P	clks
Vcc Supply Current:	Icc							
ATT21C504 operating at:								
110 MHz		—	—	—	—	—	260	mA
85 MHz		—	—	—	—	—	260	mA
ATT21C505 operating at:								mA
200 MHz		—	—	400	—	—	—	mA
170 MHz		—	—	370	—	—	—	mA
150 MHz		—	—	340	—	—	340	mA
135 MHz		—	—	325	—	—	325	mA
110 MHz		—	—	310	—	—	310	
Sleep Current:†	Islp							
ATT21C505/504		—	3	7	—	3	7	mA

* L = LOAD clock, P = pixel clock.
† Measurement conditions for powerdown:
1. PCLK ≤ 25 MHz, device is in sleep mode CR0[0] = 1, CR0[6] = 1, and CR2[7] = 0.
2. SCLK is 3-stated, 2x clock doubler is off CR3[3] = 0.
3. All inputs are at 0 V or 5 V.

Note: The power is measured at maximum pixel activity with 25% retrace. For 170 MHz and 150 MHz devices, the silicon die junction temperature may rise above 125 °C during peak power usage at 70 °C ambient temperature (still air). This is within AT&T's internal reliability limits of a junction temperature of up to 150 °C.

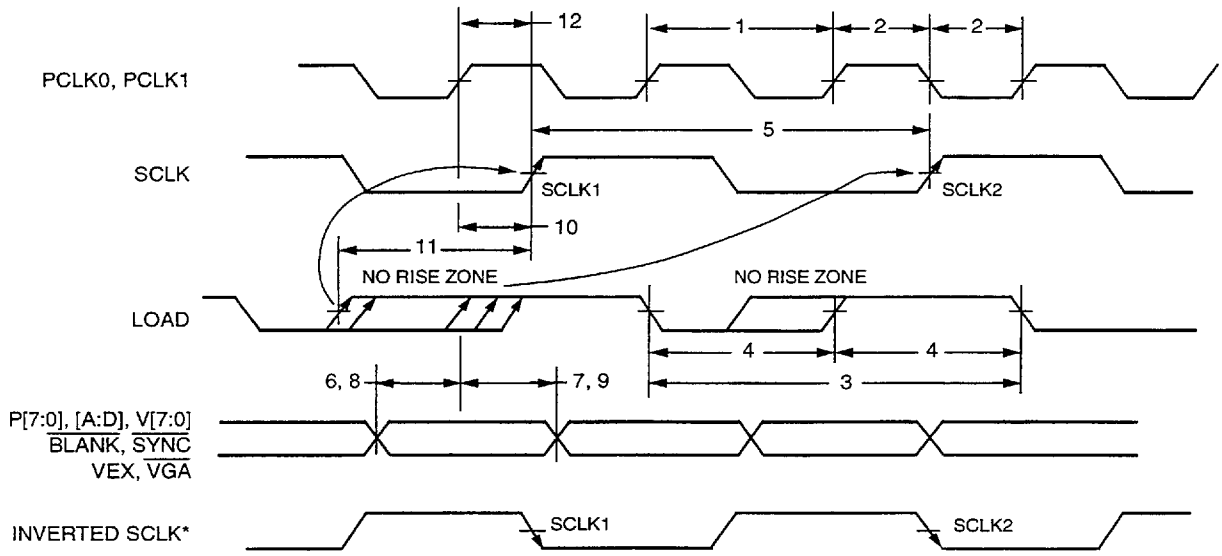
Electrical Characteristics (continued)

Table 33. ac Characteristics — Pixel Timing and MPU Port

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operating condition for generating test signals is RSET = 147 Ω, internal V_{REF}. TTL level input values are 0 V to 3 V, with input rise/fall times ≤3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Analog output load ≤10 pF, $\overline{SENSE}$, D[7:0] output load ≤50 pF. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

		200, 170, 150, 135 MHz Devices			110, 85 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Pixel Timing:								
P[A:D], [7:0] Setup to LOAD	6	2	—	—	2	—	—	ns
P[A:D], [7:0] Hold from LOAD	7	4	—	—	4	—	—	ns
V[7:0], VEX, $\overline{BLANK}$, $\overline{SYNC}$, $\overline{VGA}$, Setup to LOAD	8	3	—	—	3	—	—	ns
V[7:0], VEX, $\overline{BLANK}$, $\overline{SYNC}$, $\overline{VGA}$, Hold from LOAD	9	3	—	—	3	—	—	ns
LOAD Rising Edge Hold from SCLK Rising Edge	10	—	—	–3	—	—	–3	ns
LOAD Rising Edge Setup to SCLK Rising Edge	11	—	—	10	—	—	14	ns
SCLK Output Delay (1:1 mode)	12	—	6	11	—	6	11	ns
SCLK Output Delay (non 1:1 mode)	12	—	10	20	—	10	20	ns
$\overline{FIELD}$, Setup and Hold from LOAD	—	3	—	—	3	—	—	ns
Microprocessor Port:								
AD[3:0] Setup Time	13	10	—	—	10	—	—	ns
AD[3:0] Hold Time	14	10	—	—	10	—	—	ns
$\overline{RD}$ Asserted to D[7:0] Driven	15	5	—	—	5	—	—	ns
$\overline{RD}$ Asserted to D[7:0] Valid	16	—	—	40	—	—	40	ns
$\overline{RD}$ Negated to D[7:0] 3-Stated	17	—	—	20	—	—	20	ns
Read D[7:0] Hold Time	18	5	—	—	5	—	—	ns
Write D[7:0] Setup Time	19	10	—	—	10	—	—	ns
Write D[7:0] Hold Time	20	10	—	—	10	—	—	ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	21	50	—	—	50	—	—	ns
$\overline{RD}$, $\overline{WR}$ Pulse Width High	22	6	—	—	6	—	—	pclk

Timing Characteristics



* SCLK can be inverted by setting CR3[5] = 1. In this case, all references to the rising edge of SCLK are made to the falling edge of the inverted SCLK.

Notes:
LOAD rising edge must occur before parameter 11 in the figure above. The next LOAD rising edge must not occur until after parameter 10 (rising edge hold off time). If these conditions are met, the pixel latched by LOAD will be internally synchronized to label SCLK1. If LOAD rises after parameter 11 (setup) during the rising edge hold time, then the pixel data latched by LOAD may split between SCLK1 and SCLK2. Part of the pixels will be synchronized to label SCLK1 and part to SCLK2.

This diagram illustrates waveforms for the 2:1 multiplex mode. These restrictions on LOAD rising edge also occur in 4:1, 8:1, and 32:1 modes.

In 1:1 mode, LOAD clocks the device and there are no restrictions on the LOAD rising edge. PCLK0 and PCLK1 are used only to clock SCLK; if no SCLK is desired, no PCLK is needed.

Figure 18. Video Input Timing

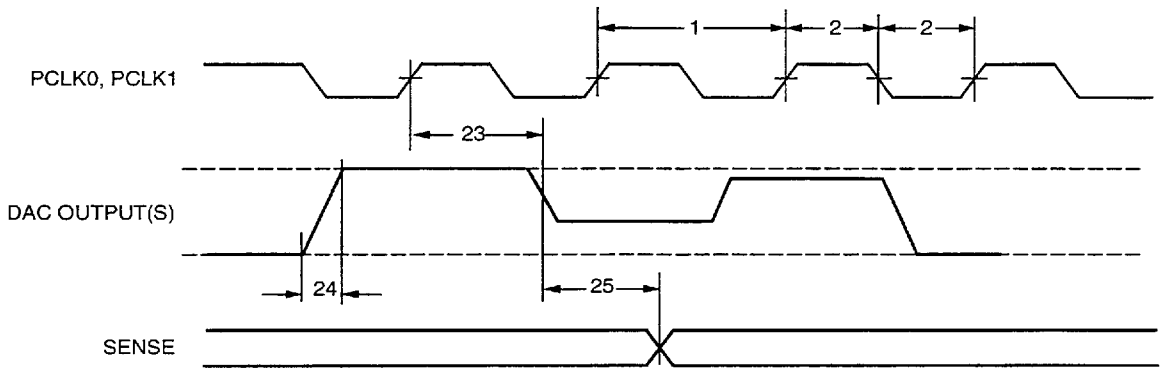


Figure 19. Video Output Timing

Timing Characteristics (continued)

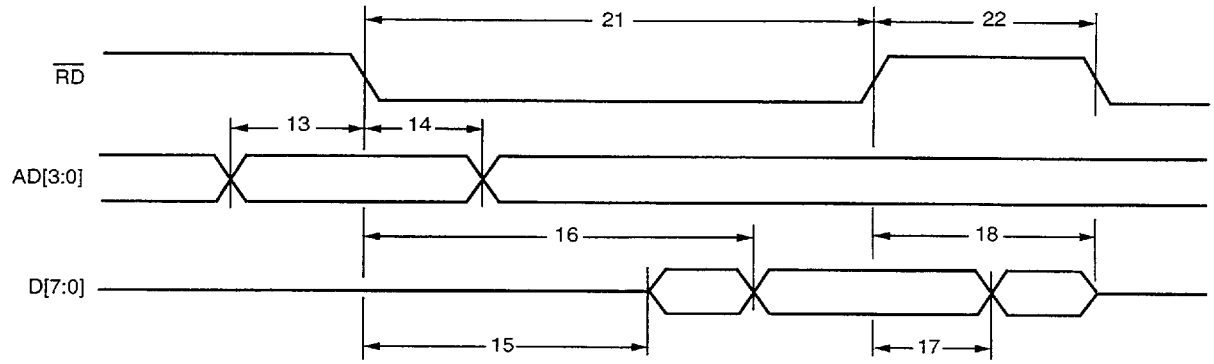


Figure 20. Read-Cycle Timing Diagram

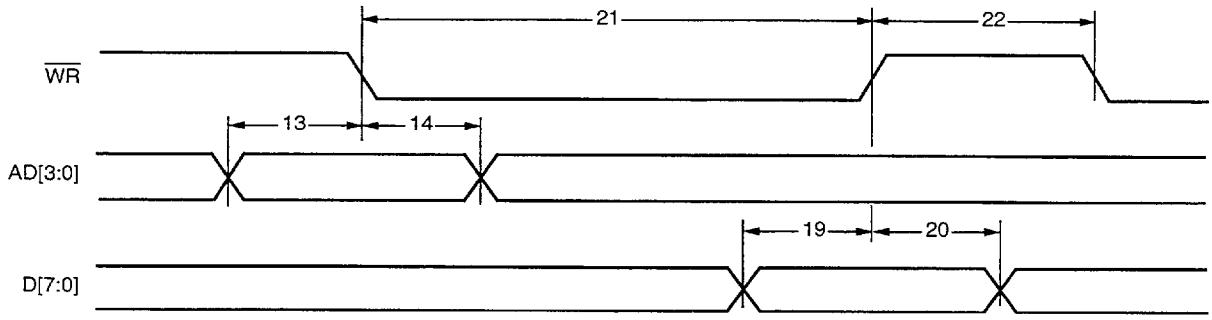
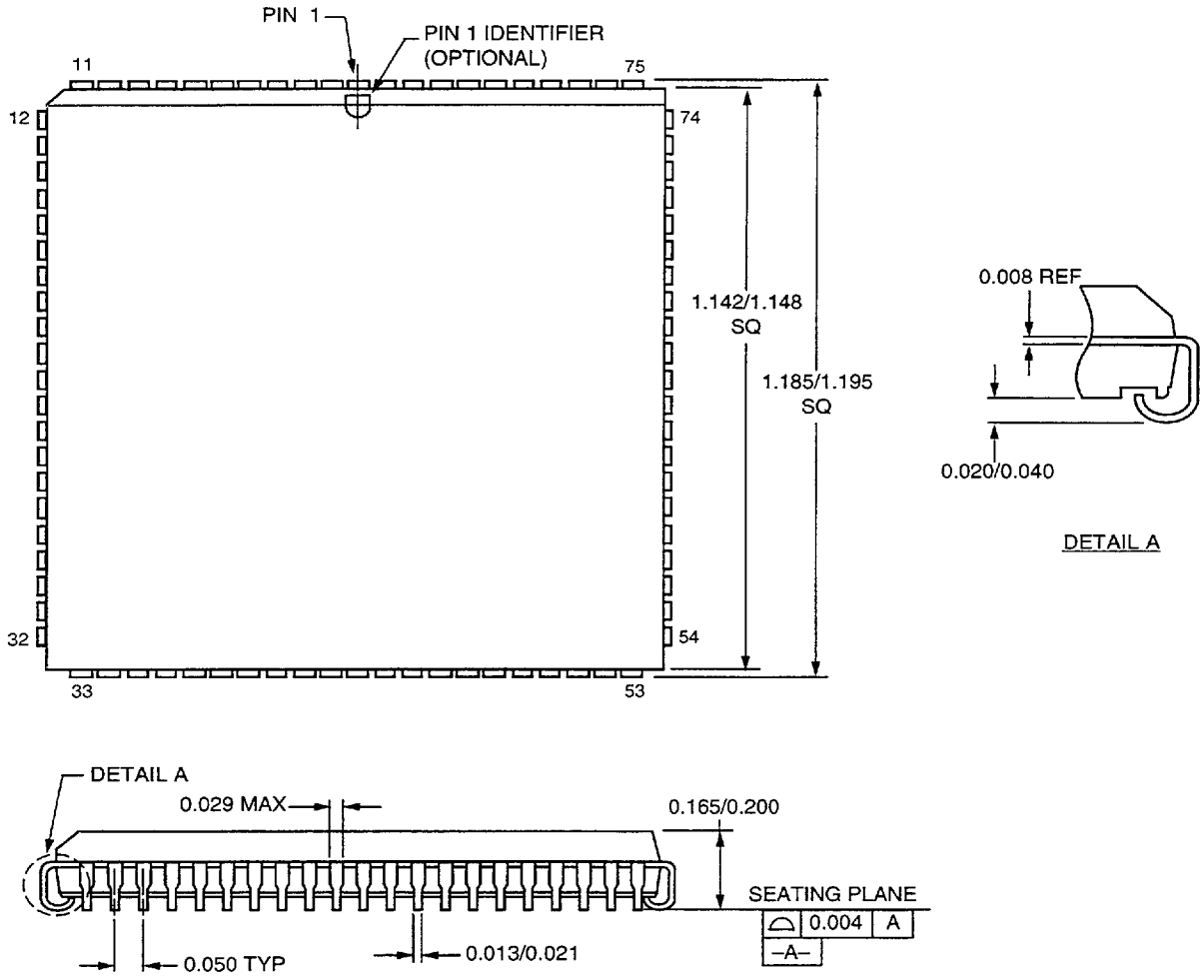


Figure 21. Write-Cycle Timing Diagram

Outline Diagram

84-Pin PLCC Package

Dmensions are in inches.



Ordering Information

Device	Speed	Temperature	Package Type
ATT21C505-20M84	200 MHz	0 °C—70 °C	84-Pin PLCC
ATT21C505-17M84	170 MHz	0 °C—70 °C	84-Pin PLCC
ATT21C505-15M84	150 MHz	0 °C—70 °C	84-Pin PLCC
ATT21C505-13M84	135 MHz	0 °C—70 °C	84-Pin PLCC
ATT21C505-11M84	110 MHz	0 °C—70 °C	84-Pin PLCC
ATT21C504-11M84	110 MHz	0 °C—70 °C	84-Pin PLCC
ATT21C504-85M84	85 MHz	0 °C—70 °C	84-Pin PLCC