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Advanced Information

Am95C82

Disk Data Separator (DDS)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Complete single-chip Disk Data Separator for floppy disk and hard disk drives (minimal external components)**
- **Complete on-chip Phase-Locked Loop (PLL), frequency may be dynamically changed**
- **Supports:**
  - — 1 to 10 Mbit/s NRZ data rate with MFM coding for hard disks and high-density floppy drives
  - — 1 to 10 Mbit/s NRZ data rate with 2,7 RLL coding for hard disk
  - — 250K to 1000 Kbit/s NRZ data rate with MFM coding for double-density floppy disks
  - — 1.5 to 2.5 Mbit/s NRZ data rate with MFM coding for high-density disk
- **On-Chip Write Precompensation (frequency proportional) (MFM)**
- **On-Chip Address Mark Generator/Detector**
- **One Am95C82 can support both floppy and hard disk drives. The on-chip analog section can dynamically be switched between those modes. No external components need to be switched.**
  - — 5 V Vcc, CMOS technology
  - — 28 Pin Dip or PLCC

GENERAL DESCRIPTION

The Am95C82 Disk Data Separator is a single-chip solution to several functions associated with reading and writing data to floppy or hard disk drive systems. The Am95C82 is divided into two basic sections: the Read section and the Write section.

The Read section contains an on-chip Phase-Locked Loop (PLL) to provide a read clock signal that tracks the serial data from the disk. The MFM or 2,7 RLL data is then fed into the MFM/2,7 RLL decoder to be converted into NRZ (Non Return to Zero) data. A built-in address mark detector recognizes the standard address marks for MFM floppy and hard disks, and a sync, preamble, and address mark sequence for 2,7 RLL disks.

The Write section contains two encoders that encode the incoming NRZ data and the Write clock into a single stream of either 2,7 RLL- or MFM-encoded data. The Write section also contains an address mark generator and the Write precompensation logic. This address mark generator can generate the standard address marks for MFM floppy and hard disk data formats, and the appropriate preamble and address mark of 2,7 RLL. Write precompensation (MFM) compensates the bit-shifting caused by the characteristics (pulse superpositioning) of the magnetic media.

The Am95C82 is the companion device for the Am9580A/Hard Disk Controller or the Am9590 ESDI Hard Disk Controller. These chip sets provide a complete disk controller solution to interface ST506- or ST412-type hard disk drives and floppy disk drives. The small size and low external component of the Am95C82 permit easy integration onto disk drives offering an NRZ data interface (e.g., ESDI or SMD).

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BLOCK DIAGRAM

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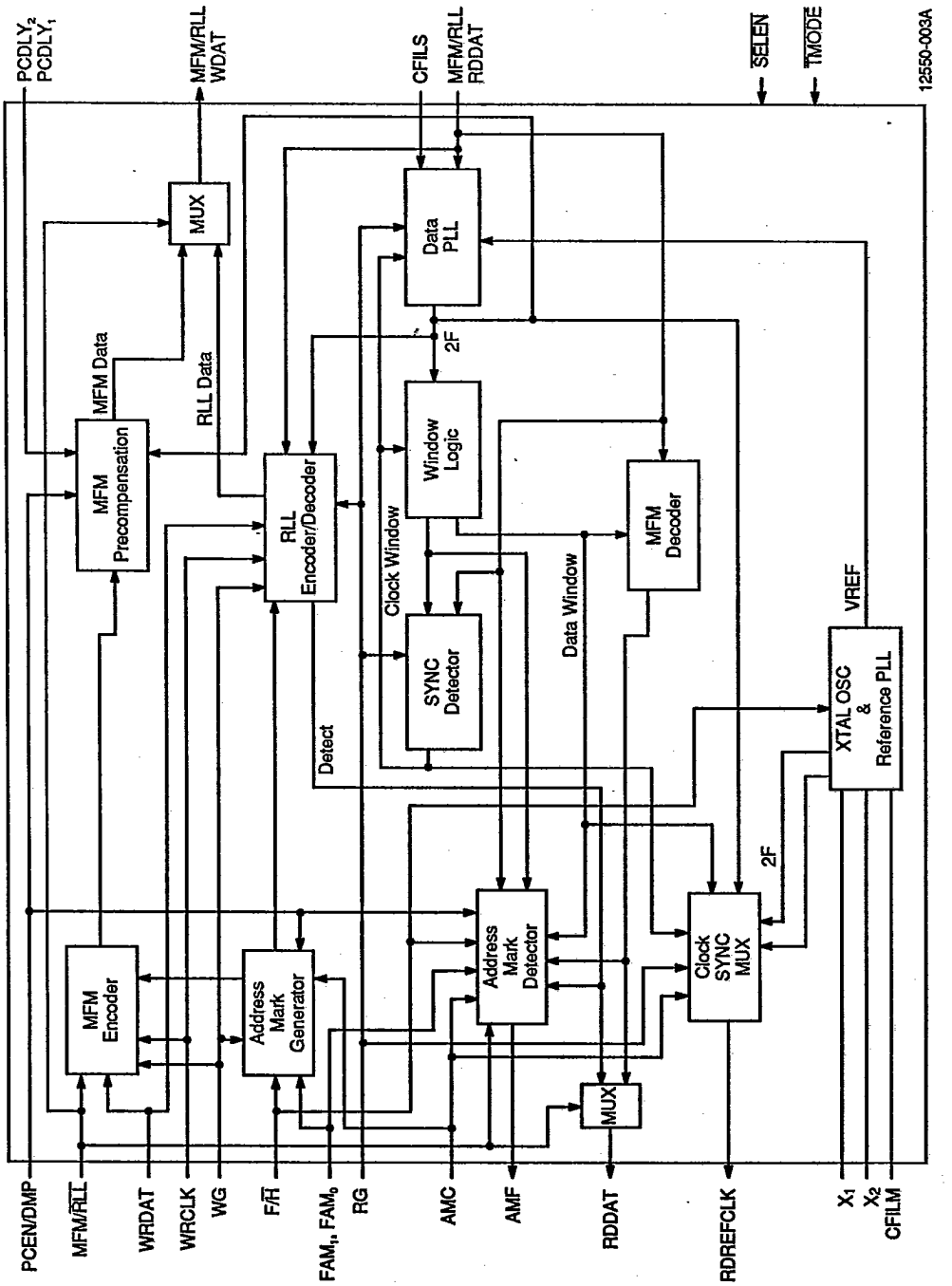

CONNECTION DIAGRAMS

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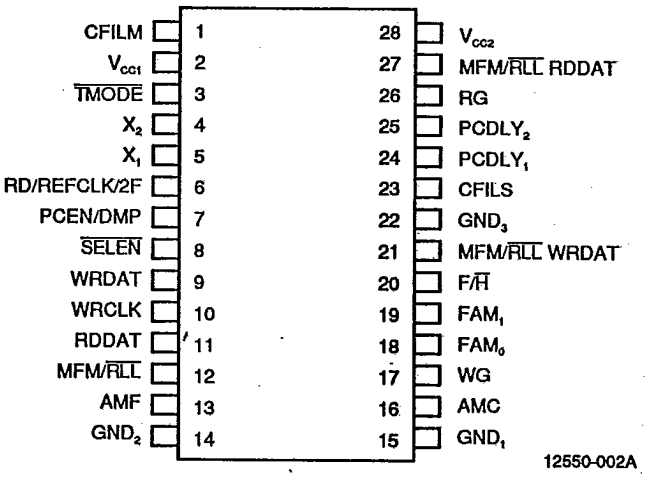
PDIP



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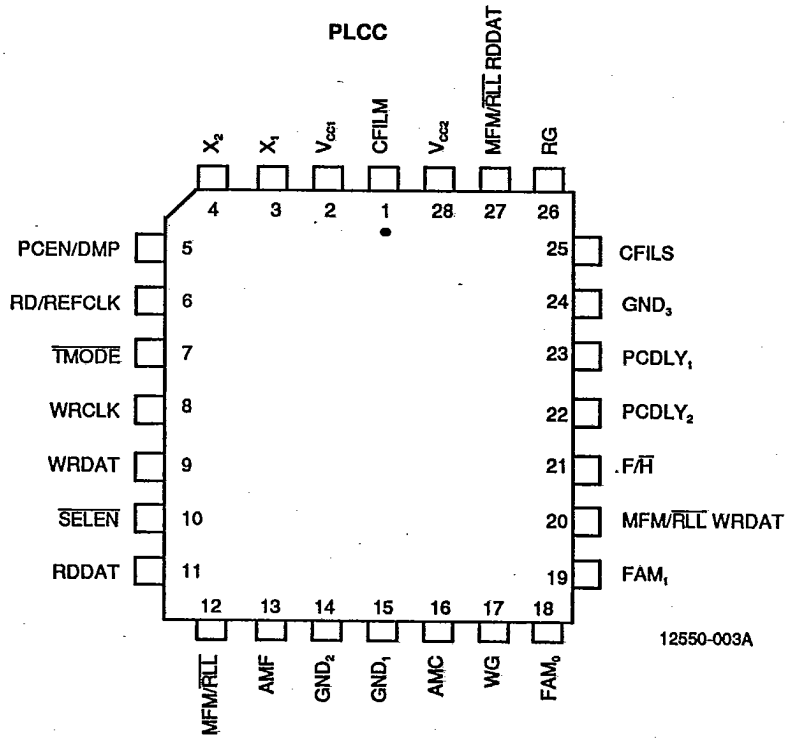
PLCC



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LOGIC DIAGRAM

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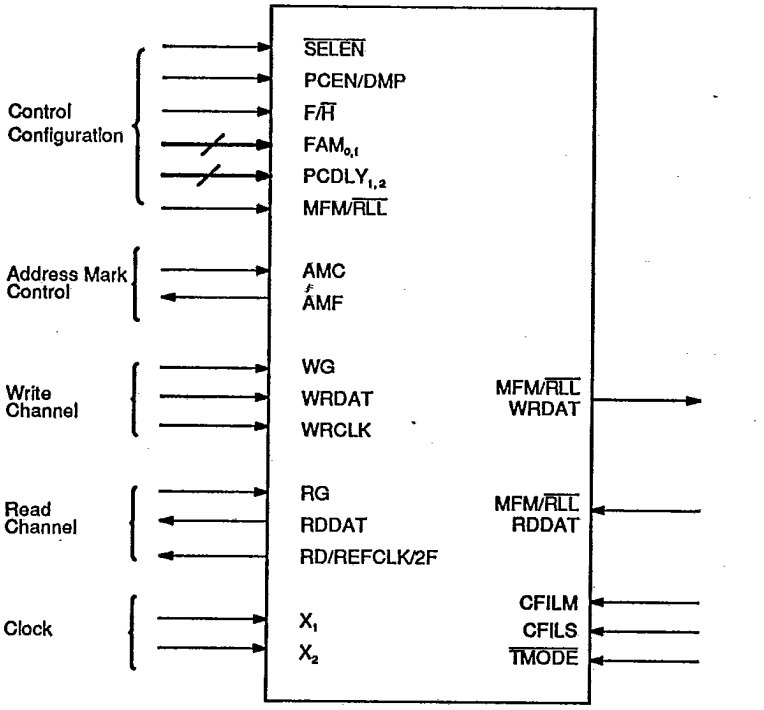

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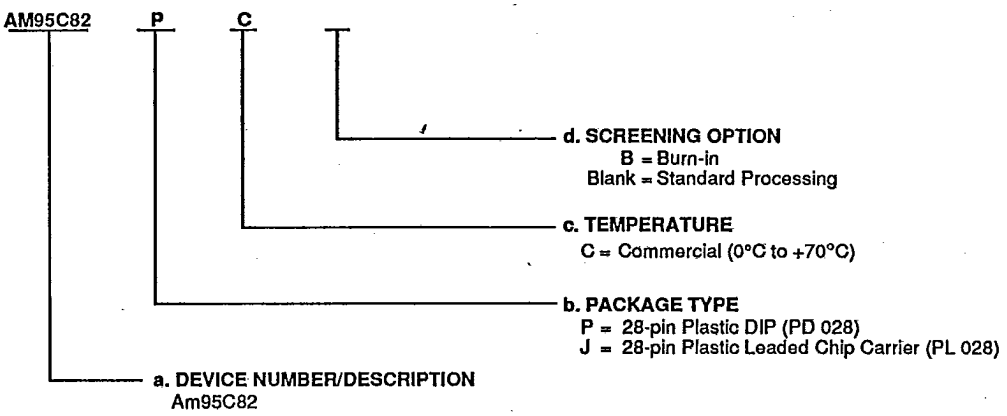
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Package Type
c. Temperature Range
d. Screening Option (if desired)



Valid Combinations	
AM95C82	JC, PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

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AMC

Address Mark Control (Input, Active High)

This pin has three functions: generate and write an address mark during a Write operation, enable detection of an address mark during a Read operation, and latch (on the Low-to-High transition) the state of the FAM_1, FAM_0 pins at the beginning of a Read operation.

AMF

Address Mark Found (Output, Three-State, Active High)

During a Write operation, AMF acknowledges that the address mark has been completely generated. The Am95C82 latches in the data bit following the address mark with the first clock after AMF has been asserted. During a Read operation, AMF acknowledges that an address mark of the requested type has been found. The Am95C82 synchronously strobes out AMF and the first data bit following the address mark.

CFILM

Filter Capacitor (Input, Analog)

This pin is for a .033-µf capacitor for the master PLL.

CFILS

Filter Network (Input, Analog)

This pin is for a user-defined passive filter network used to define the characteristics of (slave) data PLL.

FAM_1, FAM_0

Floppy Address Mark Select (Inputs)

These inputs select the address mark to be processed and set up clock dump and data dump modes for MFM data. These inputs are further qualified by the MFM/$\overline{RLL}$, F/$\overline{H}$, and PCEN/DMP pins (see Table 2).

F/$\overline{H}$

Floppy/Hard Disk (Input)

This pin has two functions. It selects the prescaler value for X_1, X_2 inputs to determine the relationship between the crystal frequency and data rate. When High, the prescale value is 16 for MFM floppy operation (250–1000 kbit/s). When Low, the prescale value is unity for MFM and RLL hard disk operation (1–10 Mbit/s).

When qualified by FAM_1, FAM_0, and MFM/$\overline{RLL}$, this pin selects the type of address mark to be generated or detected (see Table 2).

MFM/$\overline{RLL}$

Code Selection (Input)

Selects RLL or MFM modes of operation. Selects RLL (2,7) coding when Low, MFM coding when High (see Table 2). This pin has an internal pull-up to default to MFM mode if not connected.

$PCDLY_2$, $PCDLY_1$

Precompensation Delay (Inputs, Analog)

The ratio of the resistors connected between $PCDLY_1$ and V_{CC3} (R_1) and $PCDLY_2$ and V_{CC3} (R_2) sets the precompensation delay as a fraction of the reference clock cycle time. The range of the precompensation delay can be set from 1% to 20% of the bit cell time with an accuracy of ±5% of the chosen value or 1 ns, whichever is greater (using 1% resistors). The minimum precompensation delay can be set to 2 ns.

These inputs must not be left open. Open inputs disturb the operation of the on-chip PLL and thereby affect both the Read and the Write logic. If precompensation is not enabled, these inputs may be directly connected to V_{CC}. Figure 6 gives the typical values.

PCEN/DMP

Precompensation Enable/Dump Data (Input)

This input implements two functions that are multiplexed. For Read operations the Am95C82 latches the level on this pin with the falling edge of $\overline{SELEN}$. A High selects dump mode; a Low selects normal Read mode. In dump mode the first non-0 bit received after a sync field (eight consecutive 0s) will be interpreted as the address mark, AMF will be asserted, and data will then be output. This mode is useful for attempting to recover data from sectors with corrupted address marks. Dump mode applies to MFM data only.

For MFM Write operations, this input enables/disables the Write precompensation logic. When Low, PCEN disables Write precompensation, permitting Write data to flow with no alteration in timing. When High, PCEN enables Write precompensation, altering the pulse-to-pulse timing of Write data to minimize the effects of pulse superposition on the magnetic media. The degree of compensation is adjusted by the PCDLY inputs. Write precompensation is not used in RLL mode.

RD/REFCLK/2F

Read/Reference Clock/2* Data Frequency (Output, Three-State)

During a Read operation (RG active), RD/REFCLK is the Read clock that is derived from the encoded disk data signal on MFM/RLL RDDAT. The disk controller should use this clock to sample the Read data (RDDAT). When the system is not performing a Read operation (RG inactive), RD/REFCLK is the reference clock that is derived from reference frequency supplied from X_1 and X_2. The switching from RDCLK to REFCLK is a glitch-free operation. This output is three-stated when $\overline{SELEN}$ is High (inactive).

When the Am95C82 is selected to operate in the synchronizer-only mode, the recovered clock signal is output on the RD/REFCLK pin. The recovered clock is two times the data frequency.

$\overline{SELEN}$

Select Enable (Input, Active Low)

Used to enable three-state outputs (AMF, RD/REFCLK, RDDAT MFM/$\overline{RLL}$ WRDAT). Also used to strobe in the state of PCEN/DMP (falling edge of $\overline{SELEN}$) to deter-

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mine normal or dump data modes. If dump data mode is not used, $\overline{SELEN}$ may be permanently tied Low.

If the Am95C82 only controls hard disk drives (F/$\overline{H}$ tied Low), $\overline{SELEN}$ may be tied Low permanently.

$\overline{TMODE}$
Testmode (Input, Active Low)

This input is used to test the Am95C82 logic independent of the internal PLL. This input should be tied High for normal operation. It is used for test purposes only.

X_1, X_2
Crystal Oscillator 1,2 (Inputs)

An external crystal is connected to these two inputs (see Figure 2). Alternatively, a TTL-compatible clock may be connected to X_1 with X_2 not connected. Table 2 specifies the crystal frequency for various operating modes. In floppy mode, the crystal frequency is divided down internally by 16, allowing the crystal oscillator to operate between 4 and 16 MHz for floppy MFM data rates of 250 kbit/s to 1000 kbit/s.

Write Section

MFM/$\overline{RLL}$ WRDAT
MFM/$\overline{RLL}$ Write Data (Output, Three-State)

MFM/$\overline{RLL}$ Write Data is the encoded data output to the disk drive. The MFM format is used for hard disks and double-density floppy disks. The RLL format is used for hard disks. This output is three-stated when $\overline{SELEN}$ is High (inactive).

WG
Write Gate (Input, Active High)

When Write Gate is High the Write logic is enabled. This input should be connected to the Write gate output of the disk controller. WG and RG must not be active simultaneously.

WRCLK
Write Clock (Input)

In applications where the data separator and disk controller are physically close, this clock input is typically connected to the RD/REFCLK output of the Am95C82. WRDAT must satisfy the setup and hold-time requirements with respect to WRCLK. In applications where the data separator and the disk controller are physically separated (for example, ESDI), this input should be connected to the Write clock output of the disk controller (for example, the Write clock of the ESDI interface). This connection minimizes the skew between clock and data.

WRDAT
Write Data (Input, Active High)

This input receives the NRZ Write Data from the disk controller. The Am95C82 samples this input with WRCLK (Write clock).

Read Section

MFM/$\overline{RLL}$ RDDAT
MFM/$\overline{RLL}$ Read Data (Input, Active High)

This input provides the encoded data read from the disk. The Am95C82 internally separates clock and data information of the encoded MFM/$\overline{RLL}$ RDDAT and restores it to the original NRZ format (RDDAT), which is sent to the disk controller.

RDDAT
Read Data (Output, Three-State, Active High)

This output provides the decoded NRZ data for the hard disk controller. In RLL sync mode the data is not decoded; the Am95C82 directly passes the MFM/RLL RDDAT to the RDDAT output. No internal processing takes place. This output is three-state when $\overline{SELEN}$ is High.

RG
Read Gate (Input, Active High)

When RG is High, the Read section of the Am95C82 is enabled, allowing the internal PLL to lock up to the incoming encoded data stream. Read operations proceed as follows.

AMC is asserted, latching in the state of the FAM_1, FAM_0 pins and selecting the appropriate address mark to search for. RG is then asserted, switching the input of the data tracking loop from the reference loop (training mode) to the MFM/$\overline{RLL}$ RDDAT pin. The loop acquires lock and constantly searches for a sync field and address mark. AMF is asserted when the address mark is found (the address mark pattern precedes the AMF signal), and NRZ data is output starting coincident with the AMF. Receipt of the AMF by the Am9580A/90 will cause AMC to be deactivated, thereby deasserting AMF; however, NRZ data continues to be output as long as RG is asserted. At the end of the sector, RG must be deasserted in order to reset the sync field and address mark detection circuitry for the next sector.

V_{CC1}
Output power supply (+5 V)

V_{CC2}
Analog power supply (+5 V)

GND_1
Logic ground potential (0 V)

GND_2
Output ground potential (0 V)

GND_3
Analog ground potential (0 V)

FUNCTIONAL DESCRIPTION

The Am95C82 is a highly integrated single-chip data separator for both floppy and hard disk drives that use MFM codes and for hard disks that use 2,7 RLL code. Data separation is the regeneration of a reference clock from an incoming bit stream (Read data) and the use of that clock to separate out serial NRZ data. The coding rules for MFM use a unit of time called a bit cell. The coding rules for 2,7 RLL are shown in Table 1 and Figure 1.

MFM Coding

In the FM encoding scheme a bit cell accommodates up to two flux transitions: a first flux transition of the mandatory clock and an optional second flux transition if the NRZ data is 1. However, all clock flux transitions are redundant.

MFM (Modified Frequency Modulation) uses the flux transitions more efficiently. Here, each bit cell accommodates at most one flux transition. Hence, MFM recording doubles the data capacity over FM recording without increasing the flux transition density.

The rules for MFM encoding are as follows:

- Generate a pulse in the middle of the bit cell (data pulse), if a 1 is to be stored.
- Generate a pulse in the beginning of the bit cell (clock pulse), if a 0 is to be stored and the preceding bit cell also stores a 0.
- If the current bit cell stores a 0 and the preceding bit cell stores a 1, the current bit cell does not accommodate any pulses.

Because the MFM encoding only generates one flux transition per bit cell, the bit cell can be reduced to one-half of the FM bit cell, keeping the flux transition density constant. This doubles the data capacity of the disk compared to FM encoding.

The data separator regenerates a data window that covers the position of the data pulse. For a constant flux transition rate, the MFM data window is half the size of the FM data window. This means that MFM recording demands more sophisticated data separators than FM recording.

2,7 RLL Coding

The RLL encoding scheme is a more general method to encode data. Basically, RLL just defines the minimum and the maximum number of 0s between two 1s in the

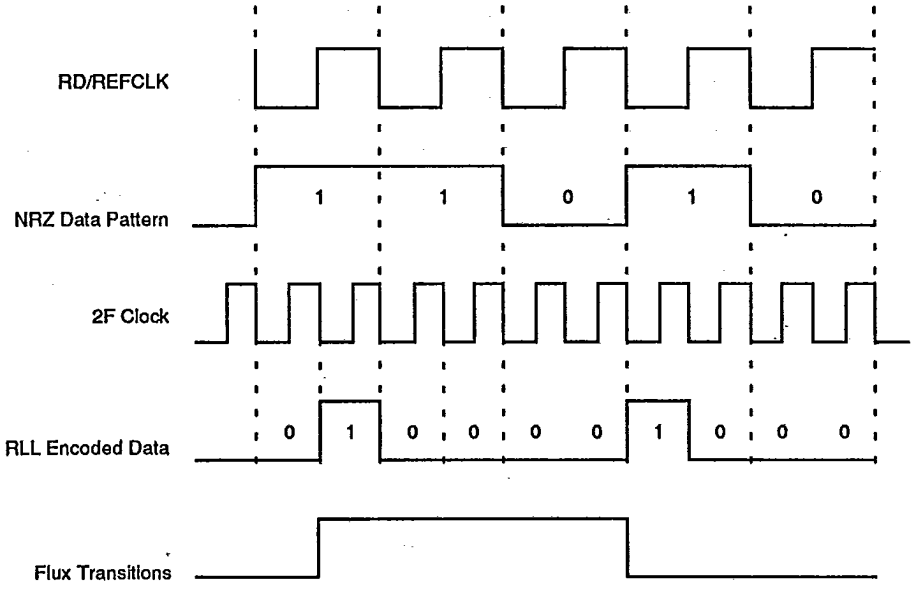

Figure 1. RLL Encoding

output data stream. Again, the output is running at twice the input speed. There are several different RLL codes in use today. They differ in their maximum and minimum numbers and in the actual bit pattern used to encode a certain input pattern.

There are certain technical and physical limitations to the values in use for these codes. The maximum number of 0s is limited by the quality of the PLL synchronizing onto the data stream while reading. The minimum number of 0s, on the other hand, is limited by the possible bit density on the magnetic media. The goal is to use a given bit density and increase the number of possible 0s as much as possible. By this definition of RLL the older MFM coding scheme is just a special case of RLL.

The most common RLL code used today is the so-called 2,7 Code. These numbers indicate that the minimum number of 0s between two 1s is two and the maximum number is seven. Table 1 shows the possible patterns on both sides of the encoder. The Am95C82 implements this RLL 2,7 Code.

PLL Operation

The on-chip PLL regenerates the Read clock from the encoded data read from the disk. It operates by comparing the input data with a reference signal generated by a Voltage Controlled Oscillator, or VCO. If the input transitions and the VCO transitions match, then the loop is said to be in lock. If these sets of transitions do not match (coincide in time), then a correction signal is generated by the phase detector and sent to the VCO to modify its output. Standard phase detectors expect a one-to-one correspondence between input transitions and VCO transitions. A disk data stream, however, contains missing pulses. If this bit stream is directly applied to the phase detector, it gives an erroneous output. For example, a repeated "...1010..." pattern would cause a standard PLL to lock to half the frequency because only half the number of transitions exist versus the "...0000..." bit stream.

Two approaches can correct this PLL behavior. First, the phase detector performs a phase comparison only if a data pulse is present, that is, within one-half bit cell time of a VCO edge. Generally, this arming function involves two data paths to the phase detector: a "prompt" path and a "delayed" path. The "prompt" path enables the phase detector for a phase comparison, which is then done using the "delayed" path. The drawbacks of this scheme are that the delay must be proportional to the data rate and that it requires external components such as delay lines or one-shots.

Table 1. FRANASZEK Coding Rules

NRZ	RLL
10	1000
11	0100
000	100100
010	001000
011	000100
0010	00001000
0011	00100100

The second technique employed by the Am95C82, however, integrates a proprietary PLL that is not sensitive to missing pulses and requires only a minimum number of nonadjustable external components. The next section describes the unique approach that is implemented on the Am95C82.

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Master and Slave PLL

The Am95C82 contains two PLLs: a Master PLL (or reference PLL) and a Slave PLL (or data PLL). The Master PLL is set to the nominal expected data frequency (as specified by the crystal), and serves to keep the slave PLL close to that frequency in the absence of any clock or data pulses. It generates a reference current that is proportional to the expected data frequency.

The slave PLL tracks the incoming data bit stream and produces a reference clock that times the actual data separation process. It has two phase detectors/filters: a "fast" detector/filter that acquires and tracks the input signal, and a "slow" detector/filter that eliminates any steady-state phase errors between the generated reference clock and the incoming bit stream. The input to the slave VCO is the weighted sum of the output of these two phase detectors/filters and the reference current from the master PLL.

The phase detectors/filters are time-to-voltage converters (integrators), which are ramped up for half the VCO time and ramped down for the other half. The "fast" phase detector consists of a matched pair of integrators that, in lock or in the absence of data, are ramped up and down in a synchronous manner. When the loop is not in lock, the arrival of a data transition will cause one integrator to "freeze" immediately, while the other integrator continues its cycle. The output of the "fast" phase detector is the difference between the outputs of the two integrators. So, the phase detector is immune to missing data transitions; in the absence of data the two integrators will merely cycle with a constant net difference of zero.

Compared to implementations that use only one integrator, this approach yields a phase detector that is faster and free of ripple. This "fast" phase detector requires well-matched, low-drift integrators for proper operation (static and dynamic matching and drift cancellation). This phase detector is called "fast" because it tracks the instantaneous changes in phase and has negligible low frequency response.

The "slow" phase detector remembers and overcomes static phase errors that the "fast" integrators do not detect.

External Components

A single, noncritical filter capacitor used in the Master PLL is required on the CFILM pin. The only absolute quantity in the circuit is the reference frequency, which is set by the crystal connected to X_1 and X_2.

The Am95C82 requires an external loop filter for the data PLL. The minimum configuration of a resistor and a capacitor is shown in Figure 3. The optimum configuration adds a second capacitor to the minimum configuration. The two-capacitor configuration is necessary in applications where the reference input frequency will be changed on the fly, requiring optimized transient response and bandwidth for the slave loop.

Mixed Control of Floppy and Hard Disk Drives

Because all read PLL parameters are adjusted automatically, one Am95C82 can provide the control for both floppy and hard disk drives. No external components need to be switched assuming that the relative precompensation value for floppy and hard disk modes is identical (for example, 1% to 20% of bit cell time). In this mixed mode it is suggested not to use the on-chip crystal oscillator. Instead, a switchable (for example, 4 MHz for 250 kbit/s MFM floppy data rate and 5 MHz for 5 Mbit/s MFM hard disk data rate) TTL clock source should be connected to X_1.

The Am95C82 is divided into two basic sections as follows: the Write section and the Read section. Both sections operate independently of each other, but they do not operate concurrently.

WRITE SECTION T-52-38

The Write section encodes the NRZ data stream supplied on WRDAT into the MFM or RLL format. It consists of a sync field translator, MFM and RLL encoders, and

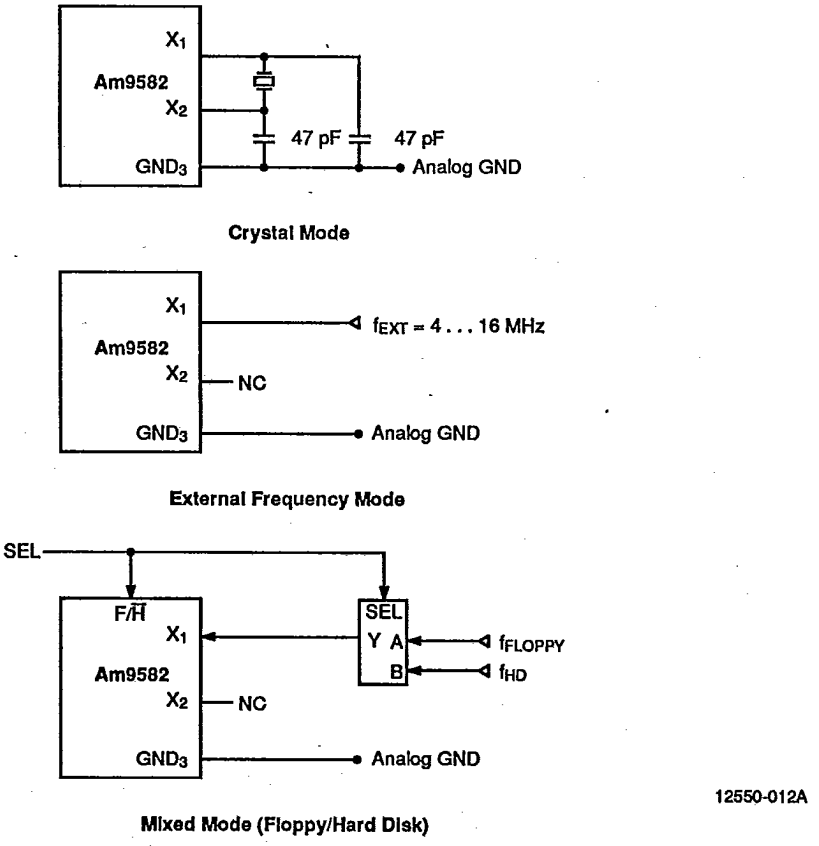
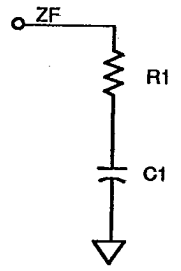
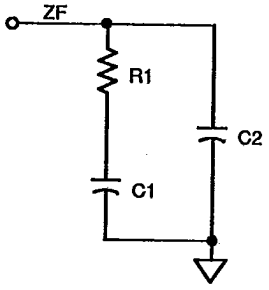


Figure 2. Crystal Oscillator Interfacing



a. Simple Lag-Lead Passive Filter Network



b. Lag-Lead Filter Network w/Ripple Filter Capacitor

Figure 3.

the address mark generator. It performs optional precompensation of the MFM data if desired.

Sync Field Translator

Before any information is written to a sector, a PLO SYNC field is written to the disk. This synchronization field is required by the PLL (Phase-Locked Loop) during reading. For MFM encoding, a pattern of several 0s is used for this purpose. However, this pattern is not suitable for the RLL 2,7 Code. Table 1 shows that the data 000 is encoded into 100100. Since this is a symmetrical pattern, it cannot be used to synchronize properly. Therefore, this application uses the data 11 instead, which translates into the RLL data 0100. The Am9580A/90 sends out a PLO SYNC field of 0s. In order to avoid a special treatment of the sync field in the encoder, all data coming from the HDC is inverted internally to the Am95C82. During a Read operation, NRZ data is inverted again, before being sent to the HDC.

Address Mark Generation T-52-38

Each sector on the disk contains two address marks. They mark the start of the header and the data field. For MFM floppy and in hard disk mode, these address marks are different (see Table 2). To make the address marks unique and always distinguishable from all possible data patterns, the MFM encoding rules are deliberately violated when an address mark is generated. This is done by deleting some of the clock bits in the encoded clock/data pattern. When a sector is read back from the disk, these missing clocks are detected and the disk controller is assured that correct synchronization has taken place. Note for RLL that although the code is unique, the encoding is not violated.

The Am95C82 generates the standard IBM address marks for floppy (IBM) format and hard disk (ST506) formats and a unique address mark for RLL format. AMC (Address Mark Control) is sampled on the rising edge of WRCLK when a Write operation is taking place. The appropriate address mark is then inserted. At completion AMF (Address Mark Found) is brought High in acknowledgment.

The type of address mark generated is dependent on FAM_1, FAM_0, and the operating mode, that is, floppy or hard, and MFM/$\overline{RLL}$. The type of address mark selected is listed in Table 2.

Table 2. Address Mark and Frequency Selection

			Mode Selection			
*MFM/$\overline{RLL}$	F/$\overline{H}$	PCEN/DMP**	FAM_1	FAM_0	MODE	XTAL
1	1	1	0	1	floppy—dump data	16X
1	1	1	1	1	floppy—dump clock	16X
1	1	0	0	0	floppy—IXAM	16X
1	1	0	1	1	floppy id or data	16X
1	0	0	0	0	hard—MFM A1	bit rate
1	0	1	0	1	hard—MFM dump data	bit rate
1	0	1	1	1	hard—MFM dump clock	bit rate
0	0	0	0	0	hard—RLL (2,7)	bit rate
0	0	0	1	0	hard—RLL sync	bit rate

*Code Rate Frequency—"2f" frequency of PLL
**Dump is a mode whereby data (or clock) is passed to the disk controller on an apparent start of address mark (end of apparent Sync Field). This is to enable the recovery of sectors that could not otherwise be read due to corruption of the address mark.

Table 3. Address Marks for Various Operating Modes T-52-38

DOUBLE DENSITY FLOPPY*			
Type	**Data Pattern**	**Clock Pattern**	**Number of Bytes**
IXAM	C2	14	3
DAM and IDAM	A1	0A	3
HARD DISK (MFM)*			
Type	**Data Pattern**	**Clock Pattern**	**Number of Bytes**
DAM and IDAM	A1	0A	1
HARD DISK (RLL)*			
Type	**Data Pattern**	**Clock Pattern**	**Number of Bytes**
DAM and IDAM	04	NA	0.5

*Note: The ID address marks and data address mark for double-density floppy and hard disks are normally qualified by an extra byte following the address mark. However, these extra bytes are normally encoded (no missing clocks), which the controller can easily detect during a Read operation.

Whenever an address mark needs to be written, the HDC asserts the AMC (Address Mark Control) signal. This causes the encoder to write the address mark pattern 00000100. This does not violate the RLL 2,7 encoding scheme, but it is a unique pattern.

The HDC, when starting a Read operation, always asserts AMC to search for an address mark. The decoder starts looking for the sync pattern 0100. This pattern has to occur at least five times before the Am95C82 starts looking for the address mark. This method ensures synchronization at the beginning of a sector.

After an address mark has been recognized, the device waits until the first 4 bits of NRZ data are available in the NRZ shift register and asserts AMF (Address Mark Found). This causes the HDC to interpret the data bit at the next rising edge of RDREF/CLK as the first bit of valid data.

Write Precompensation

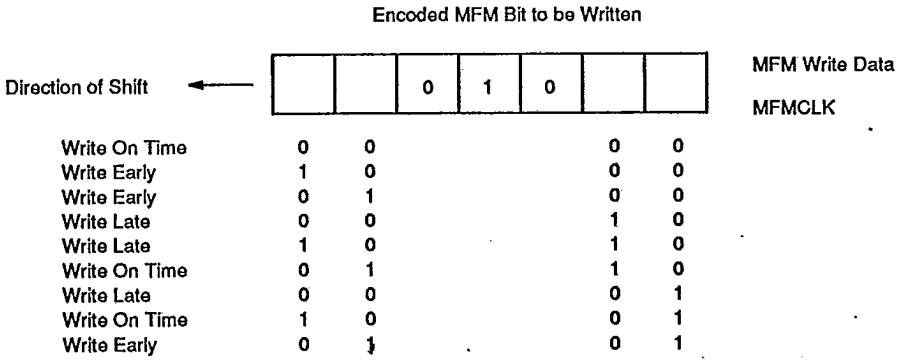
Bit shifting is a phenomenon caused by the flux changes stored on the disk, which are interacting with each other. Its effect is to move nearby flux changes away from each other, creating a timing uncertainty that can cause errors when data is read. This phenomenon is more significant on the inner tracks of a disk because the flux changes are closer together.

To overcome this interaction between flux transitions, the Write Data stream is precompensated; that is, the direction of each bit shift is anticipated and the bit is moved in the other direction by the Am95C82 before being written to the disk. When PCEN is High, precompensation is enabled and each bit will be made either Early, Nominal, or Late, depending on its interaction with its neighbors. The amount of time shift between Early, Nominal, and Late is set by two external resistors on the PCDLY pins. The precompensation procedure is shown in Figure 4 and Figure 5.

If precompensation is enabled, the pulse widths of the Early and Nominal pulses are extended (see Figure 5). The rising edges of the Early, Nominal, and Late pulses show the actual precompensation. Therefore, the rising edge of Write Data should generate a flux transition on the disk drive. The falling edges of Early, Nominal, and Late are always aligned (no precompensation) and therefore should not be used.

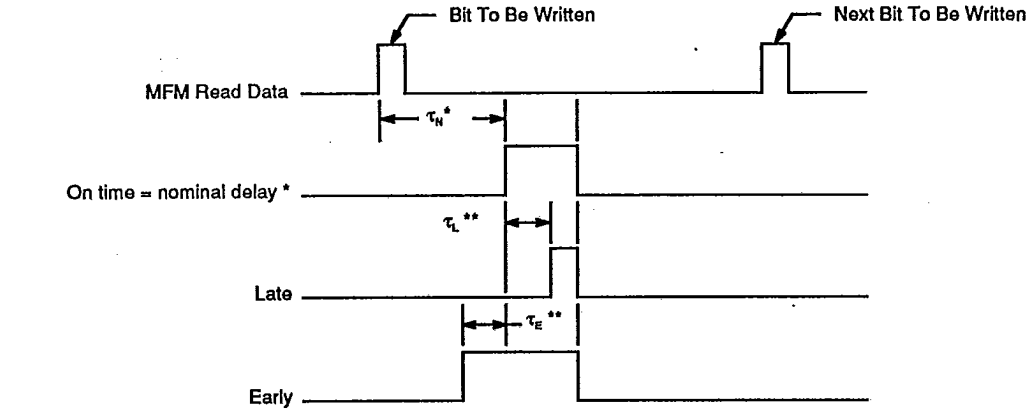
If precompensation is not used, $PCDLY_1$ and $PCDLY_2$ should still be connected to Analog V_{CC} (V_{CC3}), either directly or via pull-up resistor, to ensure proper operation of the Master PLL (required for Read and Write sections).

For RLL (2,7) mode, Write precompensation (if required) has to be performed by external circuitry.



Write On Time	0	0			0	0
Write Early	1	0			0	0
Write Early	0	1			0	0
Write Late	0	0			1	0
Write Late	1	0			1	0
Write On Time	0	1			1	0
Write Late	0	0			0	1
Write On Time	1	0			0	1
Write Early	0	1			0	1

Figure 4. Write Precompensation



*Nominal Delay = τ_N
**τ_E = τ_E= 1%–20% bit cell time

12550-008A

Figure 5. Bit Shifting for Write Precompensation

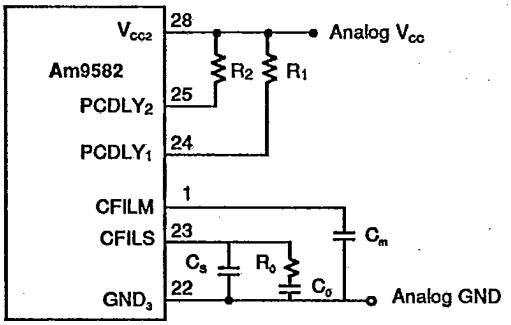


Figure 6. Discrete Components Connection

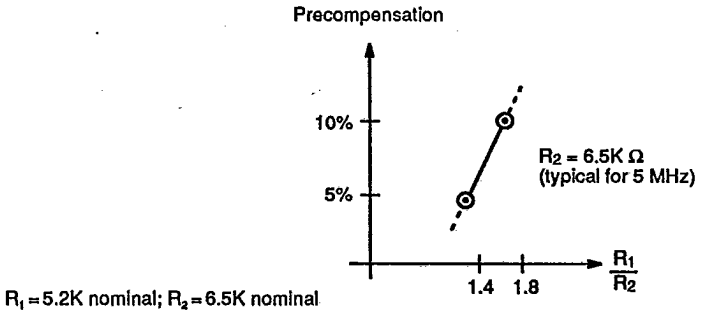


Figure 7. Suggested Resistor Values for Precompensation

READ SECTION

The Read section of the Am95C82 consists of a read data Phase-Locked Loop (PLL), Window Logic, Sync Field Detector, Address Mark Detector, MFM/RLL Decoder, Synchronized Multiplexer, crystal-controlled oscillator, a reference PLL, and a Divide-by-16 counter as shown in the Block Diagram.

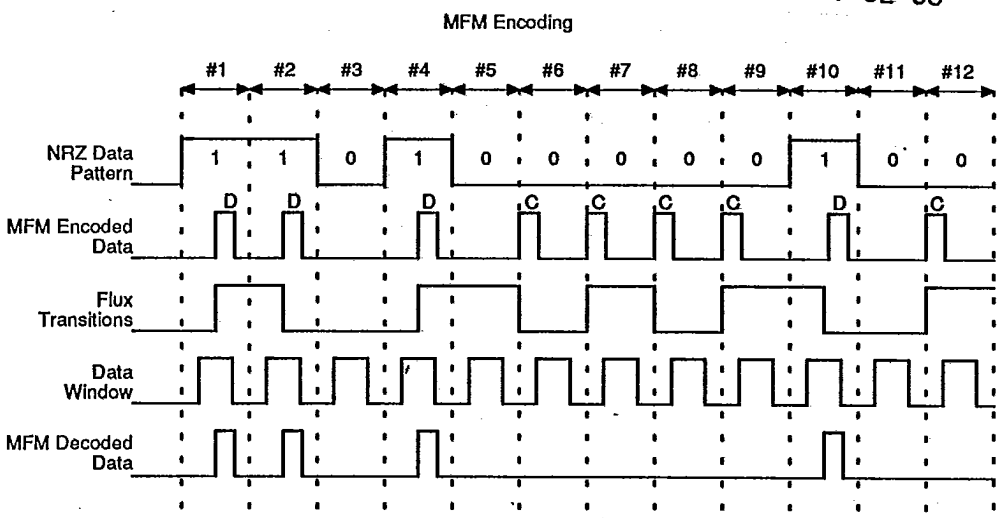
Phase-Locked Loop (PLL)

The main function of the data PLL is to provide a clock signal (shown as 2f in Figure 8) that closely tracks the MFM/RLL serial data read from the disk. The 2f signal is then used to generate clock and data windows.

When the chip is in the Write mode (WG active), the PLL is synchronized to the REFCLK derived from the crystal-controlled oscillator. When data is read from the disk (RG active), the PLL is locked to the data stream from the disk and outputs RDCLK. In either case these output signals are available on the RD/REFCLK pin. In synchronizer-only mode, the Am95C82 provides a "code rate" (2f) clock on the RD/REFCLK pin.

The Sync Field and Address Mark Detector

The Sync Field Detector looks for the code-specific sync field. For MFM the sync field consists of eight consecutive pulses in clock windows generated by the on-chip PLL. When this pattern is detected, the window signal polarity will be frozen. If the sync pattern is not found, the Am95C82 flips the window polarity so that the sync detector can continue to look for the sync pattern. The apparent sync field ending is seen as a pulse in the data window. This action arms an address mark time-out; that is, after 8 bit cells (or 24 bit cells for double-density floppy mode), an address mark must be found or the Am95C82 is reset back to the lowest level of search where it looks for eight apparent 0s (MFM).



*Note: MFM encoding doubles the bit density on the disk by replacing clock bits (C) used in FM encoding with data bits (D). MFM encoding reduces the bit cell by one half.

Figure 8. MFM Encoding*

In RLL mode, the same NRZ input is used for synchronization. However, an inverter is used on both the input of the encoder and the output of the decoder. This converts the NRZ sync pattern from 00 to 11. From Table 1 this pattern translates to the 0100 RLL code sequence placed on the disk (note: in RLL mode, the encoded RLL disk data is that of the inverse of the incoming NRZ data). The choice of the 11 pattern not only provides compatibility with MFM for the NRZ data interface, but also provides a nonsymmetric sync pattern guaranteeing proper alignment of clock and data windows. The sync detector circuitry looks for a minimum of five fields of 0100 before enabling the address mark detection logic to begin searching for the address mark. After address mark detection is enabled the only allowable patterns are the sync pattern and the address mark; any other pattern will cause the address mark detection and the sync field counters to be reset and the sync field search is begun anew.

The detection of various address marks for floppies and hard disks is performed by the Address Mark Detector. The type of address mark to be detected is determined by the signals MFM/$\overline{RLL}$, F/$\overline{H}$, FAM_0, and FAM_1 as shown in Table 2. In response to an active AMC, AMF will be asserted to indicate that the desired address mark has been found during a Read operation, or an appropriate address mark has been written during a Write operation.

Address Mark Recovery with Media Defects

In the normal MFM operating mode the Am95C82 will only detect an address mark if all 8/24 bits match the selected address mark (see Table 2). In the clock/data dump mode the Am95C82 can assist in the detection of damaged address marks. Here, the Am95C82 will assert AMF (Address Mark Found) as soon as it detects the first data bit (pulse in the data window) (see Figure 9). Selectively, the Am95C82 then provides either the clock pattern, which should show the missing clock (coding violation within the address mark, clock dump mode), or the address mark data (data dump mode).

Because of decoding scheme differences these modes are not provided for RLL.

MFM/RLL Decoder

The MFM/RLL decoder converts the incoming MFM/RLL serial data from the disk to NRZ data for the disk controller. If an MFM/RLL pulse occurs in a data window, the NRZ data is decoded as a 1. If no pulse occurs in the data window, the NRZ data is decoded as a 0.

Implementing an RLL encoder/decoder is slightly more complicated, and can require a more elaborate state machine. Before RG is asserted the NRZ and RLL regis-

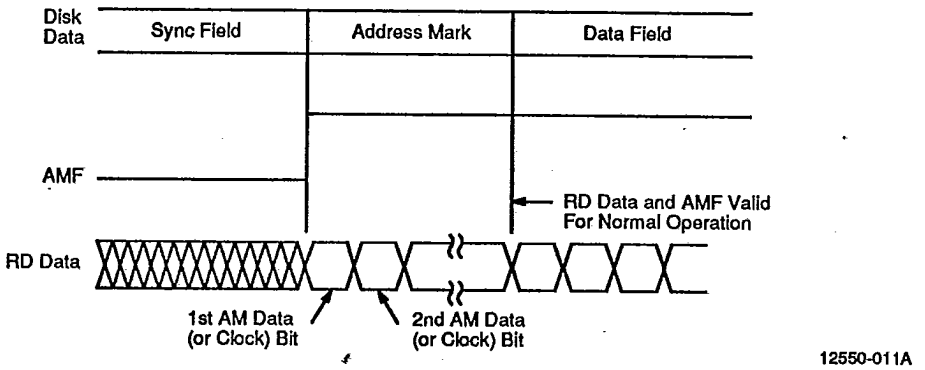


Figure 9. Dump Mode

ters are preset with unique stop patterns. After RG and AMC are asserted to begin a Read operation, the decoder begins looking for the RLL sync pattern 0100. As the RLL bits are loaded into the register the decoder compares them to a look-up table containing the right half of Table 1. When a match is detected, the corresponding NRZ pattern in Table 1 is loaded into the NRZ register and the RLL register value is reset with the unique stop pattern. On detection of a proper address mark the decoder waits until 8 more bits of RLL data have been read into the RLL register, guaranteeing the NRZ register has valid data ready, then asserts AMF. This allows the Hard Disk Controller to interpret the NRZ data bit at the next rising edge of RDREFCLK as the first valid bit of data. Disk data is then read until RG is deactivated, resetting the logic and beginning a search for the sync fields. The scheme works similarly for encoding and decoding, with the NRZ register being loaded from the disk controller. When patterns on the left of Table 1 are matched, the pattern on the right is loaded into the RLL register for shifting out to the disk.

Clock Generator

The clock generator consists of a crystal-controlled oscillator, a PLL locked to the output of the crystal oscillator, and a frequency divider. The oscillator frequency is determined by the X_1 and the X_2 inputs (crystal or TTL-level clock source). The frequency divider divides the oscillator frequency to generate the REFCLK. The appropriate divide ratio is selected internally as shown in Table 2.

The master PLL keeps the data (slave) PLL tuned to its center frequency when the Am95C82 is not reading data. When the Am95C82 is writing data (WG High), the master PLL/divider frequency is output as REFCLK to the disk controller for use during Write operations. When the Am95C82 is reading disk data (RG High), the data PLL is phase locked to the incoming data from the disk. The RDREFCLK output continues to be the REFCLK from the master clock until the proper sync fields are detected when the output switches over without any glitches to the RDCLK output from the data PLL.

Write Precompensation

The Am95C82 performs Write precompensation for MFM-encoded data only. The bit to be written is shifted early or late with respect to a nominal delay. The nominal delay is selected if data is to be written on time. Action to be taken is made by examining an internal 7-bit register through which the MFM-encoded data is passed.

Printed Circuit Board Layout Guidelines

The V_{CC} and ground of the Am95C82 contains PLL and other analog circuitry that demands noise-free power supplies to operate correctly. Therefore, Analog V_{CC} and GND should be connected to the power connector via separate supply lines. They should not be connected directly to the GND and V_{CC} plane of a multilayer PC board. These supply lines should have separate bypass capacitors located as close as possible to the supply inputs.

The filter capacitors (CFILM, CFILS) should be connected between the CFIL inputs of the Am95C82 and Analog GND. The precompensation delay resistors should be connected to Analog V_{CC}.

The crystal should be positioned as close as possible to the crystal oscillator inputs of the Am95C82 (X_1 and X_2). The two crystal capacitors should be connected to Analog GND (see Figure 2).

T-52-38

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65 to +150° C
Supply Voltage to Ground Potential Continuous ..... –0.5 to +7.0 V
DC Voltage Applied to Outputs for High Output State ..... –0.5 V to + Vcc
DC Input Voltage ..... –0.5 V to +7.0 V
DC Output Current into Outputs ..... 30 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

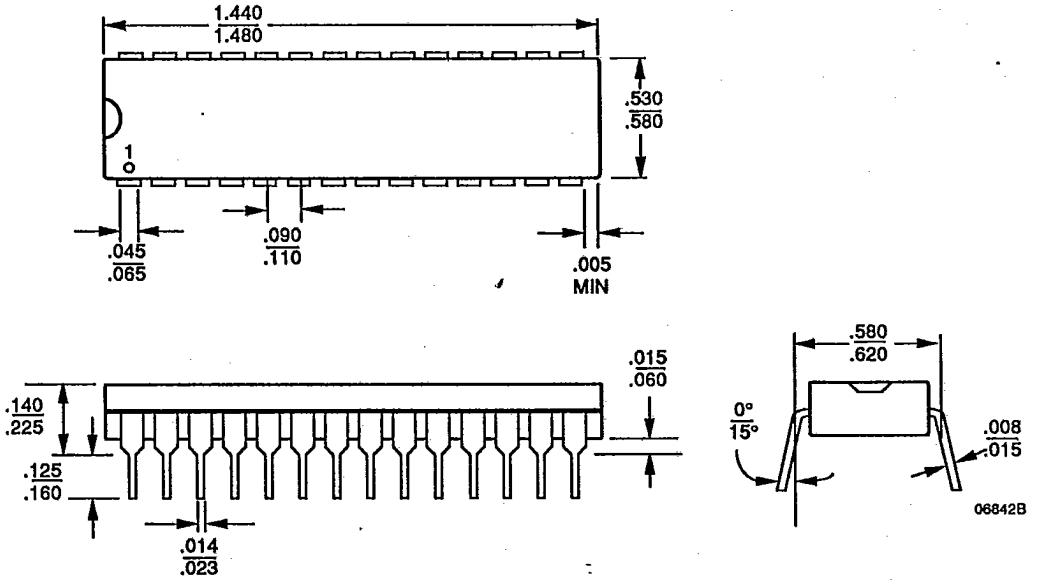
Commercial (C) Devices

Ambient Temperature (T_A) ..... 0 to +70° C
Supply Voltage (V_{CC}) ..... 5 V to ±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

PHYSICAL DIMENSIONS
PD 028
28-pin Plastic DIP

T-52-38



PHYSICAL DIMENSIONS
PL 028
28-pin Plastic Leaded Chip Carrier