MOTOROLA

Product Preview

32K x 9 Bit BurstRAM™ Synchronous Static RAM

ELECTRICALLY TESTED PER:
MPG62486A

62486A

Commercial Plus and Mil/Aero Applications

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 62486A - XX/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CQF: Y

XX = Speed in ns (25, 30, 35)

The Military 62486A is a 294,912 bit synchronous static random access memory designed to provide a burstable, high-performance, secondary cache for the i486 microprocessor. It is organized as 32,768 words of 9 bits, fabricated with Motorola's high-performance silicon-gate CMOS technology. The device integrates input registers, a 2-bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0–A14), data inputs (DQ0-DQ8), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive-edge-triggered non-inverting registers.

Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the Military 62486A (burst sequence imitates that of the i486) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

Write cycles are internally self-timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

The Military 62486A will be available in a 44-pin ceramic quad flat (CQF). Multiple power and ground pins have been utilized to minimize effects induced by output noise. Separate power and ground pins have been employed for DQ0–DQ8 to allow user-controlled output levels of 5 volts or 3.3 volts.

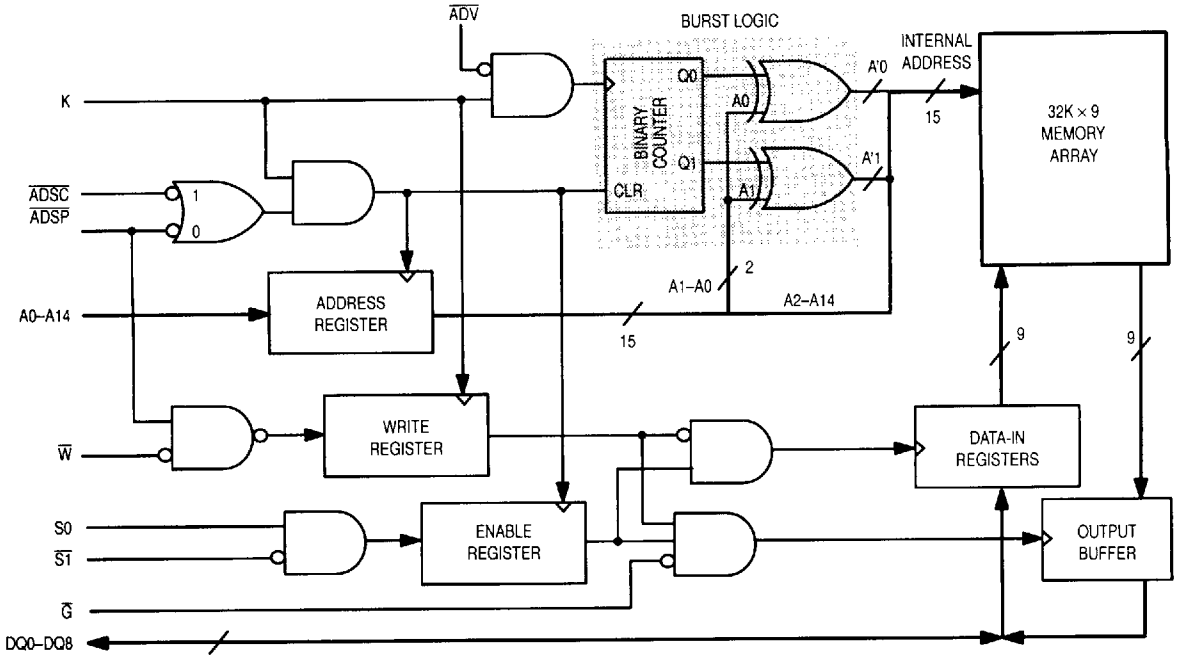
- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Level Compatibility
- Fast Access Times: 15/25/35 ns and Cycle Times: 20/30/40 ns
- Internal Input Registers (Address, Data, Control)
- Internally Self-Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- High Output Drive Capability: 85 pF per I/O
- High Board Density CQF Package
- Fully TTL Compatible
- Active High and Low Chip Select Inputs for Easy Depth Expansion

PIN NAMES	
A0–A14	Address Inputs
K	Clock
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
S0,$\overline{S1}$	Chip Selects
$\overline{ADV}$	Burst Address Advance
$\overline{ADSP}$, $\overline{ADSC}$	Address Status
DQ0–DQ8	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

BurstRAM is a trademark of Motorola, Inc.
i486 is a trademark of Intel Corp.
This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM (See Note)



NOTE: All registers are positive-edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip selects (S0, $\overline{S1}$) are sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**.

BURST SEQUENCE TABLE (See Note)

External Address	A14–A2	A1	A0
1st Burst Address	A14–A2	A1	$\overline{A0}$
2nd Burst Address	A14–A2	$\overline{A1}$	A0
3rd Burst Address	A14–A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, 3, and 4)

S	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{W}$	K	Address Used	Operation
F	L	X	X	X	L-H	N/A	Deselected
F	X	L	X	X	L-H	N/A	Deselected
T	L	X	X	X	L-H	External Address	Read Cycle, Begin Burst
T	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
T	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low-to-high transition of clock (K).
3. S represents S0 and $\overline{ST}$. T implies $\overline{ST}$ = L and S0 = H; F implies $\overline{ST}$ = H or S0 = L.
4. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out (DQ0–DQ8)
Read	H	High-Z
Write	X	High-Z — Data In (DQ0–DQ8)
Deselected	X	High-Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Output Power Supply Voltage	V_{CCQ}	– 0.5 to V_{CC}	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Temperature Under Bias	T_{bias}	– 55 to + 125	°C
Operating Temperature	T_A	– 55 to + 125	°C
Storage Temperature	T_{stg}	– 65 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = – 55 to + 125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	 4.5 3.0	 5.0 3.3	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5 *	0.0	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Typ	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	± 1.0	µA
Output Leakage Current ($\overline{G}$, $\overline{S1}$ = V_{IH}, S0 = V_{IL}, V_{out} = 0 to V_{CCQ})	$I_{lkg(O)}$	± 1.0	µA
AC Supply Current ($\overline{G}$, $\overline{S1}$, = V_{IH}, S0 = V_{IL}, All Inputs = V_{IL} = 0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min)	I_{CCA}	175	mA
Standby Current ($\overline{S1}$ = V_{IH}, S0 = V_{IL}, All Inputs = V_{IL} and V_{IH}, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	40	mA
CMOS Standby Current ($\overline{S1}$ ≥ V_{CC} – 0.2 V, S0 ≤ 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V, Cycle Time ≥ t_{KHKH} min)	I_{SB2}	30	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OLmax}	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OHmin}	2.4	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 bus cycles.

AC TEST LOADS

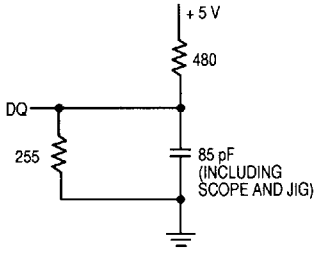


Figure 1A

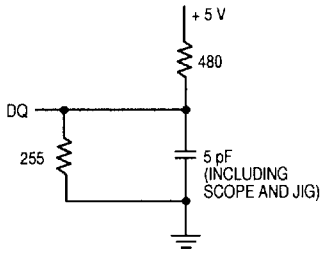
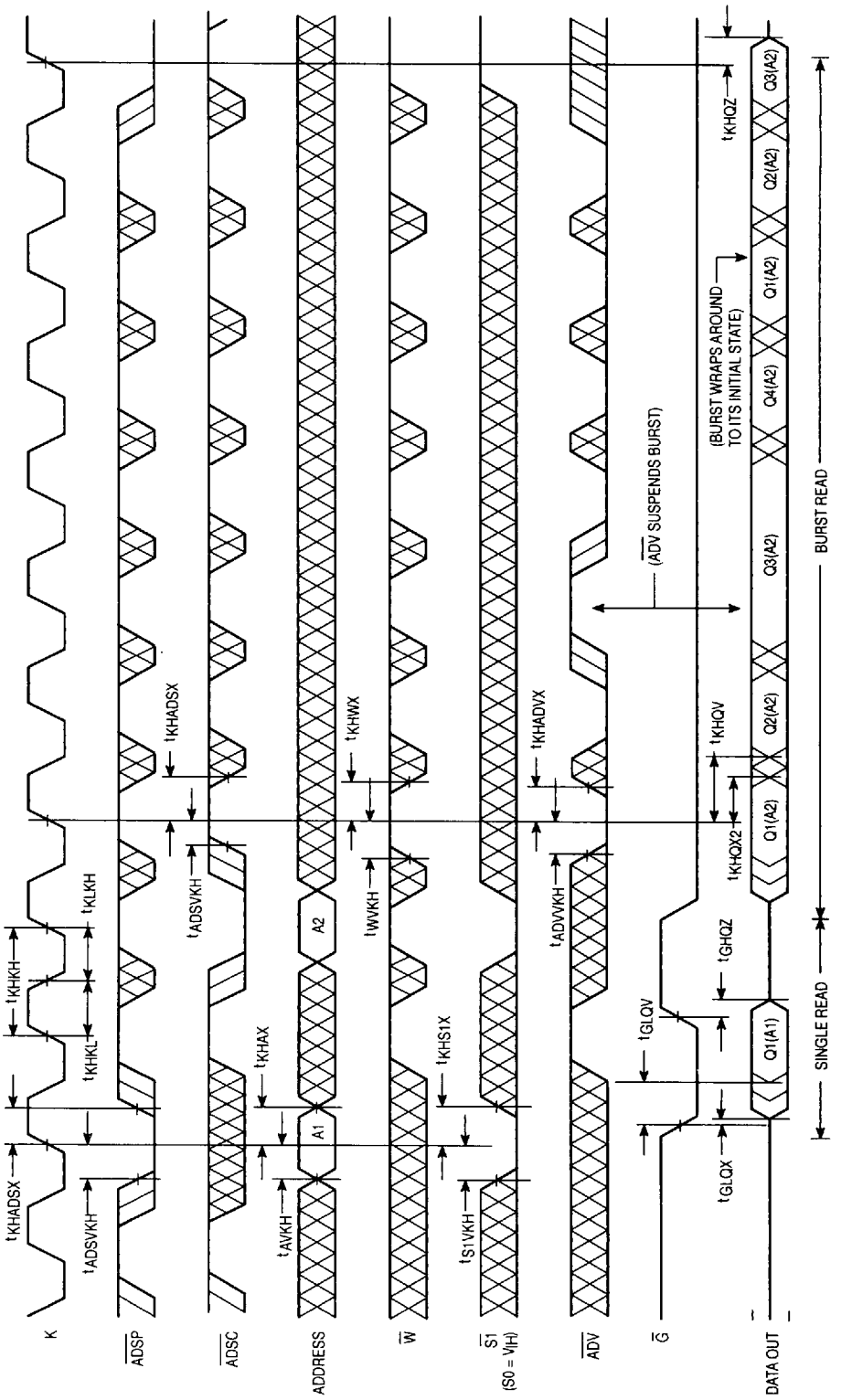


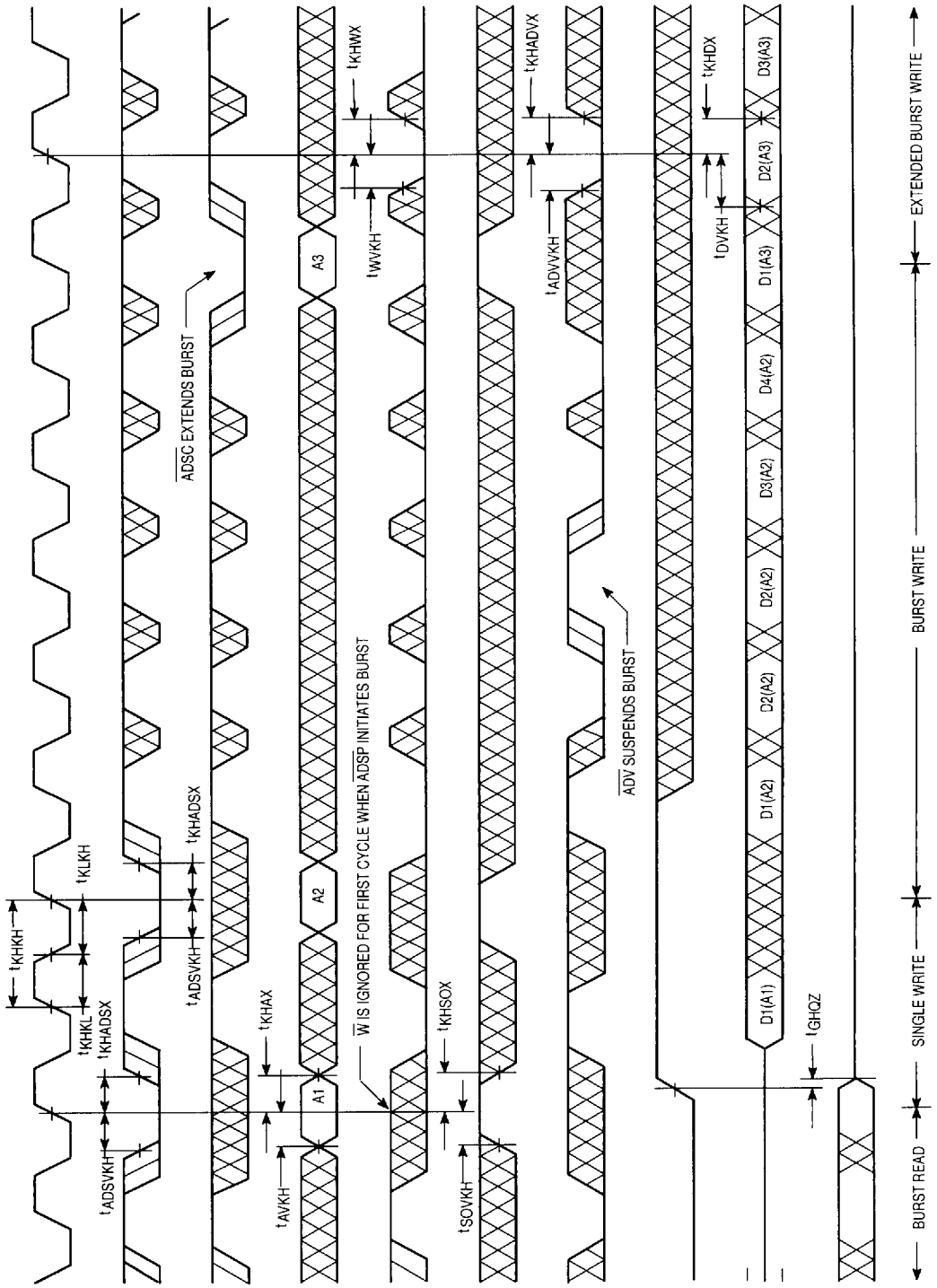
Figure 1B

READ CYCLES

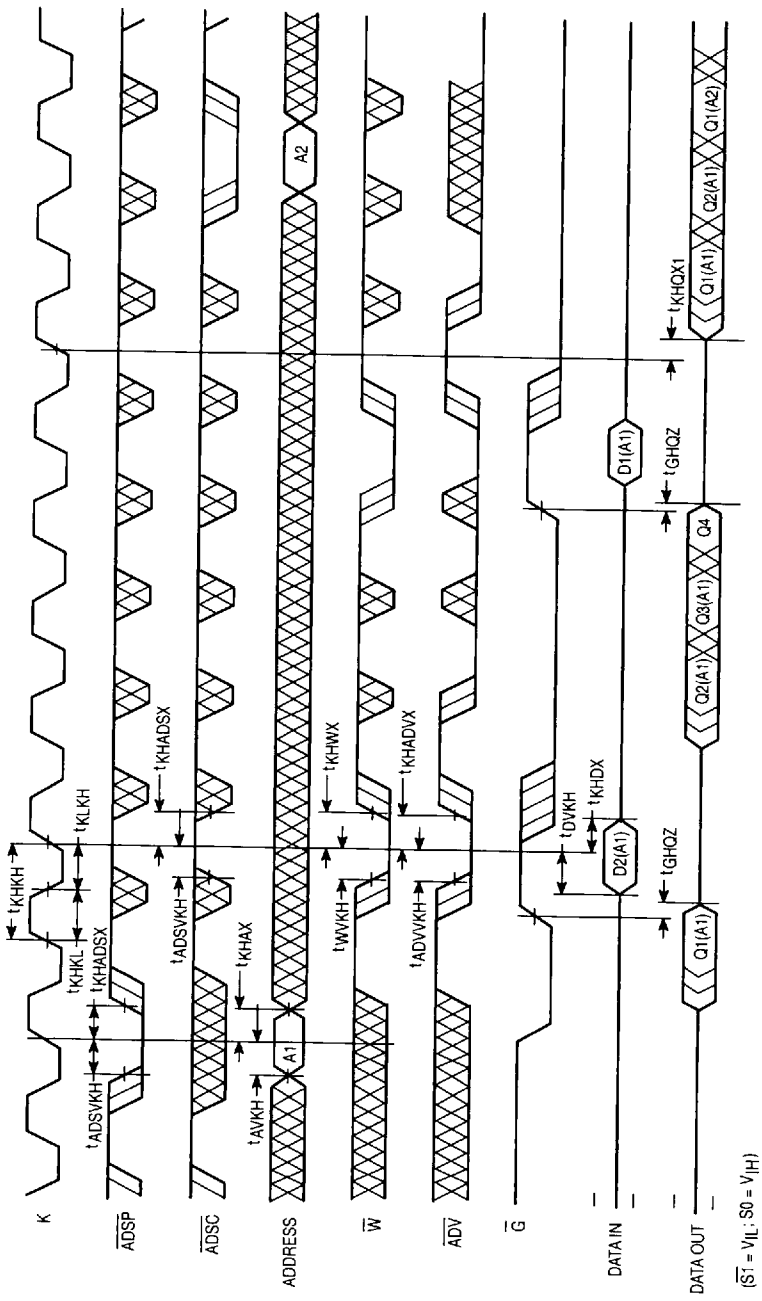


NOTE: Q1(A2) represents the first output data from the base address A2; Q2(A2) represents the next output data in the burst sequence with A2 as the base address.

WRITE CYCLES

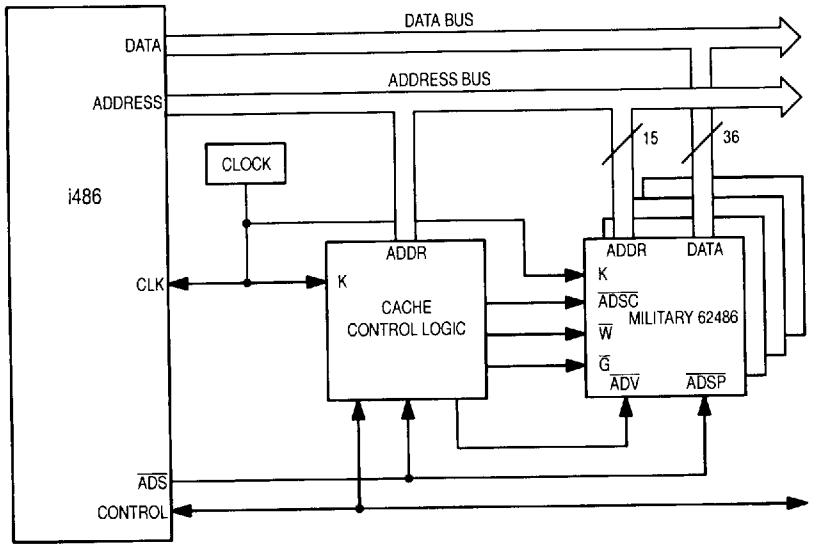


COMBINATION READ/WRITE CYCLES



NOTE: This diagram does not show typical processor cycles, but is intended to show the functionality of the SRAM.

APPLICATION EXAMPLE



128K BYTE BURSTABLE, SECONDARY CACHE USING
4 MILITARY 62486FN24s WITH A 33 MHz i486