REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 03. Inactivate device 01 for new design. Upgrade to full military temperature range. Change drawing CAGE number. Editorial changes throughout.	1988 APR 15	Weckman
B	Add case outline Y. Editorial changes throughout.	1989 SEPT 19	Weckman
C	Technical changes to table I. Changes to figure 1. Added vendor CAGE 48257 for device types 02 and 03. Editorial changes throughout.	1990 AUG 9	Weckman

CURRENT CAGE CODE 67268

REV																								
SHEET																								
REV	B	B	B	B	C																			
SHEET	22	23	24	25	26																			

REV STATUS OF SHEETS	REV	C	C	B	C	C	C	C	C	B	C	C	B	B	B	B	B	B	B	B	B	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE: 24 FEBRUARY 1987

REVISION LEVEL: C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, HCMOS FLOATING-POINT COPROCESSOR, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-86021
A	14933	

SHEET 1 OF 7

DESC FORM 193-1
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

5962-E1770

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-86021	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	68881-12	HCMOS floating point coprocessor
02	68881-16	HCMOS floating point coprocessor
03	68881-20	HCMOS floating point coprocessor

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	P-AB (68-pin, 1.080" x 1.080" x .345"), pin grid array package
Y	See figure 1 (68-lead, .960" x .960" x .135"), leaded chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range with respect to GND (V_{CC})	-0.3 V dc to +7.0 V dc
Storage temperature range	-55°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 5 seconds)	+270°C
Junction temperature (T_J)	+150°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case X	See MIL-M-38510, appendix C
Case Y	10°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
High level input voltage range (V_{IH}):	
All inputs	2.0 V dc to 5.25 V dc
Low level input voltage range (V_{IL}):	
All inputs	GND -0.3 V dc to 0.8 V dc
Minimum high level output voltage	2.4 V dc
Maximum low level output voltage	0.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standarized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Waveform reference 1/	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$ 2/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Input high voltage	V_{IH}			1,2,3	All	2.0	V_{CC}	V
Input low voltage	V_{IL}			1,2,3	All	GND -0.3	0.8	V
Input leakage current $\overline{CLK}$, $\overline{RESET}$, R/$\overline{W}$, A0-A4, $\overline{CS}$, $\overline{DS}$, $\overline{AS}$, $\overline{SIZE}$	I_{IN}		V_{CC} = 5.5 V	1,2,3	All		10	µA
Hi-Z (off-state) input current $\overline{DSACK0}$, $\overline{DSACK1}$, D0-D31	I_{TSI}		V_{IN} = 2.4 V or 0.4 V	1,2,3	All		20	µA
Supply current	I_{CC}		V_{CC} = 5.5 V 3/	1,3 2	All		190 60	mA
Output low current $\overline{SENSE}$	I_{OL}		V_{OL} = GND 4/		All		500	µA
Output high voltage $\overline{DSACK0}$, $\overline{DSACK1}$, D0-D31	V_{OH}		I_{OH} = -400 µA	1,2,3	All	2.4		V
Output low voltage $\overline{DSACK0}$, $\overline{DSACK1}$, D0-D31	V_{OL}		I_{OL} = 5.3 mA	1,2,3	All		0.5	V
Capacitance	C_{IN}		(V_{IN} = 0 V, T_C = +25°C F = 1 MHz), see 4.3.1c	4			20	pF
Functional testing			See 4.3.1d	7,8	All			
Frequency of operation	f_{MAX}		V_{IH} = 2.4 V, V_{IL} = 0.5 V See figure 4	9,10,11	01 02 03	8.0 8.0 12.5	12.5 16.67 20	MHz
Clock period	t_{CYC}	1		9,10,11	01 02 03	80 60 50	125 125 80	ns
Clock width low	t_{CL}	2		9,10,11	01 02 03	32 24 20	87 95 54	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Waveform reference 1/	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$ 2/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Clock width high	t_{CH}	3	$V_{IH} = 2.4\ V$, $V_{IL} = 0.5\ V$ See figure 4	9,10,11	01 02 03	32 24 20	87 95 54	ns
Clock fall time	t_{CF}	4		9,10,11	All		5	ns
Clock rise time	t_{CR}	5		9,10,11	All		5	ns
Address valid to $\overline{AS}$ asserted	t_{AVASL}	6 5/		9,10,11	01 02 03	20 15 10		ns
Address valid (read) to $\overline{DS}$ asserted	t_{AVRDSL}	6a 5/		9,10,11	01 02 03	20 15 10		ns
Address valid (write) to $\overline{DS}$ asserted	t_{AVWDSL}	6b 5/		9,10,11	01 02 03	65 50 50		ns
$\overline{AS}$ negated to address invalid	t_{ASHAX}	7 6/		9,10,11	01 02 03	15 10 10		ns
$\overline{DS}$ negated to address invalid	t_{DSHAX}	7a 6/		9,10,11	01 02 03	15 10 10		ns
$\overline{CS}$ asserted to $\overline{AS}$ asserted	t_{CVASL}	8 7/		9,10,11	01 02 03	0 0 -1		ns
$\overline{CS}$ asserted (read) to $\overline{DS}$ asserted	t_{CVRDSL}	8a 8/		9,10,11	01 02 03	0 0 -1		ns
$\overline{CS}$ asserted (write) to $\overline{DS}$ asserted	t_{CVWDSL}	8b		9,10,11	01 02 03	45 35 30		ns
$\overline{AS}$ negated to $\overline{CS}$ negated	t_{ASHCX}	9		9,10,11	All	10		ns
$\overline{DS}$ negated to $\overline{CS}$ negated	t_{DSHCX}	9a		9,10,11	All	10		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Waveform reference 1/	Conditions $-55°C < T_C < +125°C$ unless otherwise specified $4.5\ V \leq V_{CC} \leq 5.5\ V$ 2/	Group A subgroups	Device type	Limits Min	Limits .Max	Unit
R/$\overline{W}$ high (read) to $\overline{AS}$ asserted	t_{RVASL}	10	$V_{IN} = 2.4\ V$, $V_{IL} = 0.5\ V$ See figure 4	9,10,11	01 02 03	20 15 10		ns
R/$\overline{W}$ high (read) to $\overline{DS}$ asserted	t_{RVDSL}	10a		9,10,11	01 02 03	20 15 10		ns
R/$\overline{W}$ low (write) to $\overline{DS}$ asserted	t_{RLSL}	10b		9,10,11	01 02 03	45 35 30		ns
$\overline{AS}$ negated to R/$\overline{W}$ low (read) or $\overline{AS}$ negated to R/$\overline{W}$ high (write)	t_{ASHRX}	11		9,10,11	01 02 03	15 10 10		ns
$\overline{DS}$ negated to R/$\overline{W}$ low (read) $\overline{DS}$ negated to R/$\overline{W}$ high (write)	t_{DSHRX}	11a		9,10,11	01 02 03	15 10 10		ns
$\overline{DS}$ width asserted (write)	t_{DSL}	12		9,10,11	01 02 03	50 40 38		ns
$\overline{DS}$ width negated	t_{DSH}	13 9/			01 02 03	50 40 38		ns
$\overline{DS}$ negated to $\overline{AS}$ asserted	t_{DSHASL}	13a 9/ 10/			01 02 03	40 30 30		ns
$\overline{CS}$, $\overline{DS}$ (read) asserted to data-out valid	t_{DSLDO}	14 11/		9,10,11	01 02 03		110 80 60	ns
$\overline{DS}$ (read) negated to data-out invalid	t_{DSHDO}	15		9,10,11	All	0		ns
$\overline{DS}$ (read) negated to data-out high impedance	t_{DSHDZ}	16 9/			01 02 03		70 50 40	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Waveform reference 1/	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$ 2/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Data-in valid to $\overline{DS}$ (write) asserted	t_{DIDSL}	17	$V_{IN} = 2.4\ V$, $V_{IL} = 0.5\ V$ See figure 4	9,10,11	01	20		ns
					02	15		
					03	10		
$\overline{DS}$ (write) negated to data-in invalid	t_{DSHDI}	18		9,10,11	01	20		ns
					02	15		
					03	10		
$\overline{START}$ true to $\overline{DSACKO}$ and $\overline{DSACKI}$ asserted	t_{SLDAL}	19 11/12/		9,10,11	01	70		ns
					02	50		
					03	35		
$\overline{DSACKO}$ asserted to $\overline{DSACKI}$ asserted (skew)	t_{DADAS}	19a 4/ 13/			01	-20	20	ns
					02	-15	15	
					03	-10	10	
$\overline{DSACKO}$ to $\overline{DSACKI}$ (read) asserted to data-out valid	t_{DALDO}	20		9,10,11	01		60	ns
					02		50	
					03		43	
$\overline{START}$ false to $\overline{DSACKO}$ and $\overline{DSACKI}$ negated	t_{SHDAH}	21 12/		9,10,11	01		70	ns
					02		50	
					03		40	
$\overline{START}$ false to $\overline{DSACKO}$ and $\overline{DSACKI}$ high impedance	t_{SJDAZ}	22 9/ 12/			01		90	ns
					02		70	
					03		55	
$\overline{START}$ true to clock high (sync read)	t_{DSLCH}	23 12/14/		9,10,11	All	0		ns
Clock low to data-out valid (sync read)	t_{CLDO}	24 14/		9,10,11	01		140	ns
					02		105	
					03		80	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Waveform reference 1/	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$ 2/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
START true to data-out valid (sync read)	t_{DSSLDO}	25 12/ 14/ 15/	$V_{IN} = 2.4\ V$, $V_{IL} = 0.5\ V$ See figure 4	9,10,11	01	1.5 t_{cyc}	140+ 2.5 t_{cyc}	ns
					02	1.5 t_{cyc}	105+ 2.5 t_{cyc}	
					03	1.5 t_{cyc}	80+ 2.5 t_{cyc}	
Clock low to DSACK0 and DSACK1 asserted (sync read)	t_{CLDAL}	26 14/		9,10,11	01 02 03		100 75 55	ns
START true to DSACK0 and DSACK1 asserted (sync read)	t_{DSLDAL}	27 12/ 14/ 15/		9,10,11	01		100+ 2.5 t_{cyc}	ns
					02		75+ 2.5 t_{cyc}	
					03		55+ 2.5 t_{cyc}	

See footnotes on next page.

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1/ The waveform reference number refers to the position where the parameter appears on figure 3.

2/ T_C = -55°C and +125°C in a power off condition under thermal soak for 4 minutes minimum or until thermal equilibrium. Electrical parameters are tested instant on 100 ms after power is applied.

3/ All outputs unloaded except for load capacitance. Clock at f_{MAX}. Part in reset.

4/ Cannot be tested. Provided for system design purposes only.

5/ If the $\overline{SIZE}$ pin is not strapped to either V_{CC} or GND, it must have the same setup times as do addresses plus 5 ns.

6/ If the $\overline{SIZE}$ pin is not strapped to either V_{CC} or GND, it must have the same hold times as do addresses.

7/ $\overline{CS}$ must either be asserted or negated when $\overline{AS}$ is asserted.

8/ $\overline{CS}$ must either be asserted or negated when $\overline{DS}$ is asserted (read).

9/ As a minimum, tested initially and after design or process changes only.

10/ This specification only applies to systems in which back-to-back accesses (read-write or write-write) of the coprocessor interface operand register can occur. When the device is used as a coprocessor to the main processor, this can occur when the addressing mode is immediate.

11/ These specifications only apply if the device had completed all operations initiated by the termination of the previous bus cycle when $\overline{DS}$ was negated. Bus cycles which initiate operations in this manner are:
Write to coprocessor interface control register LSB
Write to coprocessor interface restore register LSB
Last write to coprocessor interface operand register LSB during restore with "busy" state size.
First read to coprocessor interface operand register LSB during save "idle" or "busy" state size.
Following one of these bus cycles, all operations are completed within four clocks after $\overline{DS}$ is negated. If an asynchronous read/write bus cycle is attempted prior to the completion of these operations, the new bus cycle is postponed by $\overline{DSACK0}$-$\overline{DSACK1}$ (and data for reads) being withheld. $\overline{DSACK0}$-$\overline{DSACK1}$ (and data for reads) are also withheld on asynchronous reads/writes of the coprocessor interface operand register and register selector register when the MPU overturns the device. Since the devices clock may be much slower than the MPUs clock, these registers could be empty/full when the MPU attempts to read/write.

12/ $\overline{START}$ is not an external signal, rather, it is the logical condition that indicates the start of an access. The logical equation for this condition is:
$\overline{START} = \overline{CS} + \overline{AS} + (R/\overline{W} + \overline{DS})$.

13/ This number can be reduced to 5 ns if $\overline{DSACK0}$ and $\overline{DSACK1}$ have equal loads.

14/ Synchronous reads occur only when the coprocessor interface save register or response register locations are read.

15/ Value depends on actual clock input waveform used and not clock input specifications.

Case outline Y

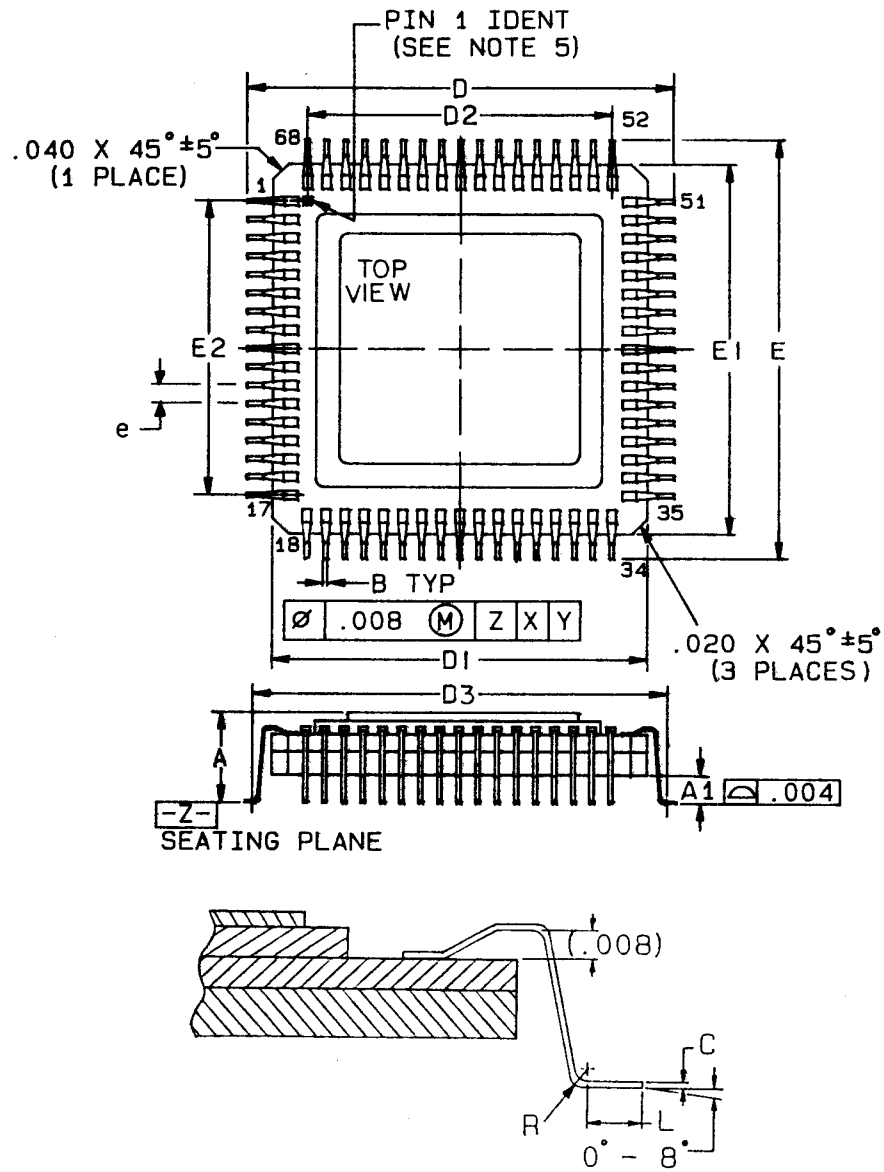

FIGURE 1. Dimensions and configuration.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-86021
		REVISION LEVEL C	SHEET 10

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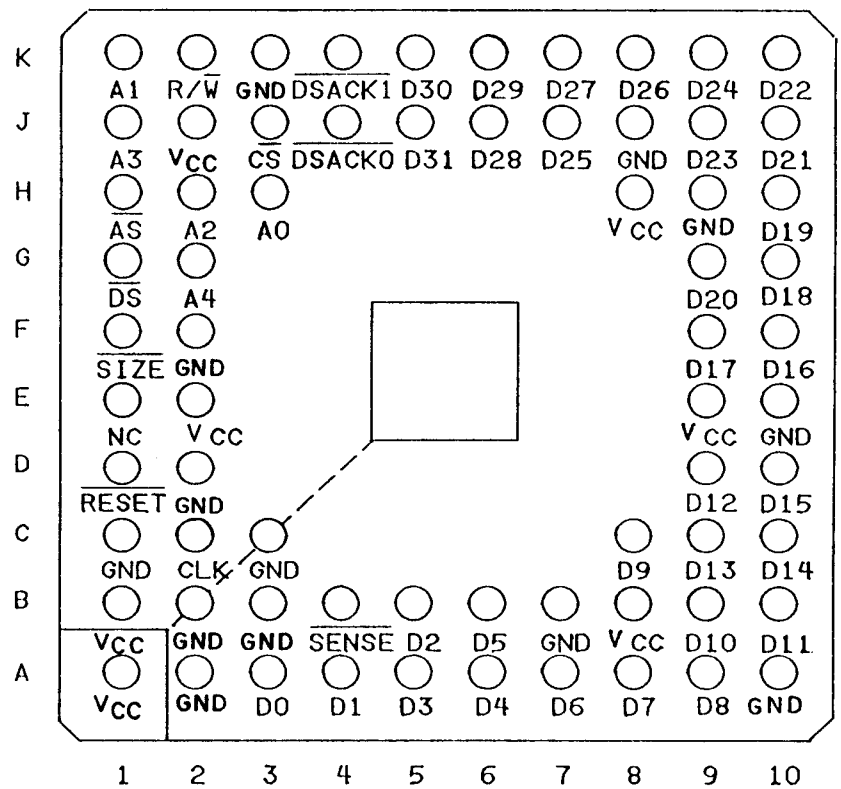
Case outline Y					
Dim	Inches		Millimeters		Note
	Min	Max	Min	Max	
A		.135		3.43	
A_1	.015	.038	0.38	0.96	
B	.013	.025	0.33	0.64	4
C	.004	.010	0.10	0.25	4
D, E	1.130	1.150	28.70	29.21	
D_1, E_1	.935	.960	23.75	24.38	3
D_2, E_2	.800 BSC		20.32		
D_3	1.080 TYP		27.43		
e	.050 BSC		1.27		
L	.022	.038	0.56	0.96	
N	68		68		7
R	.012 TYP		0.30		

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. D_1 and E1 dimensions do not include particles of package material. Such particles shall not exceed .010 inch.
4. Maximum lead thickness includes all lead finishes. Minimum dimension is base material.
5. A pin one identification mark shall be located adjacent to pin one within the shaded area shown.
6. Controlling dimension: Inch.
7. Dimension N is the number of terminal leads.
8. Corner chamfers, notches, or both are optional.

FIGURE 1. Dimensions and configuration - Continued.

Device types 01, 02, and 03

Case outline X



BOTTOM VIEW

FIGURE 2. Terminal connections.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-86021
		REVISION LEVEL B	SHEET 12

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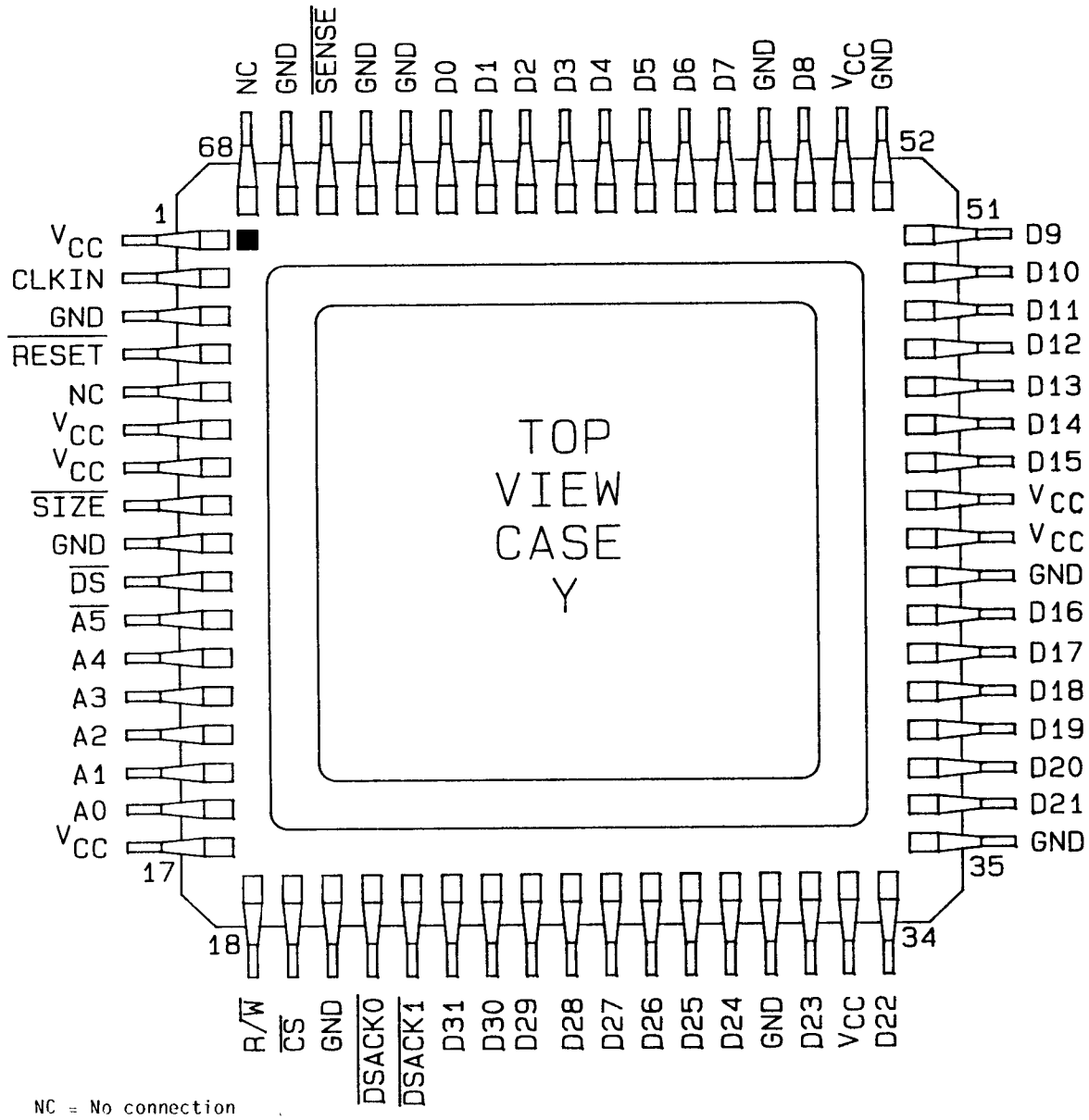
Device types 02 and 03

Case Y



NC = No connection

FIGURE 2. Terminal connections - Continued.

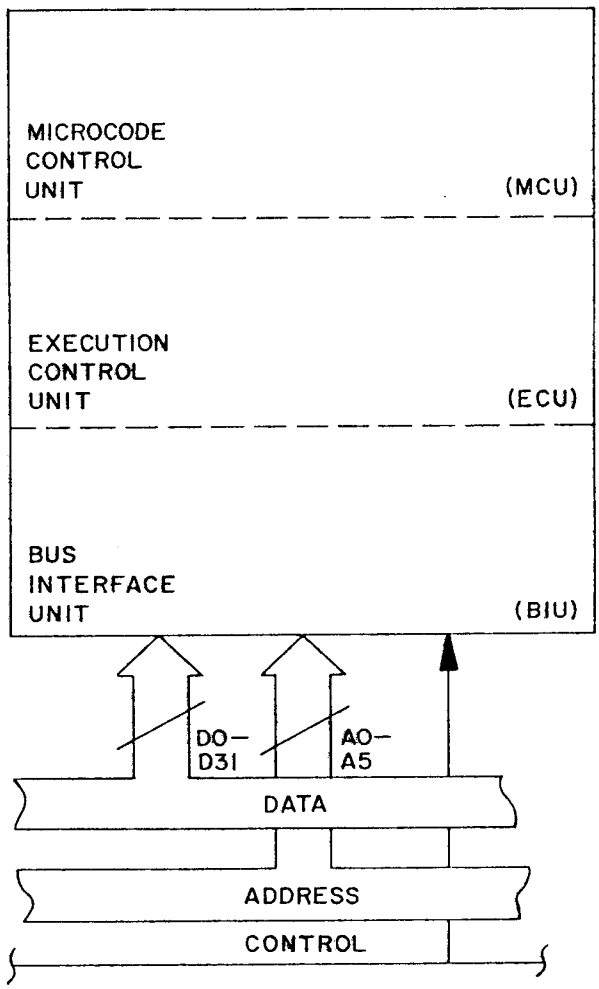
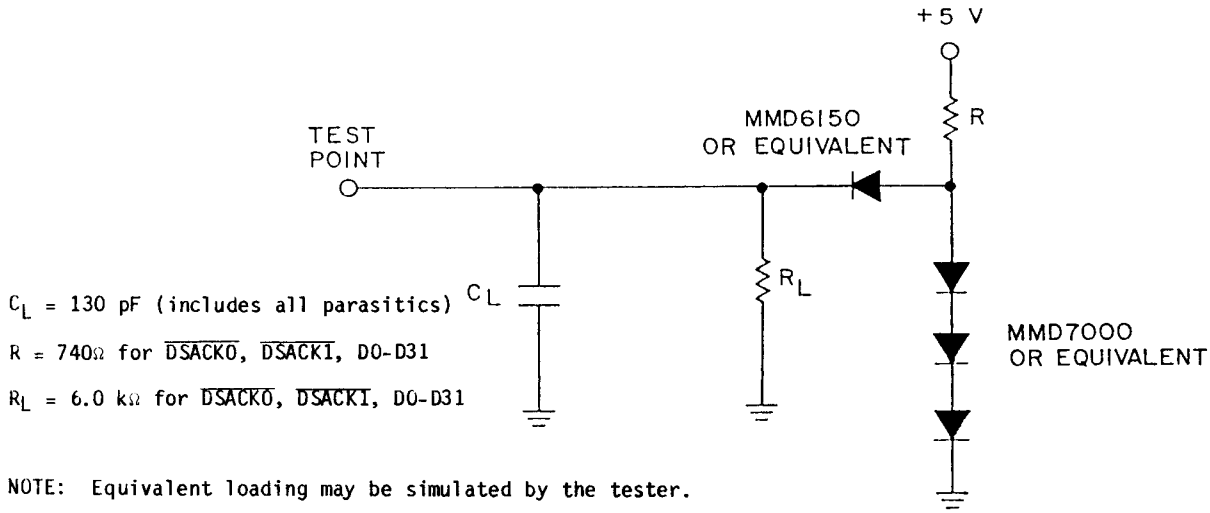


FIGURE 3. Functional block diagram.



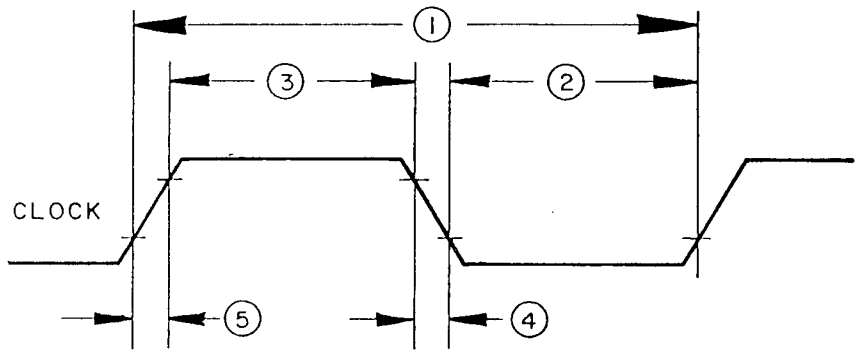
C_L = 130 pF (includes all parasitics)

R = 740Ω for $\overline{DSACK0}$, $\overline{DSACK1}$, D0-D31

R_L = 6.0 kΩ for $\overline{DSACK0}$, $\overline{DSACK1}$, D0-D31

NOTE: Equivalent loading may be simulated by the tester.

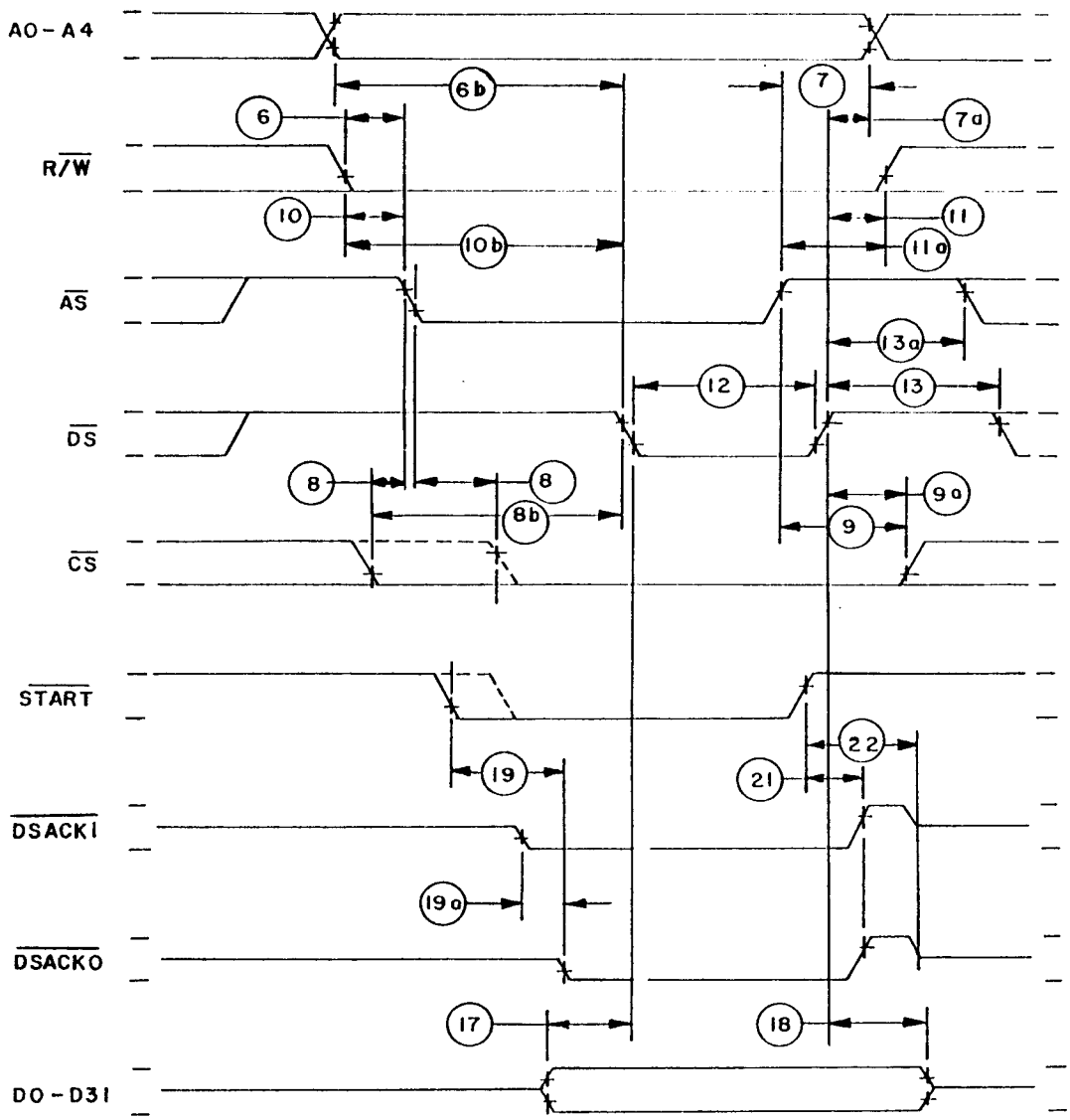
TEST CIRCUIT



CLOCK INPUT AC TIMING DIAGRAM

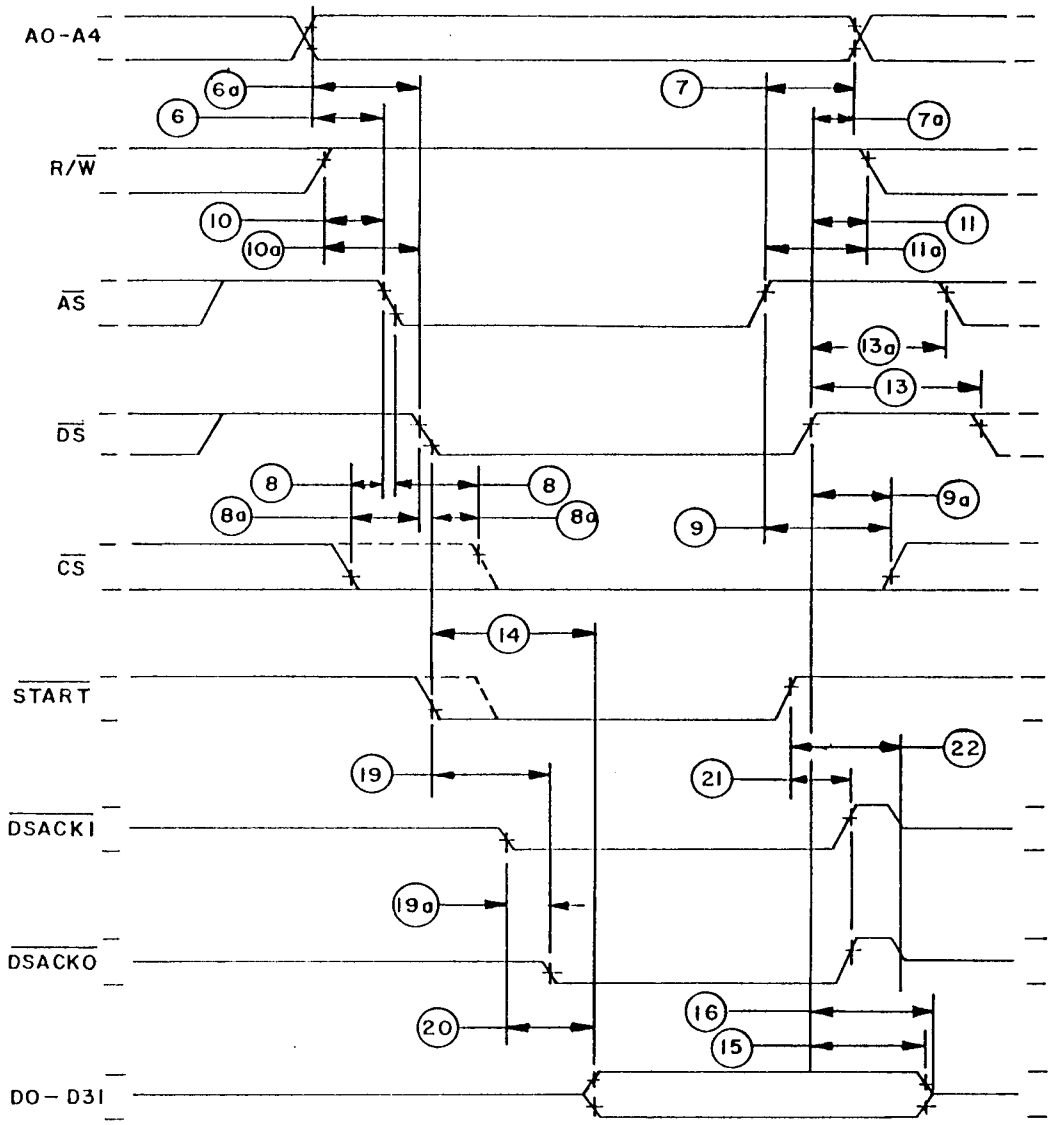
NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

FIGURE 4. Switching test circuit and waveforms.



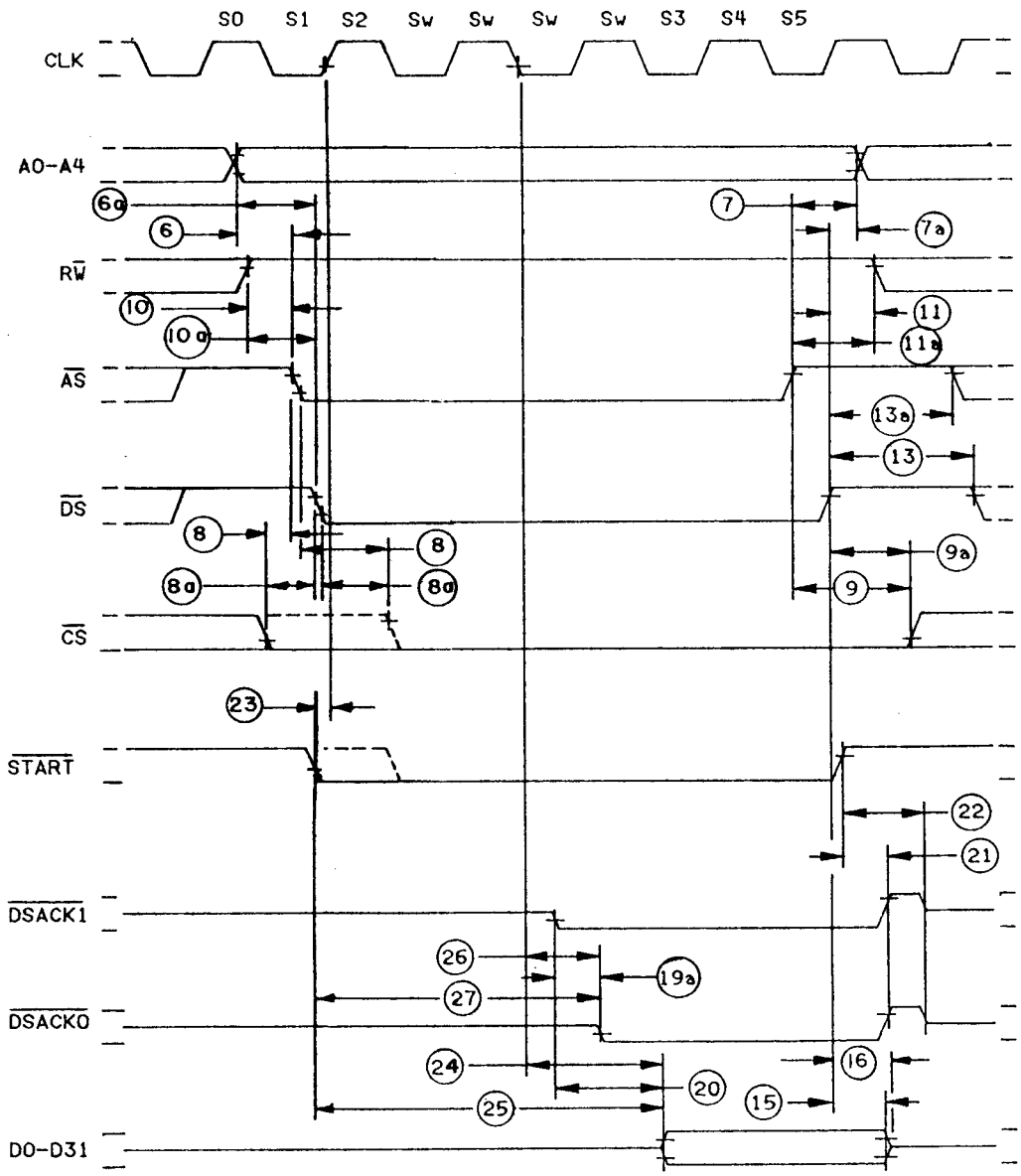
Asynchronous write cycle timing diagram

FIGURE 4. Switching test circuit and waveforms - Continued.



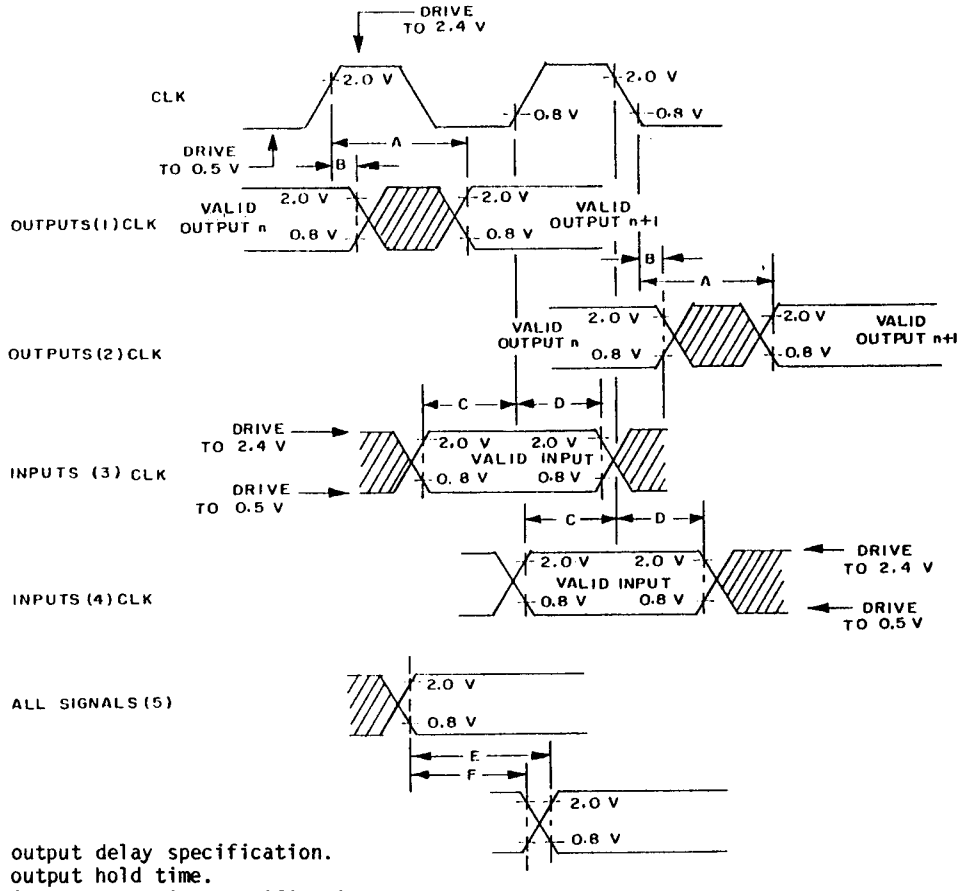
Asynchronous read cycle timing diagram

FIGURE 4. Switching test circuit and waveforms - Continued.



Synchronous read cycle timing diagram

FIGURE 4. Switching test circuit and waveforms - Continued.



LEGEND:
- A - Maximum output delay specification.
- B - Minimum output hold time.
- C - Minimum input setup time specification.
- D - Minimum input hold time specification.
- E - Signal valid to signal valid specification (maximum or minimum).
- F - Signal valid to signal invalid specification (maximum or minimum).

NOTES:
1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This output timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the rising edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

FIGURE 4. Switching test circuit and waveforms - Continued.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of five devices with zero rejects shall be required.

d. Subgroups 7 and 8 functional testing shall include verification of instruction set. The instruction set forms a part of the vendor's test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1, 7, 9
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8 (+125°C), 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	2, 7, 8 (+125°C), 9, 10

* PDA applies to subgroup 1.
** Subgroup 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.6 Symbols, definitions, and funtional descriptions. The symbols, definitions, and functional description for this device shall be as follows:

Signal summary.

Signal name	Mnemonic	Input/ output	Active state	Three-state
Address bus	A0-A4	Input	High	
Data bus	D0-D31	Input/output	High	Yes
Size	$\overline{SIZE}$	Input	Low	
Address strobe	$\overline{AS}$	Input	Low	
Chip select	$\overline{CS}$	Input	Low	
Read/write	R/$\overline{W}$	Input	High/low	
Data strobe	$\overline{DS}$	Input	Low	
Data transfer and size acknowledge	$\overline{DSACK0}$, $\overline{DSACK1}$	Output	Low	
Reset	$\overline{RESET}$	Input	Low	
Clock	CLK	Input		
Sense device	$\overline{SENSE}$	Input/output	Low	No
Power input	V_{CC}	Input		
Ground	GND	Input		

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Address bus (A0 through A4). These active-high address line inputs are used by the main processor to select the coprocessor interface register locations located in the CPU address space. When the device is configured to operate over an 8-bit system data bus, the A0 pin is used as an address lead for byte accesses of the coprocessor interface registers. When the device is configured to operate over a 16- or 32-bit system data bus, both the A0 and $\overline{SIZE}$ pins are strapped high and/or low as listed in table I.

Data bus (D0 through D31). This 32-bit, bidirectional, three-state bus serves as the general-purpose data path between the main processor and the device. Regardless of whether the device is operated as a coprocessor or a peripheral processor, all interprocessor transfers of instruction information, operand data, status information, and requests for service occur as standard similar family bus cycles. The device may be configured to operate over an 8-, 16-, or 32-bit system data bus. Depending upon the system data bus configuration, both the A0 and $\overline{SIZE}$ pins are configured specifically for the applicable bus configuration. (Refer to the address bus (A0 through A5) and size ($\overline{SIZE}$) for further details.)

Size ($\overline{SIZE}$). This active low input signal is used in conjunction with the A0 pin to configure the device for operation over an 8-, 16-, or 32-bit system data bus. When the device is configured to operate over a 16- or 32-bit system data bus, both the $\overline{SIZE}$ and A0 pins are strapped high and/or low as listed in table I.

Address strobe ($\overline{AS}$). This active low input signal indicates that there is a valid address on the address bus, and both the chip select ($\overline{CS}$) and read/write (R/$\overline{W}$) signal lines are valid.

Chip select ($\overline{CS}$). This active low input signal enables the main processor access to the device coprocessor interface registers. When operating the device as a peripheral processor, the chip select decode is system dependent (i.e., like the chip select on any peripheral). The $\overline{CS}$ signal must be valid when $\overline{AS}$ is asserted.

Read/write (R/$\overline{W}$). This active low input signal indicates the direction of a bus transaction (read/write) by the main processor. A logic high (1) indicates a read from the device, and a logic low (0) indicates a write to the device. The R/$\overline{W}$ signal must be valid when $\overline{AS}$ is asserted.

Data strobe ($\overline{DS}$). This active low input signal indicates that there is valid data on the data bus during a write bus cycle.

Data transfer and size acknowledge ($\overline{DSACK0}$, $\overline{DSACK1}$). These active-low, three-state output signals indicate the completion of a bus cycle to the main processor. The device asserts either one or both of the $\overline{DSACK0}$ and $\overline{DSACK1}$ signals upon receipt of a $\overline{CS}$ assertion. If the bus cycle is a main processor read, the device asserts $\overline{DSACK0}$ and $\overline{DSACK1}$ signals to indicate that the information on the data bus is valid. (Both $\overline{DSACK}$ signals may be asserted in advance of the valid data being placed on the bus.) If the bus cycle is a main processor write to the device, $\overline{DSACK0}$ and $\overline{DSACK1}$ are used to acknowledge acceptance of the data by the device. The device also uses $\overline{DSACK0}$ and $\overline{DSACK1}$ signals to dynamically indicate to the main processor to "port" size (system data bus width) on a cycle-by-cycle basis. Depending upon which of the two $\overline{DSACK}$ pins are asserted in a given bus cycle, the main processor will assume data has been transferred to/from an 8-, 16-, or 32-bit wide data port. Table I lists the $\overline{DSACK}$ assertions that are used by the device for the various bus cycles over the various system data bus configurations. Table I indicates that all accesses where A4 equals zero are to 16-bit registers. The device implements all 16-bit coprocessor interface registers on data lines D16-D31; the main processor expects 16-bit registers that are located in a 32-bit port at odd word addresses (A1 = 1) to be implemented on data lines D0-D15. For accesses to these registers when configured for 32-bit bus operation, the device generates $\overline{DSACK}$ signals as listed in table I to inform the main processor of valid data on D16-D31 instead of D0-D15. An external holding register is required to maintain both $\overline{DSACK0}$ and $\overline{DSACK1}$ high between bus cycles. The $\overline{DSACK0}$ and $\overline{DSACK1}$ lines are actively pulled up (negated) by the device following the rising edge of AS and both $\overline{DSACK}$ lines are then three-stated (high-impedance state) to avoid interference with the next bus cycle.

Reset ($\overline{\text{RESET}}$). This active-low input signal causes the device to initialize the floating-point data registers to nonsignaling not-a-numbers (NANs) and clears the floating-point control, status, and instruction address registers. When performing a power-up reset, the external circuitry should keep the $\overline{\text{RESET}}$ line asserted for a minimum of four clock cycles after V_{CC} is within tolerance. This assures correct initialization of the device when power is applied. For compatibility with all family devices, 100 milliseconds should be used at the minimum. When performing a reset after the device V_{CC} has been within tolerance for more than the initial power-up time, the $\overline{\text{RESET}}$ line must have an asserted pulse width which is greater than two clock cycles. For compatibility with all similar family devices, 10-clock cycles should be used as the minimum.

Clock (CLK). The device clock input is a TTL-compatible signal that is internally buffered for development of the internal clock signals. The clock input must be a constant frequency square wave.

Sense device ($\overline{\text{SENSE}}$). This pin may optionally be used as an additional GND pin, or as an indicator to external hardware that the device is present in the system. This signal is internally connected to the GND of the die, but it is not necessary to connect it to the external ground for correct device operation. If a pull-up resistor is connected to this pin, external hardware may sense the presence of the device in a system. If the pin floats high, then the coprocessor is not installed; while the pin will be pulled low if the device is installed in the system.

Power (V_{CC} and GND). These pins provide the supply voltage and system reference level for the internal circuitry of the device. Care should be taken to reduce the noise level on these pins with appropriate capacitive decoupling.

6.7 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved source of supply listed below is for information purposes only and is current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8602101XX	2/	68881-12/BZAJC
5962-8602102XX	04713	68881-16/BZAJC
5962-8602102YX		68881-16/BYCJC
5962-8602102XX	48257	TS68881MRB/C16
5962-8602103XX	04713	68881-20/BZAJC
5962-8602103YX		68881-20/BYCJC
5962-8602103XX	48257	TS68881MRB/C20

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
2/ Inactive for new design. Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
04713	Motorola, Incorporated 5005 E. McDowell Road Phoenix, AZ 85008 Point of contact: 2100 E. Elliot Rd. Tempe, AZ 85283
48257	Thomson Electron Tubes and Devices Corporation 40 G Commerce Way Totowa, NJ 07511