512Kx8 MONOLITHIC FLASH

*PRELIMINARY**

FEATURES

- Access Times of 70, 90, 120 and 150nS
- Packaging
  - 32 Lead, Plastic J-Leaded Chip Carrier PLCC
  - 32 Lead, Plastic Thin Small Outline Package TSOP
- Standard Commercial Off-The-Shelf (COTS) Memory Devices for Extended Temperature Range
- Electrical and Speed Characteristics for:
  - Military Temperature (-55°C to +125°C)
  - Industrial Temperature (-40°C to +85°C)
- Burn-in and Temperature Cycling Available
- 10,000 Erase/Program Cycles
- Sector Erase Architecture
  - 8 equal size sectors of 64K bytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Organized as 512Kx8
- 5 Volt Programming. 5V ±10% Supply.
- Low Power CMOS, 30mA Read Current, Typical
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Page Program Operation and Internal Program Control Time.

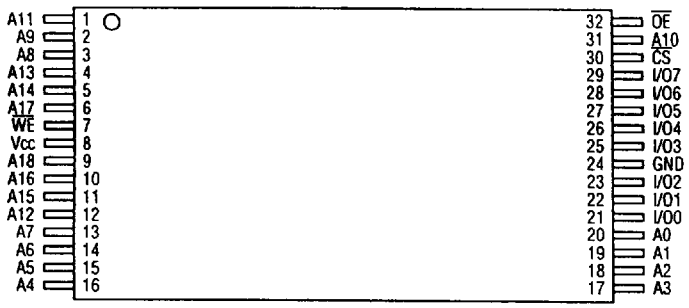
* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

Note: Programming information available upon request.

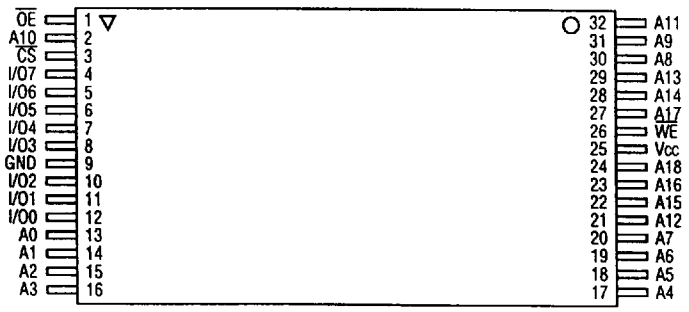
Plastic

PIN CONFIGURATIONS

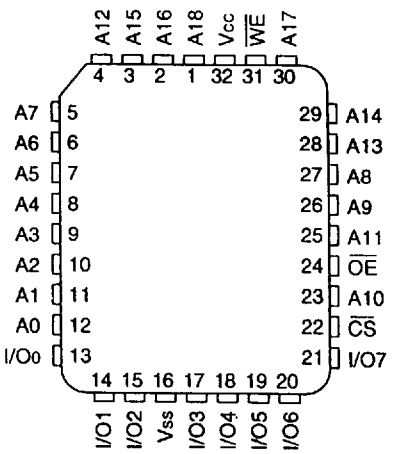
32 TSOP (STANDARD) TOP VIEW



32 TSOP (REVERSE) TOP VIEW



32 PLCC TOP VIEW



PIN DESCRIPTION

A_{0-18}	Address Inputs
I/O_{0-7}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
Vcc	+5.0V Power
Vss	Ground

ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage (V_{CC}) (1)	-2.0 to +7.0	V
Signal Voltage Range(any pin except A_9) (2)	-2.0 to +7.0	V
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10 seconds)	+300	°C
Data Retention	10 years	
Endurance (erase/program cycles)	10,000	
A_9 Voltage for sector protect (V_{ID}) (3)	-2.0 to +14.0	V

NOTES:
1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot Vss to -2.0 V for periods of up to 20nS. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods of up to 20nS.
3. Minimum DC input voltage on A_9 pin is -0.5V. During voltage transitions, A_9 may overshoot Vss to -2V for periods of up to 20nS. Maximum Dc input voltage on A_9 is +13.5V which may overshoot to 14.0 V for periods up to 20nS.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C
A_9 Volatage for Sector Protect	V_{ID}	11.5	12.5	V

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
Address Input capacitance	C_{AD}	$V_{I/O}$ = 0 V, f = 1.0 MHz	15	pF
Output Enable capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	15	pF
Write Enable capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	15	pF
Chip Select capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	15	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	15	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LOx32}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Vcc Active Current for Read (1)	I_{CC1}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz		50	mA
Vcc Active Current for Program or Erase (2)	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}		60	mA
Vcc Standby Current	I_{CC4}	V_{CC} = 5.5, $\overline{CS}$ = V_{IH}, f = 5MHz		1.6	mA
Output Low Voltage	V_{OL}	I_{OL} = 12.0 mA, V_{CC} = 4.5		0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -2.5 mA, V_{CC} = 4.5	0.85 x V_{CC}		V
Low Vcc Lock-Out Voltage	V_{LKO}		3.2	4.2	V

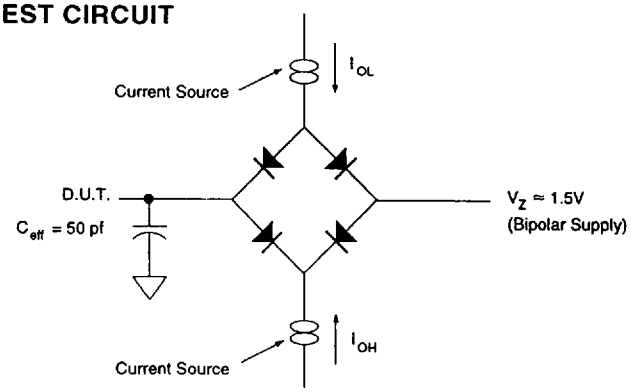
NOTES:
1. The Icc current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. Icc active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max			
Write Cycle Time	t_{AVAV}	t_{WC}	70		90		120		150		nS
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		0		nS
Chip Select Pulse Width	t_{ELEH}	t_{CP}	45		45		50		50		nS
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		0		nS
Data Setup Time	t_{DVEH}	t_{DS}	45		45		50		50		nS
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		0		nS
Address Hold Time	t_{ELAX}	t_{AH}	45		45		50		50		nS
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		20		nS
Duration of Byte Programming Operation	t_{WHWH1}		16		16		16		16		µS
Sector Erase Time	t_{WHWH2}			30		30		30		30	Sec
Read Recovery Time	t_{GHEL}		0		0		0		0		µS
Chip Programming Time				50		50		50		50	Sec
Chip Erase Time	t_{WHWH2}			120		120		120		120	Sec

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{WE}$ CONTROLLED

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	70		90		120		150		nS
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		0		nS
Write Enable Pulse Width	t_{WLWH}	t_{WP}	45		45		50		50		nS
Address Setup Time	t_{AVWH}	t_{AS}	0		0		0		0		nS
Data Setup Time	t_{DVWH}	t_{DS}	45		45		50		50		nS
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		0		nS
Address Hold Time	t_{WHAX}	t_{AH}	45		45		50		50		nS
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		20		nS
Duration of Byte Programming Operation	t_{WHWH1}		16		16		16		16		µS
Sector Erase Time	t_{WHWH2}			30		30		30		30	Sec
Read Recovery Time before Write	t_{GHWL}		0		0		0		0		µS
Vcc Set-up Time	t_{VCS}		50		50		50		50		µs
Chip Programming Time				50		50		50		50	Sec
Output Enable Setup Time		t_{OES}	0		0		0		0		nS
Output Enable Hold Time (1)		t_{OEH}	10		10		10		10		nS
Chip Erase Time	t_{WHWH2}			120		120		120		120	Sec

1. For Toggle and Data Polling.

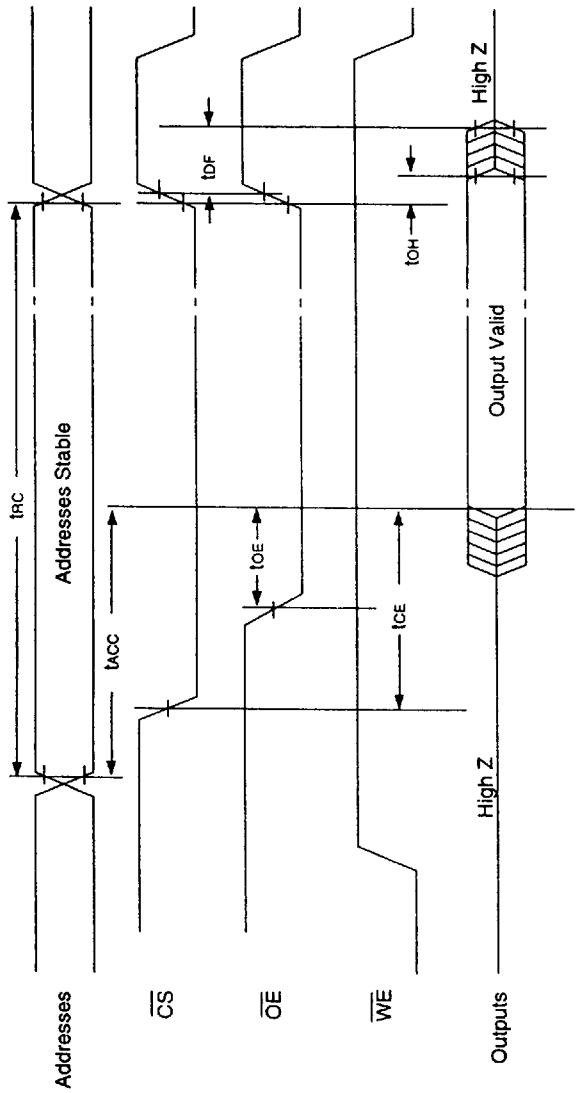
AC CHARACTERISTICS – READ ONLY OPERATIONS

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

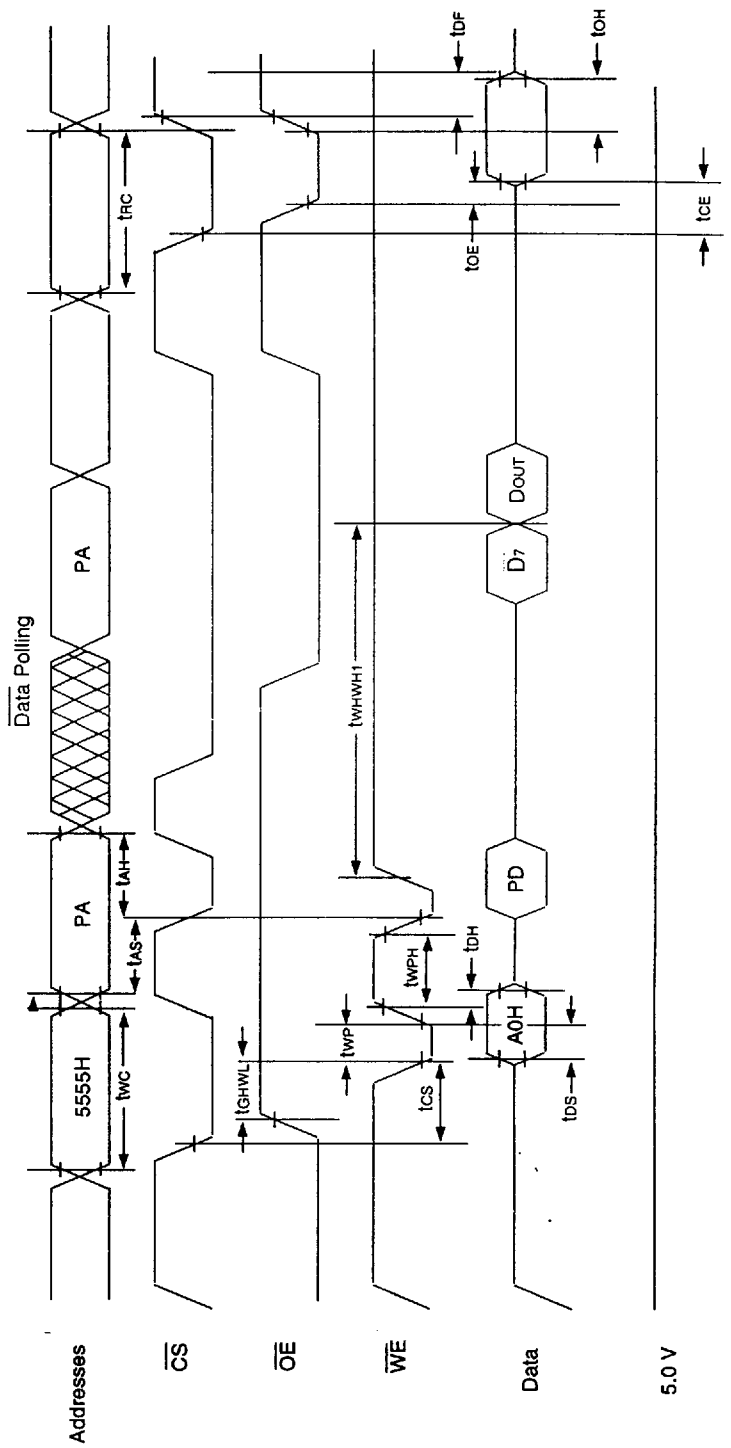
Parameter	Symbol		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	70		90		120		150		nS
Address Access Time	t_{AVQV}	t_{ACC}		70		90		120		150	nS
Chip Select Access Time	t_{ELQV}	t_{CE}		70		90		120		150	nS
Output Enable to Output Valid	t_{GLQV}	t_{OE}		35		35		50		55	nS
Chip Select to Output High Z (1)	t_{EHQZ}	t_{DF}		20		20		30		35	nS
Output Enable High to Output High Z (1)	t_{GHQZ}	t_{DF}		20		20		30		35	nS
Output Hold from Address, $\overline{CS}$ or $\overline{OE}$ Change, whichever is First	t_{AXQX}	t_{OH}	0		0		0		0		nS

1. Guaranteed by design, but not tested

AC WAVEFORMS FOR READ OPERATIONS

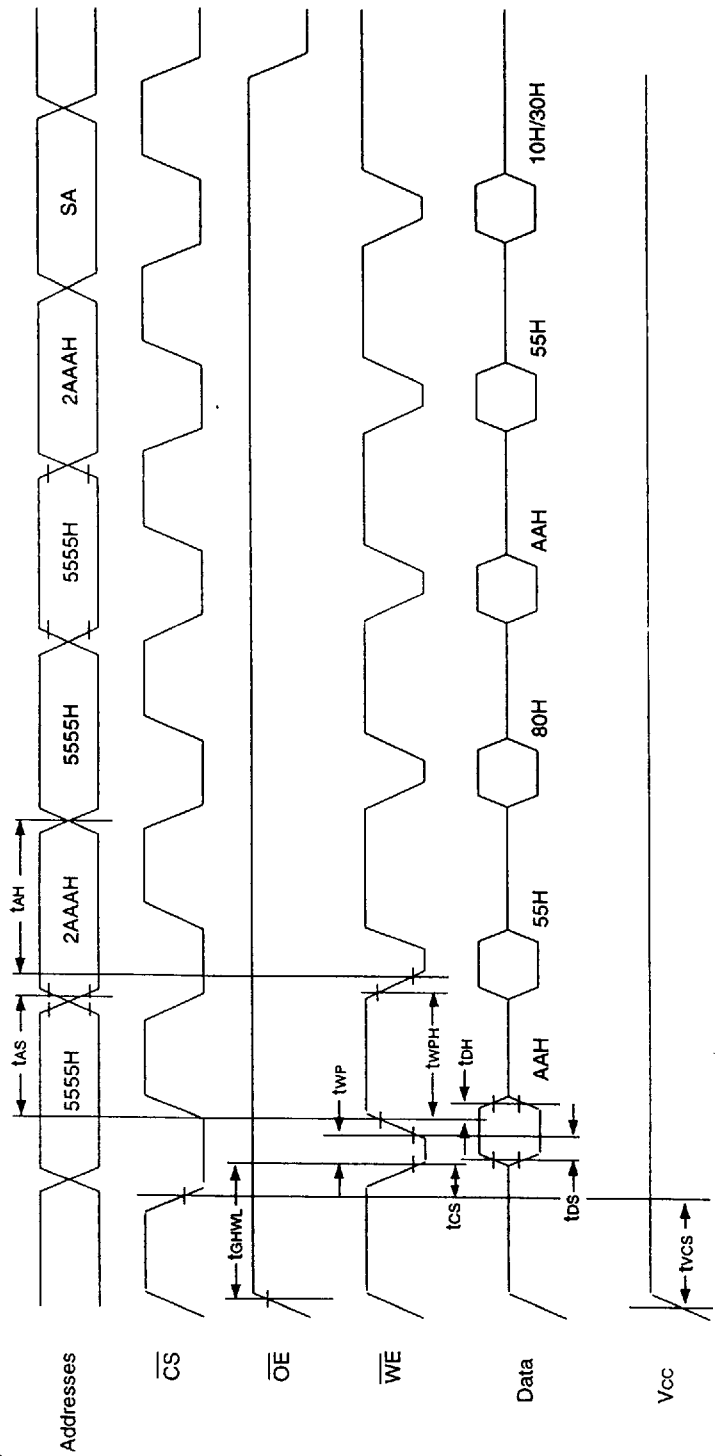


WRITE/ERASE/PROGRAM OPERATION, $\overline{WE}$ CONTROLLED



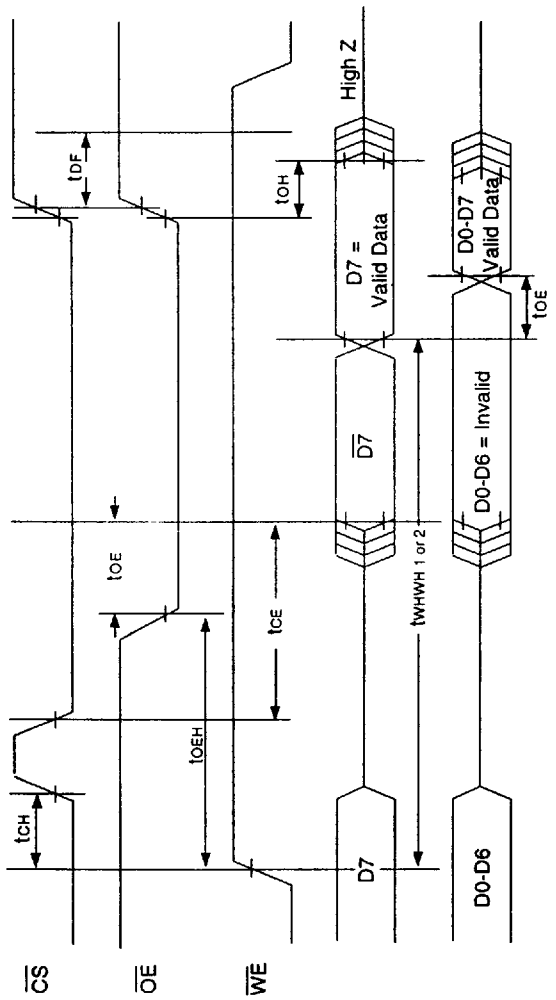
NOTES:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. $\overline{D_7}$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS

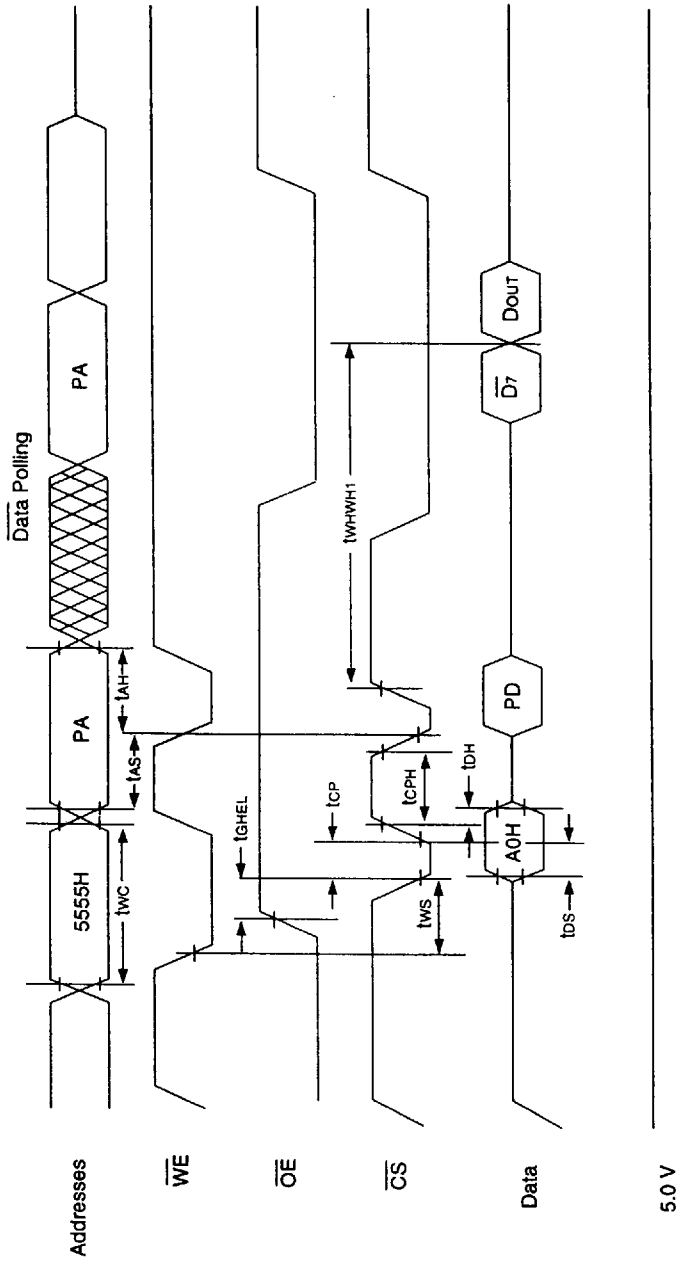


NOTE:
1. SA is the sector address for Sector Erase.

AC WAVEFORMS FOR $\overline{\text{DATA}}$ POLLING DURING EMBEDDED ALGORITHM OPERATIONS



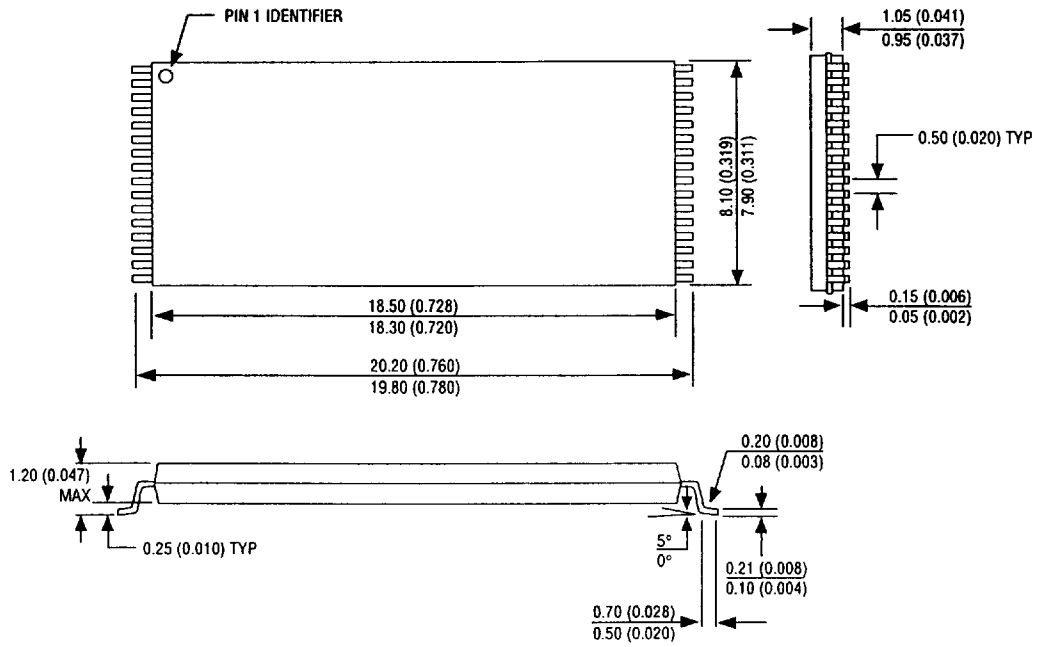
ALTERNATE $\overline{CS}$ CONTROLLED PROGRAMMING OPERATION TIMINGS



NOTES:

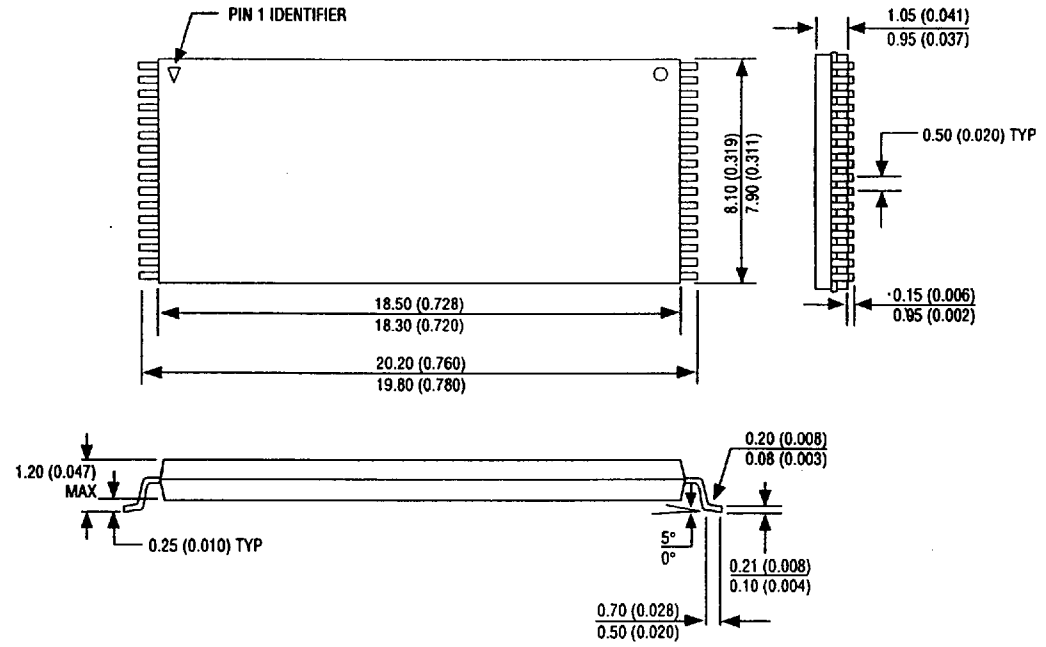
1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

32 LEAD, STANDARD PLASTIC TSOP PACKAGE DIMENSION



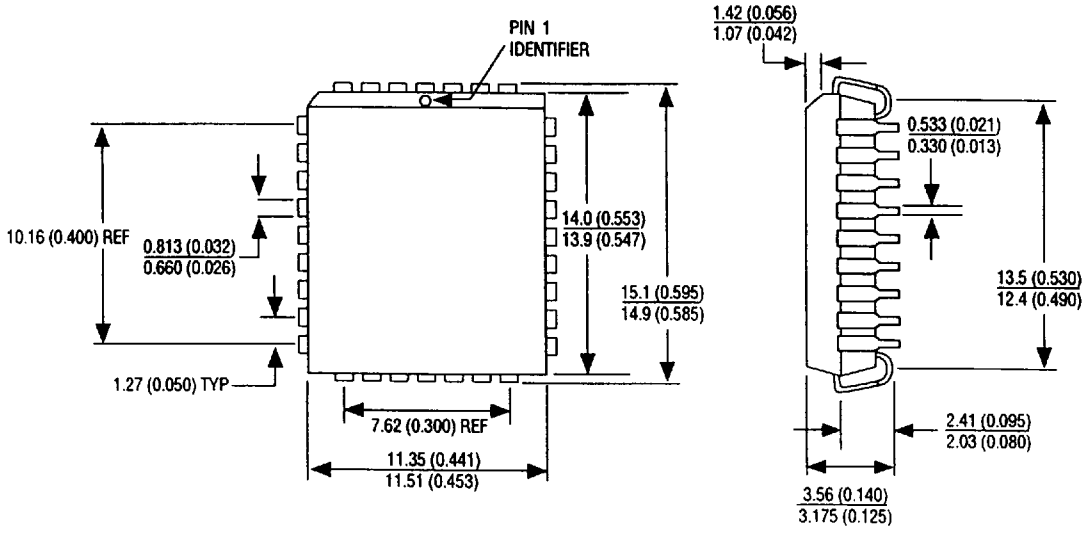
DIMENSIONS IN MILLIMETERS AND (INCHES)

32 LEAD, REVERSED PLASTIC TSOP PACKAGE DIMENSION



DIMENSIONS IN MILLIMETERS AND (INCHES)

32 LEAD, PLASTIC J-LEADED PLCC PACKAGE DIMENSION



DIMENSIONS IN MILLIMETERS AND (INCHES)

ORDERING INFORMATION

W P F 512K 8 X - XXX X X

DEVICE GRADE:
- M = Military Temperature -55°C to +125°C
- I = Industrial Temperature -40°C to +85°C

PACKAGE:
- TF = 32 lead Plastic TSOP
- TR = 32 lead Plastic TSOP Reverse
- PL = 32 lead Plastic LCC (J-lead)

ACCESS TIME in nS

IMPROVEMENT MARK
- B = Burn-in
- T = Temperature Cycle
- C = Burn-in and Temp Cycle

ORGANIZATION, 512K x 8

FLASH

PLASTIC PLUS™

WHITE MICROELECTRONICS