128Kx32 EEPROM MODULE, SMD 5962-94585

FEATURES

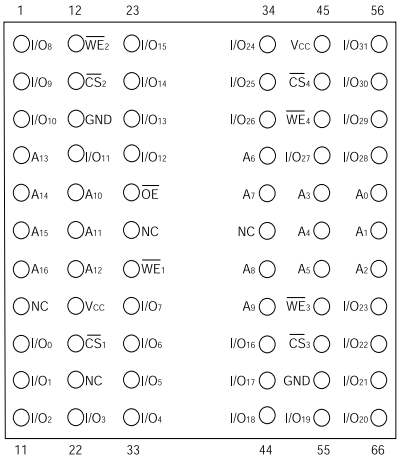
- Access Times of 120*, 140, 150, 200, 250, 300ns
- Packaging:
  - 66-pin, PGA Type, 27.3mm (1.075") square, Hermetic Ceramic HIP (Package 400)
  - 68 lead, 22.4mm sq. CQFP (G2T)[1], 4.57mm (0.180") high, (Package 509)
  - 68 lead, 23.9mm sq. Low Profile CQFP (G1U), 3.57mm (0.140") high, (Package 519)
  - 68 lead, 23.9mm sq. Low Profile CQFP (G1T), 4.06mm (0.160") high, (Package 524)
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Write Endurance 10,000 Cycles
- Data Retention Ten Years Minimum (at +25°C)
- Commercial, Industrial and Military Temperature Ranges
- Low Power CMOS
- Automatic Page Write Operation
- Page Write Cycle Time: 10ms Max
- Data Polling for End of Write Detection
- Hardware and Software Data Protection
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  WE128K32-XG2TX[1] - 8 grams typical
  WE128K32-XG1UX - 5 grams typical
  WE128K32-XG1TX - 5 grams typical
  WE128K32-XH1X - 13 grams typical

** 120ns not available for SMD product*

Note 1: Package Not Recommended For New Design

FIG. 1 PIN CONFIGURATION FOR WE128K32N-XH1X

TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
WE1-4	Write Enables
CS1-4	Chip Selects
OE	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

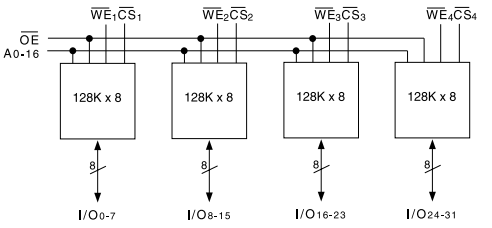
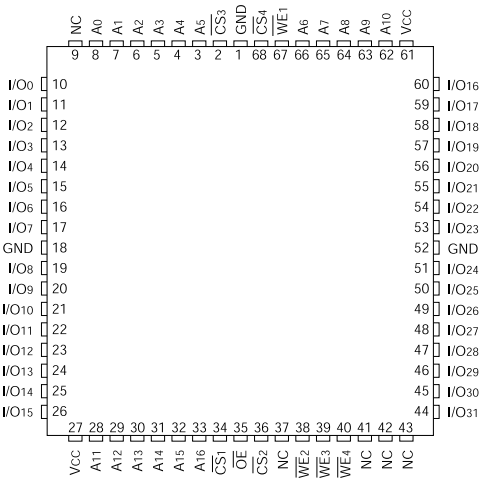
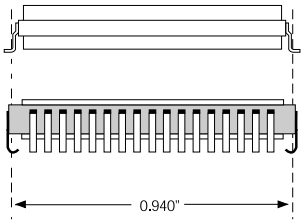


FIG. 3 PIN CONFIGURATION FOR WE128K32-XG2TX[1], WE128K32-XG1UX AND WE128K32-XG1TX

TOP VIEW



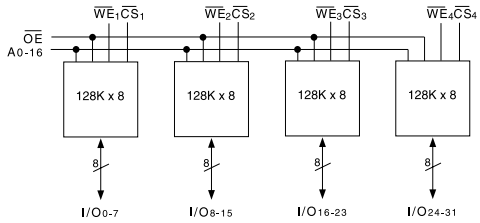


The White 68 lead CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But it has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



Note 1: Package Not Recommended For New Design

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol		Unit
Operating Temperature	T_A	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Signal Voltage Relative to GND	V_G	-0.6 to +6.25	V
Voltage on $\overline{OE}$ and A9		-0.6 to +13.5	V

NOTE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O
H	X	X	Standby	High Z
L	L	H	Read	Data Out
L	H	L	Write	Data In
X	H	X	Out Disable	High Z/Data Out
X	X	H	Write	
X	L	X	Inhibit	

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}_{1-4}$ capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz		pF
HIP (PGA)			20	
CQFP G2T/G1U/G1T			20	
$\overline{CS}_{1-4}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

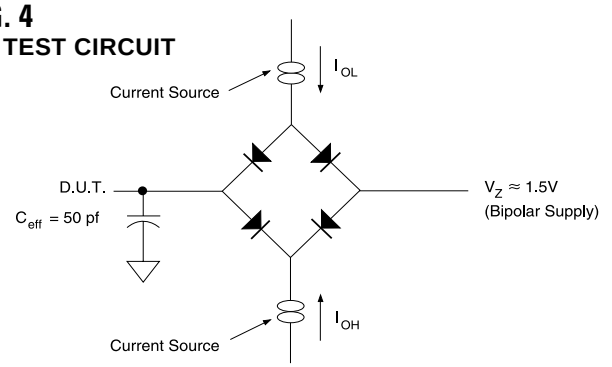
DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LOx32}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current x 32 Mode	I_{CCx32}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz		250	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz		2.5	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA, V_{CC} = 4.5V		0.45	V
Output High Voltage	V_{OH}	I_{OH} = -400µA, V_{CC} = 4.5V	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

FIG. 4
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

WRITE

A write cycle is initiated when $\overline{OE}$ is high and a low pulse is on $\overline{WE}$ or $\overline{CS}$ with $\overline{CS}$ or $\overline{WE}$ low. The address is latched on the falling edge of $\overline{CS}$ or $\overline{WE}$ whichever occurs last. The data is latched by the rising edge of $\overline{CS}$ or $\overline{WE}$, whichever occurs first. A byte write operation will automatically continue to completion.

WRITE CYCLE TIMING

Figures 5 and 6 show the write cycle timing relationships. A write cycle begins with address application, write enable and chip select. Chip select is accomplished by placing the $\overline{CS}$ line low. Write enable consists of setting the $\overline{WE}$ line low. The write cycle begins when the last of either $\overline{CS}$ or $\overline{WE}$ goes low.

The $\overline{WE}$ line transition from high to low also initiates an internal 150 µsec delay timer to permit page mode operation. Each subsequent $\overline{WE}$ transition from high to low that occurs before the completion of the 150 µsec time out will restart the timer from zero. The operation of the timer is the same as a retriggerable one-shot.

AC WRITE CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Write Cycle Parameter	Symbol	Min	Max	Unit
Write Cycle Time, TYP = 6ms	t_{WC}		10	ms
Address Set-up Time	t_{AS}	0		ns
Write Pulse Width ($\overline{WE}$ or $\overline{CS}$)	t_{WP}	150		ns
Chip Select Set-up Time	t_{CS}	0		ns
Address Hold Time	t_{AH}	100		ns
Data Hold Time	t_{DH}	10		ns
Chip Select Hold Time	t_{CSH}	0		ns
Data Set-up Time	t_{DS}	100		ns
Output Enable Set-up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns
Write Pulse Width High	t_{WPH}	50		ns

FIG. 5
WRITE WAVEFORMS
$\overline{WE}$ CONTROLLED

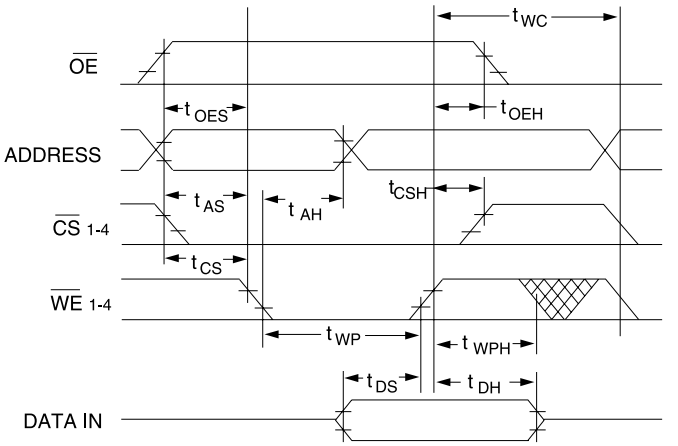
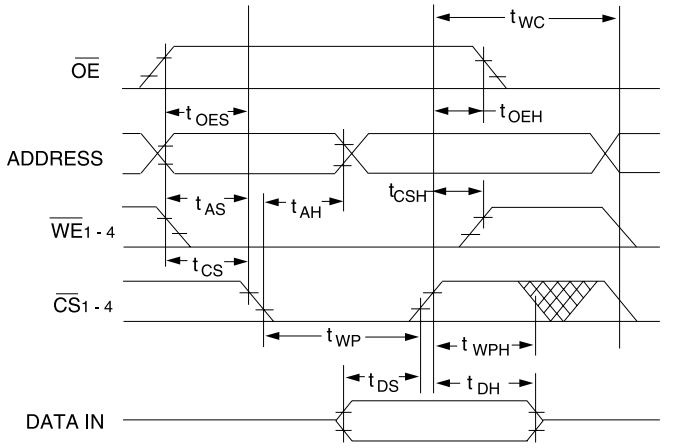


FIG. 6
WRITE WAVEFORMS
$\overline{CS}$ CONTROLLED



READ

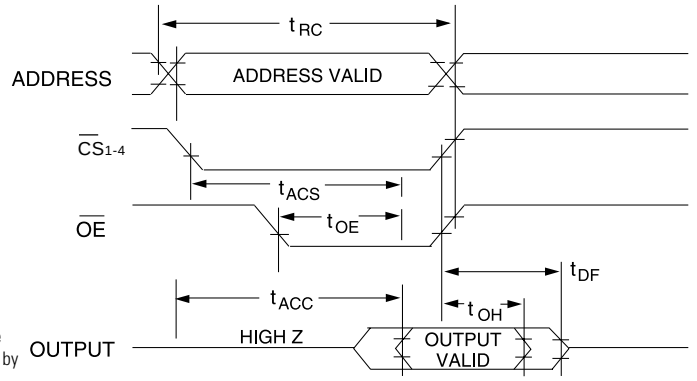
The WE128K32-XXX stores data at the memory location determined by the address pins. When $\overline{CS}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, this data is present on the outputs. When $\overline{CS}$ and $\overline{OE}$ are high, the outputs are in a high impedance state. This two line control prevents bus contention.

AC READ CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Read Cycle Parameter	Symbol	-120		-140		-150		-200		-250		-300		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		140		150		200		250		300		ns
Address Access Time	t_{ACC}		120		140		150		200		250		300	ns
Chip Select Access Time	t_{ACS}		120		140		150		200		250		300	ns
Output Hold from Add. Change, $\overline{OE}$ or $\overline{CS}$	t_{OH}	0		0		0		0		0		0		ns
Output Enable to Output Valid	t_{OE}	0	50	0	55	0	55	0	55	0	85	0	85	ns
Chip Select or $\overline{OE}$ to High Z Output	t_{DF}		70		70		70		70		70		70	ns

FIG. 7
READ WAVEFORMS



NOTES:
$\overline{OE}$ may be delayed up to t_{ACS} - t_{OE} after the falling edge of $\overline{CS}$ without impact on t_{OE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.

DATA POLLING

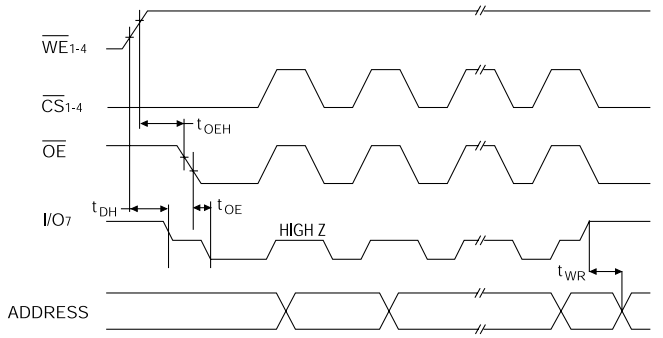
The WE128K32-XXX offers a data polling feature which allows a faster method of writing to the device. Figure 8 shows the timing diagram for this function. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data on D_7 (for each chip.) Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. Data polling may begin at any time during the write cycle.

DATA POLLING CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Min	Max	Unit
Data Hold Time	t_{DH}	10		ns
$\overline{OE}$ Hold Time	t_{OEH}	10		ns
$\overline{OE}$ To Output Valid	t_{OE}		55	ns
Write Recovery Time	t_{WR}	0		ns

FIG. 8
DATA POLLING WAVEFORMS



PAGE WRITE OPERATION

The WE128K32-XXX has a page write operation that allows one to 128 bytes of data to be written into the device and consecutively loads during the internal programming period. Successive bytes may be loaded in the same manner after the first data byte has been loaded. An internal timer begins a time out operation at each write cycle. If another write cycle is completed within 150µs or less, a new time out period begins. Each write cycle restarts the delay period. The write cycles can be continued as long as the interval is less than the time out period.

The usual procedure is to increment the least significant address lines from A0 through A6 at each write cycle. In this manner a page of up to 128 bytes can be loaded in to the EEPROM in a burst mode before beginning the relatively long interval programming cycle.

After the 150µs time out is completed, the EEPROM begins an internal write cycle. During this cycle the entire page of bytes will be written at the same time. The internal programming cycle is the same regardless of the number of bytes accessed.

PAGE WRITE CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Page Mode Write Characteristics	Symbol			Unit
Parameter		**Min**	**Max**	
Write Cycle Time, TYP = 6ms	t_{WC}		10	ms
Address Set-up Time	t_{AS}	0		ns
Address Hold Time (1)	t_{AH}	100		ns
Data Set-up Time	t_{DS}	100		ns
Data Hold Time	t_{DH}	10		ns
Write Pulse Width	t_{WP}	150		ns
Byte Load Cycle Time	t_{BLC}		150	µs
Write Pulse Width High	t_{WPH}	50		ns

1. Page address must remain valid for duration of write cycle.

FIG. 9
PAGE MODE WRITE WAVEFORMS

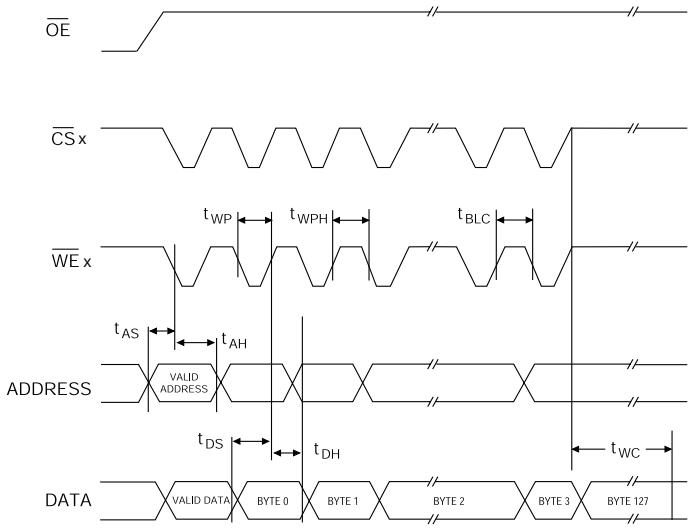
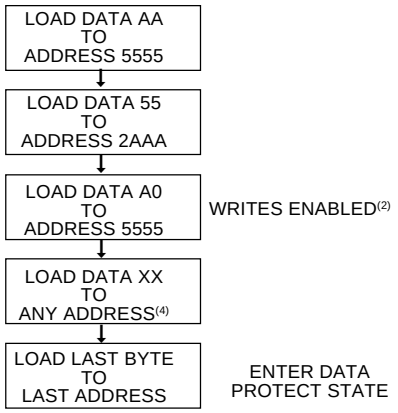
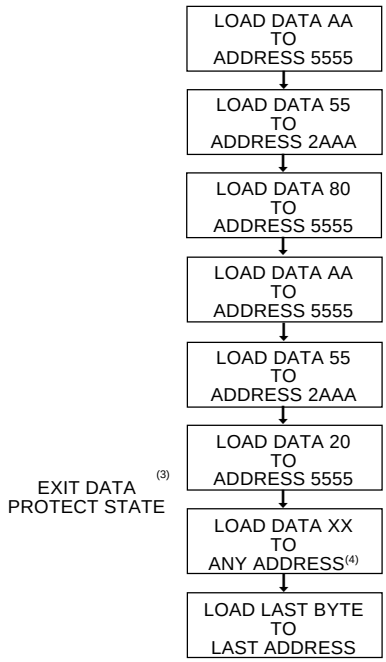


FIG. 10
SOFTWARE DATA PROTECTION ENABLE ALGORITHM(1)



NOTES:
1. Data Format: D_7 - D_0 (Hex);
   Address Format: A_{16} - A_0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data may be loaded.

FIG. 11
SOFTWARE DATA PROTECTION DISABLE ALGORITHM(1)



NOTES:
1. Data Format: D_7 - D_0 (Hex);
   Address Format: A_{16} - A_0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data may be loaded.

SOFTWARE DATA PROTECTION

A software write protection feature may be enabled or disabled by the user. When shipped by White Microelectronics, the WE-128K32-XXX has the feature disabled. Write access to the device is unrestricted.

To enable software write protection, the user writes three access code bytes to three special internal locations. Once write protection has been enabled, each write to the EEPROM must use the same three byte write sequence to permit writing. After setting software data protection, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device, however, for the duration of t_{WC}. The write protection feature can be disabled by a six byte write sequence of specific data to specific locations. Power transitions will not reset the software write protection.

Each 128K byte block of the EEPROM has independent write protection. One or more blocks may be enabled and the rest disabled in any combination. The software write protection guards against inadvertent writes during power transitions, or unauthorized modification using a PROM programmer.

HARDWARE DATA PROTECTION

These features protect against inadvertent writes to the WE128K32-XXX. These are included to improve reliability during normal operation:

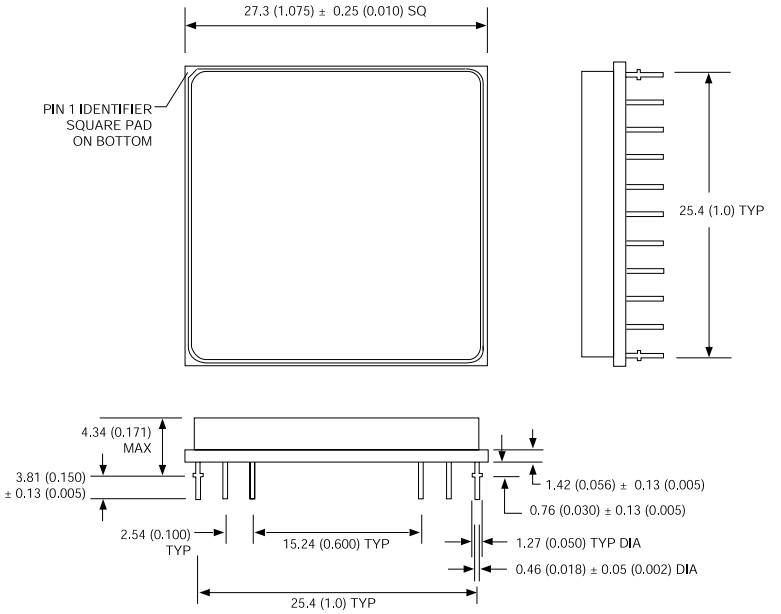
a) V_{CC} power on delay
As V_{CC} climbs past 3.8V typical the device will wait 5msec typical before allowing write cycles.

b) V_{CC} sense
While below 3.8V typical write cycles are inhibited.

c) Write inhibiting
Holding $\overline{OE}$ low and either $\overline{CS}$ or $\overline{WE}$ high inhibits write cycles.

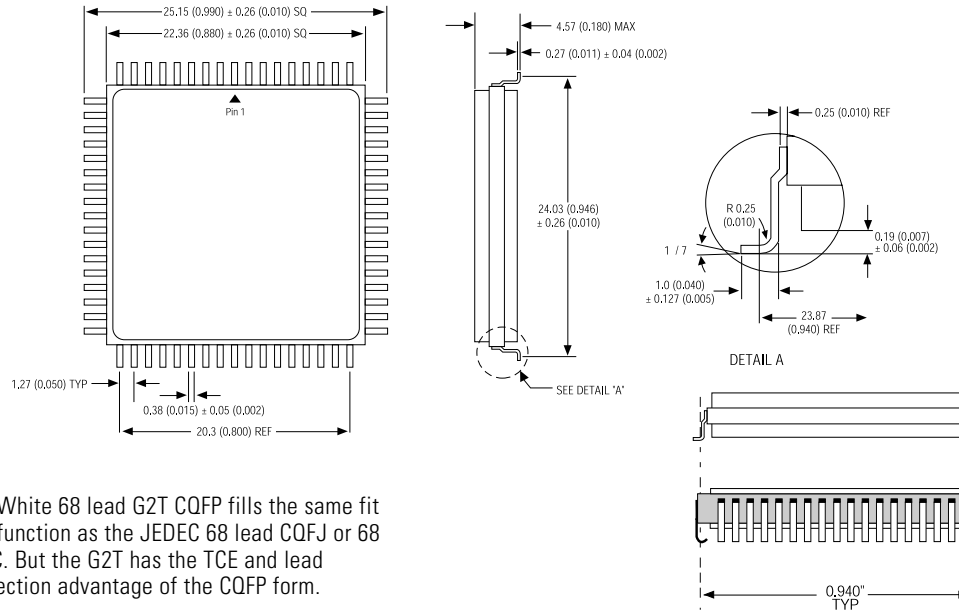
d) Noise filter
Pulses of <8ns (typ) on $\overline{WE}$ or $\overline{CS}$ will not initiate a write cycle.

PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 509: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2T)[1]

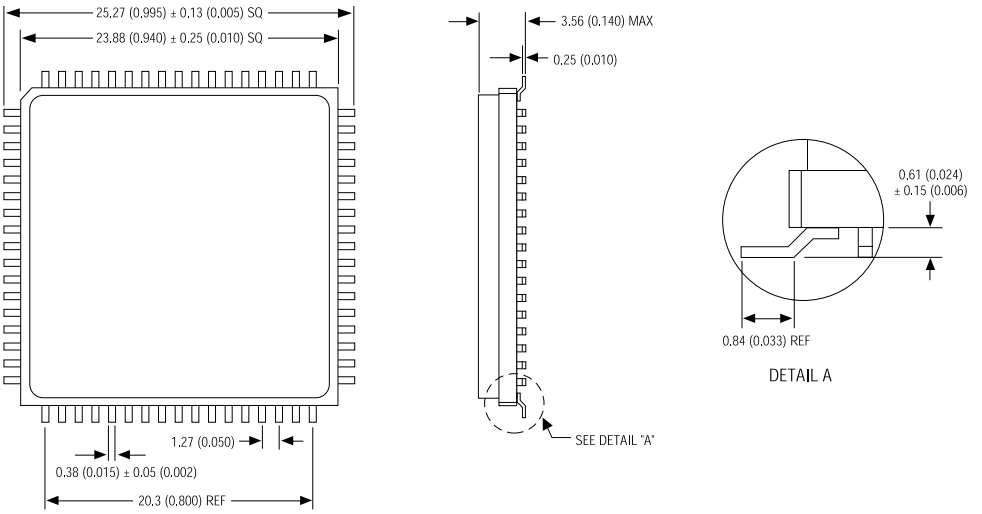


The White 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

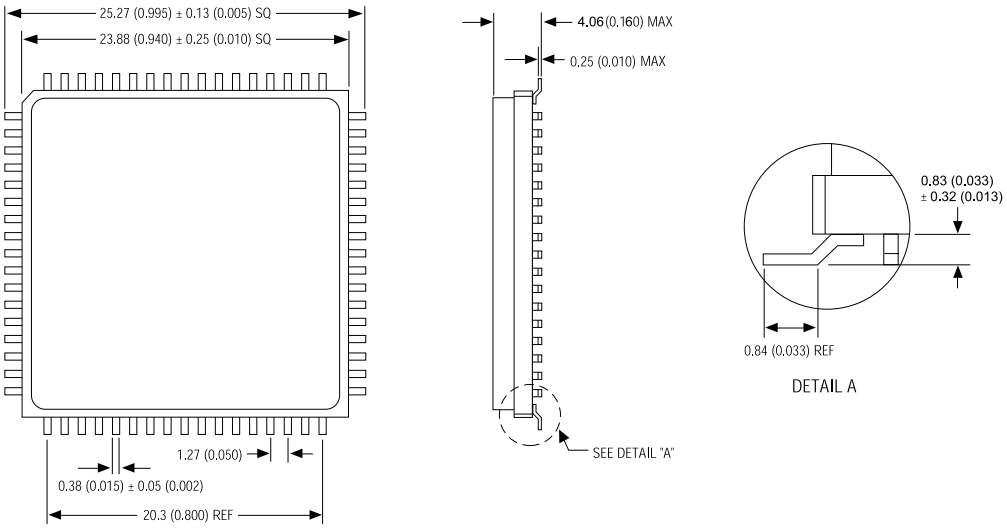
Note 1: Package Not Recommended For New Design

PACKAGE 519: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G1U)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 524: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G1T)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

FIG. 12 ALTERNATE PIN CONFIGURATION FOR WE128K32NP-XH1X

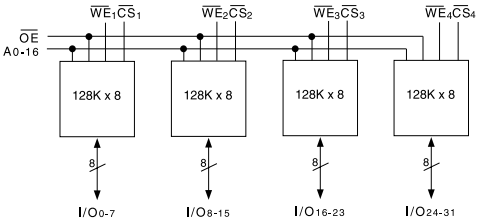
TOP VIEW

1	12	23	34	45	56
I/O8	$\overline{WE}_2$	I/O15	I/O24	VCC	I/O31
I/O9	$\overline{CS}_2$	I/O14	I/O25	$\overline{CS}_4$	I/O30
I/O10	GND	I/O13	I/O26	$\overline{WE}_4$	I/O29
A14	I/O11	I/O12	A7	I/O27	I/O28
A16	A10	$\overline{OE}$	A12	A4	A1
A11	A9	NC	NC	A5	A2
A0	A15	$\overline{WE}_1$	A13	A6	A3
NC	VCC	I/O7	A8	$\overline{WE}_3$	I/O23
I/O0	$\overline{CS}_1$	I/O6	I/O16	$\overline{CS}_3$	I/O22
I/O1	NC	I/O5	I/O17	GND	I/O21
I/O2	I/O3	I/O4	I/O18	I/O19	I/O20
11	22	33	44	55	66

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



ORDERING INFORMATION

W E 128K32 X - XXX X X X

LEAD FINISH:
Blank = Gold plated leads
A = Solder dip leads

DEVICE GRADE:
Q = Compliant
M = Military Screened -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C

PACKAGE TYPE:
H1 = 1.075" sq. Ceramic Hex In-line Package, HIP (Package 400*)
G2T[1] = 22.4mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 509)
G1U = 23.9mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 519)
G1T = 23.9mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 524)

ACCESS TIME (ns)

IMPROVEMENT MARK
N = No Connect at pins 8, 21, 28, and 39 in HIP for upgrade
P = Alternate Pin Configuration for HIP package

ORGANIZATION 128K x 32
User Configurable as 256K x 16 or 512K x 8

EEPROM

WHITE ELECTRONIC DESIGNS CORP.

Note 1: Package Not Recommended For New Design

DEVICE TYPE	SPEED	PACKAGE	SMD NO.
128K x 32 EEPROM Module	300ns	66 pin HIP (H1)	5962-94585 01H5X
128K x 32 EEPROM Module	250ns	66 pin HIP (H1)	5962-94585 02H5X
128K x 32 EEPROM Module	200ns	66 pin HIP (H1)	5962-94585 03H5X
128K x 32 EEPROM Module	150ns	66 pin HIP (H1)	5962-94585 04H5X
128K x 32 EEPROM Module	140ns	66 pin HIP (H1)	5962-94585 05H5X
128K x 32 EEPROM Module	300ns	66 pin HIP (H1, P type pinout)	5962-94585 01H6X
128K x 32 EEPROM Module	250ns	66 pin HIP (H1, P type pinout)	5962-94585 02H6X
128K x 32 EEPROM Module	200ns	66 pin HIP (H1, P type pinout)	5962-94585 03H6X
128K x 32 EEPROM Module	150ns	66 pin HIP (H1, P type pinout)	5962-94585 04H6X
128K x 32 EEPROM Module	140ns	66 pin HIP (H1, P type pinout)	5962-94585 05H6X
128K x 32 EEPROM Module	300ns	68 lead CQFP/J (G2T)[1]	5962-94585 01HMX[1]
128K x 32 EEPROM Module	250ns	68 lead CQFP/J (G2T)[1]	5962-94585 02HMX[1]
128K x 32 EEPROM Module	200ns	68 lead CQFP/J (G2T)[1]	5962-94585 03HMX[1]
128K x 32 EEPROM Module	150ns	68 lead CQFP/J (G2T)[1]	5962-94585 04HMX[1]
128K x 32 EEPROM Module	140ns	68 lead CQFP/J (G2T)[1]	5962-94585 05HMX[1]
128K x 32 EEPROM Module	300ns	68 lead CQFP (G1U)	5962-94585 01H9X
128K x 32 EEPROM Module	250ns	68 lead CQFP (G1U)	5962-94585 02H9X
128K x 32 EEPROM Module	200ns	68 lead CQFP (G1U)	5962-94585 03H9X
128K x 32 EEPROM Module	150ns	68 lead CQFP (G1U)	5962-94585 04H9X
128K x 32 EEPROM Module	140ns	68 lead CQFP (G1U)	5962-94585 05H9X