

# **PDC16RV7244C-(102/103)T-S**

## **128MByte (16M x 72) CMOS, PC/100**

### **Synchronous DRAM Module - ECC (Registered)**

#### **General Description**

The PDC16RV7244C-(102/103)T-S is a high performance, 128-megabyte synchronous, dynamic RAM module organized as 16M words by 72 bits, in a 168-pin, dual-in-line memory module (DIMM) package.

The module utilizes eighteen Fujitsu MB81F64442C-(102/103)FN CMOS 16Mx4 synchronous dynamic RAMs in surface mount package (TSOP) on an epoxy laminated substrate. Each device is accompanied by a decoupling capacitor for improved noise immunity.

A 256 Byte Serial EEPROM contains the module configuration information.

#### **Features**

- High Density 128MByte
- Cycle Time: 10ns
- Low Power: Active 15.7W
- LVTTTL-compatible inputs and outputs
- Separate power and ground planes to improve noise immunity
- Single power supply of 3.3V±0.3V
- Height: 1.700 inch

#### **ABSOLUTE MAXIMUM RATINGS**

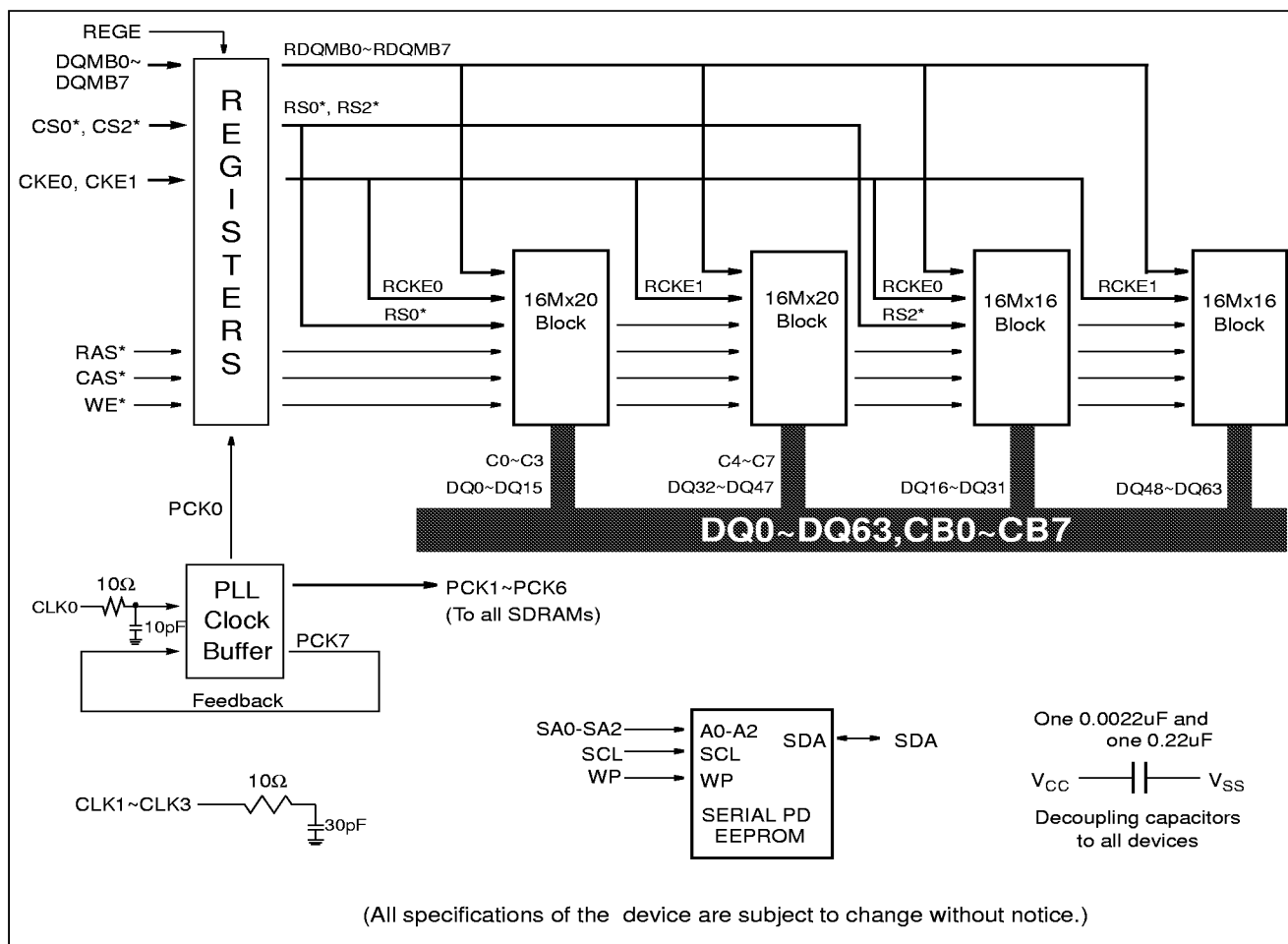
| Item                                           | Symbol           | Ratings      | Unit |
|------------------------------------------------|------------------|--------------|------|
| Voltage on any pin relative to V <sub>SS</sub> | V <sub>T</sub>   | -0.5 to +4.6 | V    |
| Power Dissipation                              | P <sub>T</sub>   | 18.0         | W    |
| Operating Temperature                          | T <sub>opr</sub> | 0 to +70     | °C   |
| Storage Temperature                            | T <sub>stg</sub> | -55 to +125  | °C   |
| Short Circuit Output Current                   | I <sub>OS</sub>  | ±50          | mA   |

#### **RECOMMENDED DC OPERATING CONDITIONS**

(T<sub>A</sub> = 0 to +70 °C)

| Symbol          | Parameter          | Min  | Typ | Max                  | Unit |
|-----------------|--------------------|------|-----|----------------------|------|
| V <sub>CC</sub> | Supply Voltage     | 3.0  | 3.3 | 3.6                  | V    |
| V <sub>SS</sub> | Ground             | 0    | 0   | 0                    | V    |
| V <sub>IH</sub> | Input High voltage | 2.0  | -   | V <sub>CC</sub> +0.5 | V    |
| V <sub>IL</sub> | Input Low voltage  | -0.5 | -   | 0.8                  | V    |

### Functional Diagram



- Notes:
1. A0~A11 and BA0 to all SDRAMs through registers.
  2. BA1 to all SDRAMs through registers.
  3. Register Block comprises of two registers.
  4. Data is terminated using 10Ω series resistors.
  5. REGE, when asserted active high the buffer-register operates in register mode, when deasserted inactive low the buffer-register operates in "real time" buffer mode.
  6. CLK signals are terminated with series resistors and / or padding capacitors depending on load per clock.
  7. Each 16Mx16 Block comprises of four 16Mx4 SDRAMs and each 16Mx20 Block comprises of five 16Mx4 SDRAMs.
  8. WP signal has a pull-down of 47 KΩ.
  9. RDQMs vs. Data I/Os

RDQMB0 controls DQ0~DQ7  
RDQMB1 controls DQ8~DQ15, CB0~CB3  
RDQMB2 controls DQ16~DQ23  
RDQMB3 controls DQ24~DQ31  
RDQMB4 controls DQ32~DQ39  
RDQMB5 controls DQ40~DQ47, CB4~CB7  
RDQMB6 controls DQ48~DQ55  
RDQMB7 controls DQ56~DQ63

# **PDC16RV7244C-(102/103)T-S**

## **Pin Name**

|                 |                        |                 |                          |
|-----------------|------------------------|-----------------|--------------------------|
| A0~A11          | Addresses              | CS0*, CS2*      | Chip Select              |
| BA0, BA1        | Bank Select Address    | WE*             | Write Enable             |
| DQ0~DQ63, C0~C7 | Data Inputs/Outputs    | SA0~SA2         | Decode Input             |
| CLK0~CLK3       | Clock Inputs           | SCL             | Serial Clock             |
| RAS*            | Row Address Strokes    | SDA             | Serial Data Input/Output |
| CAS*            | Column Address Strokes | WP              | Write Protect            |
| CKE0, CKE1      | Clock Enables          | V <sub>CC</sub> | Power Supply             |
| DQMB0-DQMB7     | DQ Mask Enables        | V <sub>SS</sub> | Ground                   |
| REGE            | Register enable        | NC              | No Connection            |

| Pin No. | Pin Designation | Pin No. | Pin Designation | Pin No. | Pin Designation | Pin No. | Pin Designation |
|---------|-----------------|---------|-----------------|---------|-----------------|---------|-----------------|
| 1       | V <sub>SS</sub> | 43      | V <sub>SS</sub> | 85      | V <sub>SS</sub> | 127     | V <sub>SS</sub> |
| 2       | DQ0             | 44      | NC              | 86      | DQ32            | 128     | CKE0            |
| 3       | DQ1             | 45      | CS2*            | 87      | DQ33            | 129     | NC              |
| 4       | DQ2             | 46      | DQMB2           | 88      | DQ34            | 130     | DQMB6           |
| 5       | DQ3             | 47      | DQMB3           | 89      | DQ35            | 131     | DQMB7           |
| 6       | V <sub>CC</sub> | 48      | NC              | 90      | V <sub>CC</sub> | 132     | NC              |
| 7       | DQ4             | 49      | V <sub>CC</sub> | 91      | DQ36            | 133     | V <sub>CC</sub> |
| 8       | DQ5             | 50      | NC              | 92      | DQ37            | 134     | NC              |
| 9       | DQ6             | 51      | NC              | 93      | DQ38            | 135     | NC              |
| 10      | DQ7             | 52      | C2              | 94      | DQ39            | 136     | C6              |
| 11      | DQ8             | 53      | C3              | 95      | DQ40            | 137     | C7              |
| 12      | V <sub>SS</sub> | 54      | V <sub>SS</sub> | 96      | V <sub>SS</sub> | 138     | V <sub>SS</sub> |
| 13      | DQ9             | 55      | DQ16            | 97      | DQ41            | 139     | DQ48            |
| 14      | DQ10            | 56      | DQ17            | 98      | DQ42            | 140     | DQ49            |
| 15      | DQ11            | 57      | DQ18            | 99      | DQ43            | 141     | DQ50            |
| 16      | DQ12            | 58      | DQ19            | 100     | DQ44            | 142     | DQ51            |
| 17      | DQ13            | 59      | V <sub>CC</sub> | 101     | DQ45            | 143     | V <sub>CC</sub> |
| 18      | V <sub>CC</sub> | 60      | DQ20            | 102     | V <sub>CC</sub> | 144     | DQ52            |
| 19      | DQ14            | 61      | NC              | 103     | DQ46            | 145     | NC              |
| 20      | DQ15            | 62      | NC              | 104     | DQ47            | 146     | NC              |
| 21      | C0              | 63      | CKE1            | 105     | C4              | 147     | REGE            |
| 22      | C1              | 64      | V <sub>SS</sub> | 106     | C5              | 148     | V <sub>SS</sub> |
| 23      | V <sub>SS</sub> | 65      | DQ21            | 107     | V <sub>SS</sub> | 149     | DQ53            |
| 24      | NC              | 66      | DQ22            | 108     | NC              | 150     | DQ54            |
| 25      | NC              | 67      | DQ23            | 109     | NC              | 151     | DQ55            |
| 26      | V <sub>CC</sub> | 68      | V <sub>SS</sub> | 110     | V <sub>CC</sub> | 152     | V <sub>SS</sub> |
| 27      | WE*             | 69      | DQ24            | 111     | CAS*            | 153     | DQ56            |
| 28      | DQMB0           | 70      | DQ25            | 112     | DQMB4           | 154     | DQ57            |
| 29      | DQMB1           | 71      | DQ26            | 113     | DQMB5           | 155     | DQ58            |
| 30      | CS0*            | 72      | DQ27            | 114     | NC              | 156     | DQ59            |
| 31      | NC              | 73      | V <sub>CC</sub> | 115     | RAS*            | 157     | V <sub>CC</sub> |
| 32      | V <sub>SS</sub> | 74      | DQ28            | 116     | V <sub>SS</sub> | 158     | DQ60            |
| 33      | A0              | 75      | DQ29            | 117     | A1              | 159     | DQ61            |
| 34      | A2              | 76      | DQ30            | 118     | A3              | 160     | DQ62            |
| 35      | A4              | 77      | DQ31            | 119     | A5              | 161     | DQ63            |
| 36      | A6              | 78      | V <sub>SS</sub> | 120     | A7              | 162     | V <sub>SS</sub> |
| 37      | A8              | 79      | CLK2            | 121     | A9              | 163     | CLK3            |
| 38      | A10 / AP (Note) | 80      | NC              | 122     | BA0 (Note)      | 164     | NC              |
| 39      | BA1 (Note)      | 81      | WP              | 123     | A11             | 165     | SA0             |
| 40      | V <sub>CC</sub> | 82      | SDA             | 124     | V <sub>CC</sub> | 166     | SA1             |
| 41      | V <sub>CC</sub> | 83      | SCL             | 125     | CLK1            | 167     | SA2             |
| 42      | CLK0            | 84      | V <sub>CC</sub> | 126     | NC              | 168     | V <sub>CC</sub> |

Note : 1. Address A10 / AP : Initiates Auto Precharge  
2. Address BA0,BA1 : Bank select within the SDRAM devices

**SERIAL PD INFORMATION**

| Byte# | Function Described                                            | Function Supported             |      | Hex Value         |      |
|-------|---------------------------------------------------------------|--------------------------------|------|-------------------|------|
|       |                                                               | -102                           | -103 | -102              | -103 |
| 0     | # Bytes Written into serial memory at module mfr              | 128 bytes                      |      | 80h               |      |
| 1     | Total # bytes of SPD memory device                            | 256 bytes                      |      | 08h               |      |
| 2     | Fundamental memory type                                       | SDRAM                          |      | 04h               |      |
| 3     | # Row Address on this assembly                                | 12                             |      | 0Ch               |      |
| 4     | # Column Addresses on this assembly                           | 10                             |      | 0Ah               |      |
| 5     | # Module Banks on this assembly                               | 1                              |      | 01h               |      |
| 6     | Data Width of this assembly                                   | 72 bits                        |      | 48h               |      |
| 7     | Data Width of this assembly (continued)                       |                                |      | 00h               |      |
| 8     | Voltage interface standard of this assembly                   | LVTTL                          |      | 01h               |      |
| 9     | SDRAM cycle time at CL=3 (tCLK)                               | 10ns                           |      | A0h               |      |
| 10    | SDRAM Access from Clock at CL=3 (tAC)                         | 6ns                            |      | 60h               |      |
| 11    | DIMM configuration type                                       | ECC                            |      | 02h               |      |
| 12    | Refresh Rate/Type                                             | S/R, Normal 15.6 ms            |      | 80h               |      |
| 13    | SDRAM Width Primary DRAM                                      | x4                             |      | 04h               |      |
| 14    | ECC SDRAM Data Width                                          | x4                             |      | 04h               |      |
| 15    | Min. clock delay, Back to Back Random Column Addresses (ICCD) | 1CLK                           |      | 01h               |      |
| 16    | Burst Length Supported                                        | 1, 2, 4, 8 & Full Page         |      | 8Fh               |      |
| 17    | # Banks on each SDRAM device                                  | 4                              |      | 04h               |      |
| 18    | CAS# Latency                                                  | 2,3                            |      | 06h               |      |
| 19    | CS# Latency                                                   | 0                              |      | 01h               |      |
| 20    | Write Latency                                                 | 0                              |      | 01h               |      |
| 21    | SDRAM Module Attribute                                        | Registered/Buffered and PLL    |      | 1Fh               |      |
| 22    | SDRAM Device Attribute                                        | Vcc +/-10%, B/R, S/W, P/A, A/P |      | 0Eh               |      |
| 23    | Min Clock cycle Time at CL=2 (tCLK)                           | 10ns                           | 15ns | A0h               | F0h  |
| 24    | Max. Data Access Time from clock at CL=2 (tAC)                | 6ns                            | 8ns  | 60h               | 80h  |
| 25    | Min Clock cycle Time at CL=1 (tCLK)                           | N/A                            |      | 00h               |      |
| 26    | Max. Data Access Time from clock at CL=1 (tAC)                | N/A                            |      | 00h               |      |
| 27    | Min. Row Precharge Time (tRP)                                 | 20ns                           |      | 14h               |      |
| 28    | Min. Row Active Delay (tRRD)                                  | 20ns                           |      | 14h               |      |
| 29    | Min. RAS to CAS Delay (tRCD)                                  | 20ns                           |      | 14h               |      |
| 30    | Min. RAS Pulse Width (tRAS)                                   | 50ns                           |      | 32h               |      |
| 31    | Module Bank Density                                           | 128MB                          |      | 20H               |      |
| 32    | Add. & CMD Input Setup Time (tSI)                             | 2ns                            |      | 20h               |      |
| 33    | Add. & CMD Input Hold Time (tHI)                              | 1ns                            |      | 10h               |      |
| 34    | Data Input Setup Time (tSI)                                   | 2ns                            |      | 20h               |      |
| 35    | Data Input Hold Time (tHI)                                    | 1ns                            |      | 10h               |      |
| 36-61 | Superset Information                                          |                                |      | 00h               |      |
| 62    | SPD Revision                                                  | Rev. 1.2                       |      | 12h               |      |
| 63    | Checksum for bytes 0-62                                       | JEDEC Calculation              |      | JEDEC Calculation |      |

## PDC16RV7244C-(102/103)T-S

### SERIAL PD INFORMATION (CONTINUED)

| Byte#   | Function Described                       | Function Supported |      | Hex Value         |      |
|---------|------------------------------------------|--------------------|------|-------------------|------|
|         |                                          | -102               | -103 | -102              | -103 |
| 64      | Manufacturers JEDEC ID code per JEP-106E | Continuation code  |      | 7Fh               |      |
| 65      | Manufacturers JEDEC ID code per JEP-106E | SMART's ID         |      | 94h               |      |
| 66-71   | Manufacturers JEDEC ID code per JEP-106E | None               |      | FFh               |      |
| 72      | Manufacturing location                   | Mfr Specific Data  |      |                   |      |
| 73      | Manufacturer's Part Number               | P                  |      | 50h               |      |
| 74      | Manufacturer's Part Number               | D                  |      | 44h               |      |
| 75      | Manufacturer's Part Number               | C                  |      | 43h               |      |
| 76      | Manufacturer's Part Number               | 1                  |      | 31h               |      |
| 77      | Manufacturer's Part Number               | 6                  |      | 36h               |      |
| 78      | Manufacturer's Part Number               | R                  |      | 52h               |      |
| 79      | Manufacturer's Part Number               | V                  |      | 56h               |      |
| 80      | Manufacturer's Part Number               | 7                  |      | 37h               |      |
| 81      | Manufacturer's Part Number               | 2                  |      | 32h               |      |
| 82      | Manufacturer's Part Number               | 4                  |      | 34h               |      |
| 83      | Manufacturer's Part Number               | 4                  |      | 34h               |      |
| 84      | Manufacturer's Part Number               | C                  |      | 43h               |      |
| 85      | Manufacturer's Part Number               | 1                  | 1    | 31h               | 31h  |
| 86      | Manufacturer's Part Number               | 0                  | 0    | 30h               | 30h  |
| 87      | Manufacturer's Part Number               | 2                  | 3    | 32h               | 33h  |
| 88      | Manufacturer's Part Number               | T                  |      | 54h               |      |
| 89      | Manufacturer's Part Number               | S                  |      | 53h               |      |
| 90      | Manufacturer's Part Number               | None               |      | FFh               |      |
| 91      | Revision Code                            | Mfr Specific Data  |      | Mfr Specific Data |      |
| 92      | Revision Code                            | None               |      | FFh               |      |
| 93      | Manufacturing Date                       | DATE               |      | DATE              |      |
| 94      | Manufacturing Date                       | DATE               |      | DATE              |      |
| 95-98   | Assembly Serial Number                   | Serial Number      |      | S.No.             |      |
| 99      | Manufacturer Specific Data               | S                  |      | 53h               |      |
| 100     | Manufacturer Specific Data               | M                  |      | 4Dh               |      |
| 101     | Manufacturer Specific Data               | A                  |      | 41h               |      |
| 102     | Manufacturer Specific Data               | R                  |      | 52h               |      |
| 103     | Manufacturer Specific Data               | T                  |      | 54h               |      |
| 104     | Manufacturer Specific Data               | M                  |      | 4Dh               |      |
| 105     | Manufacturer Specific Data               | o                  |      | 6Fh               |      |
| 106     | Manufacturer Specific Data               | d                  |      | 64h               |      |
| 107     | Manufacturer Specific Data               | u                  |      | 75h               |      |
| 108     | Manufacturer Specific Data               | l                  |      | 6Ch               |      |
| 109     | Manufacturer Specific Data               | a                  |      | 61h               |      |
| 110     | Manufacturer Specific Data               | r                  |      | 72h               |      |
| 111     | Manufacturer Specific Data               | T                  |      | 54h               |      |
| 112     | Manufacturer Specific Data               | e                  |      | 65h               |      |
| 113     | Manufacturer Specific Data               | c                  |      | 63h               |      |
| 114     | Manufacturer Specific Data               | h                  |      | 68h               |      |
| 115     | Manufacturer Specific Data               | n                  |      | 6Eh               |      |
| 116     | Manufacturer Specific Data               | o                  |      | 6Fh               |      |
| 117     | Manufacturer Specific Data               | l                  |      | 6Ch               |      |
| 118     | Manufacturer Specific Data               | o                  |      | 6Fh               |      |
| 119     | Manufacturer Specific Data               | g                  |      | 67h               |      |
| 120     | Manufacturer Specific Data               | i                  |      | 69h               |      |
| 121     | Manufacturer Specific Data               | e                  |      | 65h               |      |
| 122     | Manufacturer Specific Data               | s                  |      | 73h               |      |
| 123     | Manufacturer Specific Data               | None               |      | FFh               |      |
| 124     | Manufacturer Specific Data               | None               |      | FFh               |      |
| 125     | Manufacturer Specific Data               | None               |      | FFh               |      |
| 126     | Intel Spec Frequency                     | 100Mhz             |      | 64h               |      |
| 127     | Intel Spec Detail for 100Mhz             | 1000-1111          |      | 8Fh               |      |
| 128-255 | Open for CPQ Use for Read & Write        | None               |      | FFh               |      |

## DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted) Notes 1,2

| Parameter                                           | Symbol       | Conditions                                                                                                                                                                                                                             | Value |      | Unit    |
|-----------------------------------------------------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------|---------|
|                                                     |              |                                                                                                                                                                                                                                        | Min.  | Max. |         |
| Output High Voltage                                 | $V_{OH(DC)}$ | $I_{OH} = -2mA$                                                                                                                                                                                                                        | 2.4   | -    | V       |
| Output Low Voltage                                  | $V_{OL(DC)}$ | $I_{OL} = 2mA$                                                                                                                                                                                                                         | -     | 0.4  | V       |
| Input Leakage Current (Any Input)                   | $I_{LI}$     | $0V \leq V_{IN} \leq V_{CC}$ ;<br>All other pins not under test = 0V                                                                                                                                                                   | -180  | 180  | $\mu A$ |
| Output Leakage Current                              | $I_{LO}$     | $0V \leq V_{IN} \leq V_{CC}$<br>$D_{out} = \text{Disable}$                                                                                                                                                                             | -20   | 20   | $\mu A$ |
| Operating Current<br>(Average Power Supply Current) | $I_{CC1S}$   | Burst: Length=4,<br>$t_{RC} = \text{min}$ for BL=4,<br>$t_{CK} = \text{min}$ .<br>One bank- active,<br>Outputs open,<br>Addresses changed up to<br>3-times during $t_{RC}$ (min),<br>$0V \leq V_{in} \leq V_{CC}$                      | -     | 1234 | mA      |
|                                                     | $I_{CC1D}$   | Burst: Length=4 (each bank),<br>$t_{RC} = \text{min}$ for BL=4 (each bank),<br>$t_{CK} = \text{min}$ .<br>2 banks active,<br>Output open,<br>Addresses changed up to<br>3-times during $t_{RC}$ (min),<br>$0V \leq V_{in} \leq V_{CC}$ | -     | 1999 | mA      |
| Precharge Standby Current<br>(Power Supply Current) | $I_{CC2P}$   | $CKE = V_{IL}$ ,<br>All banks idle,<br>$t_{CK} = \text{min}$ ,<br>Power down mode,<br>$0V \leq V_{in} \leq V_{CC}$                                                                                                                     | -     | 68   | mA      |
|                                                     | $I_{CC2PS}$  | $CKE = V_{IL}$ ,<br>All banks idle,<br>CLK=H or L,<br>Power down mode,<br>$0V \leq V_{in} \leq V_{CC}$                                                                                                                                 | -     | 50   |         |
| Precharge Standby Current<br>(Power Supply Current) | $I_{CC2N}$   | $CKE = V_{IH}$ ,<br>All banks idle,<br>$t_{CK} = \text{min}$ ,<br>NOP commands only,<br>Input signals (except to CMD) are<br>changed one time during 3 clock<br>cycles,<br>$0V \leq V_{in} \leq V_{CC}$                                | -     | 302  | mA      |
| Precharge Standby Current<br>(Power Supply Current) | $I_{CC2NS}$  | $CKE = V_{IH}$ ,<br>All banks idle,<br>CLK=H or L,<br>Input signals are stable,<br>$0V \leq V_{in} \leq V_{CC}$                                                                                                                        | -     | 68   |         |

**PDC16RV7244C-(102/103)T-S**

(Continued)

| Parameter                                            | Symbol      | Test Condition                                                                                                                                                                                        | Value |      | Unit |
|------------------------------------------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------|------|
|                                                      |             |                                                                                                                                                                                                       | Min.  | Max. |      |
| Active Standby Current (Power Supply Current)        | $I_{CC3P}$  | CKE= $V_{IL}$ ,<br>Any bank active,<br>$t_{CK}=\text{min}$ ,<br>$0V \leq V_{in} \leq V_{CC}$                                                                                                          | -     | 68   | mA   |
|                                                      | $I_{CC3PS}$ | CKE= $V_{IL}$ ,<br>Any bank active,<br>CLK = H or L,<br>$0V \leq V_{in} \leq V_{CC}$                                                                                                                  | -     | 50   | mA   |
|                                                      | $I_{CC3N}$  | CKE= $V_{IH}$ ,<br>Any bank active,<br>$t_{CK}=\text{min}$ ,<br>NOP commands only,<br>Input signals (except to CMD) are<br>changed one time during 3 clock<br>cycles,<br>$0V \leq V_{in} \leq V_{CC}$ | -     | 482  | mA   |
|                                                      | $I_{CC3NS}$ | CKE= $V_{IH}$ ,<br>Any bank active,<br>CLK = H or L,<br>$0V \leq V_{in} \leq V_{CC}$                                                                                                                  | -     | 68   | mA   |
| Burst mode Current<br>(Average Power supply current) | $I_{CC4}$   | $t_{CK}=\text{min}$ ,<br>Burst length=4,<br>Outputs open,<br>Multiple-banks active,<br>Gapless data,<br>$0V \leq V_{in} \leq V_{CC}$                                                                  | -     | 1022 | mA   |
| Refresh Current #1<br>(Average Power Supply Current) | $I_{CC5}$   | Auto-refresh;<br>$t_{CK}=\text{min}$ ,<br>$t_{RC}=\text{min}$ ,<br>$0V \leq V_{in} \leq V_{CC}$                                                                                                       | -     | 4352 | mA   |
| Refresh Current #2 (Average Power Supply Current)    | $I_{CC6}$   | Self-refresh;<br>$t_{CK}=\text{min}$ ,<br>CKE $\leq 0.2V$ ,<br>$0V \leq V_{in} \leq V_{CC}$                                                                                                           | -     | 50   | mA   |

†CL = CAS\* Latency

- Notes:
- $I_{CC}$  depends on the output termination or load conditions, clock cycle rate, and signal clocking rate;  
The specified values are obtained with the output open and no termination register.
  - An initial pause (DESL or NOP) of 200  $\mu s$  is required after power-up followed by a minimum of eight Auto-refresh cycles.

## CAPACITANCE

(TA = +25°C, VCC = 3.3V±0.3V)

| Parameter                                         | Symbol           | Max. | Unit | Note |
|---------------------------------------------------|------------------|------|------|------|
| Input Capacitance (Address, WE*, CE*, RAS*, CAS*) | C <sub>I1</sub>  | 18   | pF   | 1    |
| Input Capacitance (DQMB0~7)                       | C <sub>I2</sub>  | 18   | pF   | 1    |
| Input Capacitance (CS0*, CS2*)                    | C <sub>I3</sub>  | 18   | pF   | 1    |
| Input Capacitance (CLK0)                          | C <sub>I4</sub>  | 33   | pF   | 1    |
| Input Capacitance (CLK1~CLK3)                     | C <sub>I5</sub>  | 35   | pF   | 1    |
| Input/Output Capacitance (DQ0~DQ63)               | C <sub>I/O</sub> | 17   | pF   | 1, 2 |

- Notes: 1. Capacitance is measured with Boonton Meter or effective capacitance method.  
2. CAS\* - V<sub>IH</sub> to disable D<sub>out</sub>.

## AC CHARACTERISTICS: MB81F64842C-(102/103)

(At recommended operating conditions unless otherwise noted) Notes 2,3,4

| Parameter                                     |               | Symbol            | Unit | -102 |      | -103 |      | Notes |
|-----------------------------------------------|---------------|-------------------|------|------|------|------|------|-------|
|                                               |               |                   |      | Min. | Max. | Min. | Max. |       |
| Clock Period                                  | CAS Latency=2 | t <sub>CK2</sub>  | ns   | 10   | -    | 15   | -    |       |
|                                               | CAS Latency=3 | t <sub>CK3</sub>  |      | 10   | -    | 10   | -    |       |
| Clock High Time                               |               | t <sub>CH</sub>   | ns   | 3    | -    | 3    | -    |       |
| Clock Low Time                                |               | t <sub>CL</sub>   | ns   | 3    | -    | 3    | -    |       |
| Input Setup Time                              |               | t <sub>SI</sub>   | ns   | 2    | -    | 2    | -    |       |
| Input Hold Time                               |               | t <sub>HI</sub>   | ns   | 1    | -    | 1    | -    |       |
| Access time from Clock (t <sub>CK</sub> =min) | CAS Latency=2 | t <sub>AC2</sub>  | ns   | -    | 6    | -    | 8    | 5,6   |
|                                               | CAS Latency=3 | t <sub>AC3</sub>  |      | -    | 6    | -    | 6    |       |
| Output In Low-Z                               |               | t <sub>LZ</sub>   | ns   | 0    | -    | 0    | -    |       |
| Output in High-Z                              | CAS Latency=2 | t <sub>HZ2</sub>  | ns   | 3    | 6    | 3    | 8    | 7     |
|                                               | CAS Latency=3 | t <sub>HZ3</sub>  |      | 3    | 6    | 3    | 6    |       |
| Output Hold Time                              | CAS Latency=2 | t <sub>OH</sub>   | ns   | 3    | -    | 3    | -    |       |
|                                               | CAS Latency=3 |                   |      | 3    | -    | 3    | -    |       |
| Time between Auto-Refresh command Interval    |               | t <sub>REFI</sub> | ms   | -    | 65.6 | -    | 65.6 |       |
| Transition Time                               |               | t <sub>T</sub>    | ns   | 0.5  | 2    | 0.5  | 2    |       |
| CKE Set Up time for Power Down Exit           |               | t <sub>CKSP</sub> | ns   | 3    | -    | 3    | -    |       |



## PDC16RV7244C-(102/103)T-S

### BASE VALUES FOR CLOCK COUNT/LATENCY: MB81F64842C-(102/103)

| Parameter                                | Symbol        | Unit       | -102          |        | -103          |        | Notes |
|------------------------------------------|---------------|------------|---------------|--------|---------------|--------|-------|
|                                          |               |            | Min.          | Max.   | Min.          | Max.   |       |
| RAS Cycle Time                           | $t_{RC}$      | ns         | 70            | -      | 70            | -      | 8     |
| RAS Precharge Time                       | $t_{RP}$      | ns         | 20            | -      | 20            | -      |       |
| RAS Active Time                          | $t_{RAS}$     | ns         | 50            | 110000 | 50            | 100000 |       |
| RAS to CAS Delay Time                    | $t_{RCD}$     | ns         | 20            | -      | 20            | -      | 9     |
| Write Recovery Time                      | $t_{WR}$      | ns         | 10            | -      | 10            | -      |       |
| Data-in to Precharge Lead Time           | $t_{DPL}$     | ns         | 10            | -      | 10            | -      |       |
| Data-in to Active/Refresh command period | CAS Latency=2 | $t_{DAL2}$ | $1cyc+t_{RP}$ | -      | $1cyc+t_{RP}$ | -      |       |
|                                          | CAS Latency=3 | $t_{DAL3}$ | $2cyc+t_{RP}$ | -      | $2cyc+t_{RP}$ | -      |       |
| Mode Register set cycle Time             | $t_{RSC}$     | ns         | 20            | -      | 20            | -      |       |
| RAS to RAS Bank Active Delay Time        | $t_{RRD}$     | ns         | 20            | -      | 20            | -      |       |

### CLOCK COUNT FORMULA

(Note 10)

$$\text{Clock} \geq \frac{\text{Base Value}}{\text{Clock Period}} \quad (\text{Round off a whole number})$$

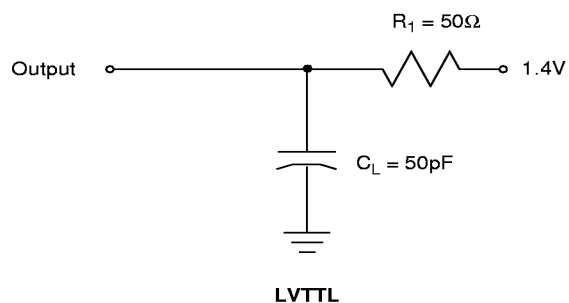
### LATENCY-FIXED VALUES: MB81F64842C-(102/103)

(The latency values on these parameters are fixed regardless of clock period)

| Parameter                                    | Symbol    | Unit       | -102 | -103 | Notes |
|----------------------------------------------|-----------|------------|------|------|-------|
| CKE to Clock Disable                         | $I_{CKE}$ | cycle      | 1    | 1    |       |
| DQM to Output in High-Z                      | $I_{DQZ}$ | cycle      | 2    | 2    |       |
| DQM to Input Data Delay                      | $I_{DQD}$ | cycle      | 0    | 0    |       |
| Last Output to Write Command Delay           | $I_{OWD}$ | cycle      | 2    | 2    |       |
| Write Command to Input Data Delay            | $I_{DWD}$ | cycle      | 0    | 0    |       |
| Precharge to Output in High-Z Delay          | CL = 2    | $I_{ROH2}$ | 2    | 2    |       |
|                                              | CL = 3    | $I_{ROH3}$ | 3    | 3    |       |
| Burst Stop Command to Output in High-Z Delay | CL = 2    | $I_{BSH2}$ | 2    | 2    |       |
|                                              | CL = 3    | $I_{BSH3}$ | 3    | 3    |       |
| CAS to CAS Delay (min)                       | $I_{CCD}$ | cycle      | 1    | 1    |       |
| CAS Bank Delay (min)                         | $I_{CBD}$ | cycle      | 1    | 1    |       |

- Notes:
- $I_{CC}$  depends on the output termination or load conditions, clock cycle rate, and signal clocking rate; The specified values are obtained with the output open and no termination register.
  - An initial pause (DESL or NOP) of 200  $\mu$ s is required after power-up followed by a minimum of eight Auto-refresh cycles.
  - AC characteristics assume  $t_T = 1$  ns and 50 pF of capacitive load.
  - 1.4 V is the reference level for measuring timing of input signals. Transition times are measured between  $V_{IH}$  (min) and  $V_{IL}$  (max).
  - Assumes  $t_{RCD}$  is satisfied.
  - $t_{AC}$  also specifies the access time at burst mode.
  - Specified where output buffer is no longer driven.
  - Actual clock count of  $t_{RC}$  ( $I_{RC}$ ) will be sum of clock count of  $t_{RAS}$  ( $I_{RAS}$ ) and  $t_{RP}$  ( $I_{RP}$ ).
  - Operation within the ( $t_{RCD}$ ) (min) ensures that access time is determined by ( $t_{RCD}$ ) (min) + ( $t_{AC}$ ) (max); If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (min), access time is determined by  $t_{AC}$ .
  - All base values are measured from the clock edge at the command input to the clock edge for the next command input. All clock counts are calculated by a simple formula: clock count equals base value divided by clock period (round off a whole number).

**Fig. 4 - EXAMPLE OF AC TEST LOAD CIRCUIT**

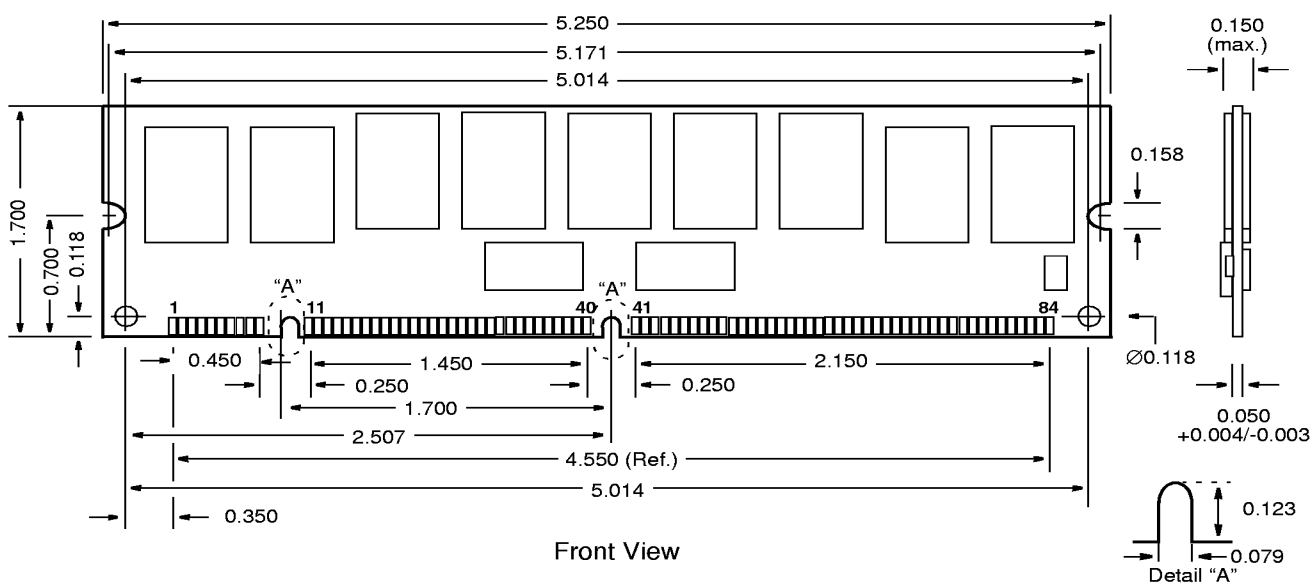


**Note:** AC characteristics are measured in this condition. This load circuits are not applicable for  $V_{OH}$  and  $V_{OL}$ .

## **PDC16RV7244C-(102/103)T-S**

### **Physical Dimensions**

168-pin (84x2) 3.3V DIMM



- Notes:
1. All dimensions are in inches.
  2. Pin 85 is behind pin 1 on the back side.

## Ordering Information

**P D C 16 R V 72 4 4 C - 102 T - S**

(1) (2) (3) (4) (5) (6) (7) (8) (9) (10) (11) (12) (13)

- |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
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| <p>(1) <b>Memory Type</b><br/>S : SDRAM (PC/66)<br/>G : SGRAM<br/>P : SDRAM-Fast (PC/100)</p> <p>(2) <b>Module Shape</b><br/>S : SIMM<br/>D : DIMM<br/>O : Small Outline DIMM</p> <p>(3) <b>Module Pin Count</b><br/>A : 72-pin<br/>B : 144-pin<br/>C : 168-pin<br/>D : 200-pin</p> <p>(4) <b>Word Depth</b><br/>1 : 1M<br/>2 : 2M<br/>4 : 4M<br/>8 : 8M<br/>16 : 16M<br/>256 : 256K<br/>512 : 512K</p> <p>(5) <b>Buffer Type</b><br/>B : Buffered<br/>U : Unbuffered<br/>R : Registered</p> <p>(6) <b>Operating Voltage &amp; Power Consumption</b><br/>V : 3.3V &amp; LVTTTL &amp; Standard Power<br/>L : 3.3V &amp; LVTTTL &amp; Low Power<br/>S : 3.3V &amp; SSTL &amp; Standard Power</p> <p>(7) <b>Data Width</b><br/>(ex. 64=x64, 72=x72 etc.)</p> <p>(8) <b>Device Configuration</b><br/>4 : x4<br/>8 : x8<br/>1 : x16<br/>3 : x32</p> <p>(9) <b>Refresh</b><br/>2 : 2krf<br/>4 : 4krf<br/>8 : 8krf</p> | <p>(10) <b>Module Revision / Applied "Standard" *1</b><br/>Blank : Rev. 0<br/>A : Rev. 1<br/>B : Rev. 2 (etc.)</p> <p>*1 When DRAM device or PCB is revised, the revision is changed</p> <p>(11) <b>Clock Frequency</b><br/><i>SDRAM</i><br/>100 : 100Mhz<br/><br/><i>SDRAM-Fast (100Mhz, PC/100)</i><br/>102 : CL=2; t<sub>RCD</sub>=2; t<sub>RP</sub>=2<br/>103 : CL=3; t<sub>RCD</sub>=2; t<sub>RP</sub>=2<br/>10 : CL=3; t<sub>RCD</sub>=3; t<sub>RP</sub>=3</p> <p>(12) <b>Package of Component</b><br/>T : TSOP</p> <p>(13) <b>Assembly &amp; Test Site</b><br/>S : Smart Modular Technologies</p> |
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