



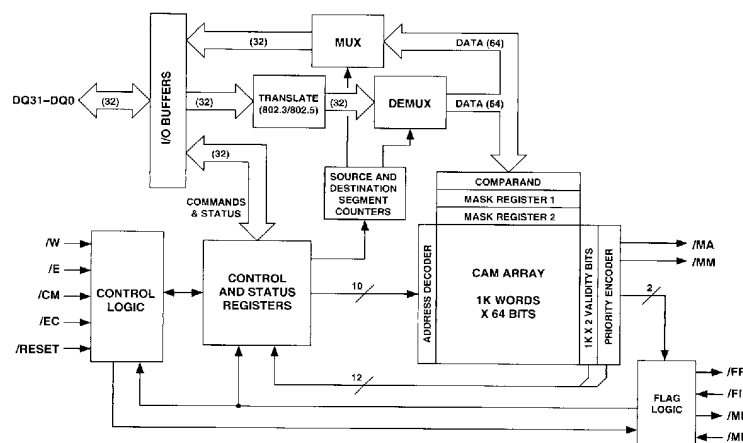
MU9C1485 WidePort LANCAM®

PRELIMINARY DATA SHEET

DISTINCTIVE CHARACTERISTICS

- 32-bit WidePort version of the MU9C1480 LANCAM offers twice the I/O bandwidth for higher performance
- 32-bit Data reads and writes speed access to Comparand register, Mask registers, and Memory array
- 32-bit Command writes and Status reads accelerate control sequence execution
- Dedicated match output pins /MA and /MM give rapid device match status
- 1024 X 64-bit Content-addressable Memory (CAM)
- Two validity bits per entry for increased flexibility—can be read via the Status register
- Priority encoder returns Highest-priority Match address
- Patented Associated Data feature allows storage of related data with each CAM entry
- Memory Array width can be configured as a mixture of CAM and RAM on 16-bit boundaries
- 64-bit internal data path multiplexed two ways over 32-bit I/O interface
- Memory operations allow random access, associative access, and write-at-next-free-address cycles
- Extensive instruction set adds control flexibility
- Two Mask registers allow masking of individual bits for both writing and comparing
- Vertical cascading and system flag generation require no external logic
- Programmable data translation facility converts between IEEE 802.3 and 802.5 formats
- 80-pin TQFP package

BLOCK DIAGRAM



GENERAL DESCRIPTION

The MU9C1485 LANCAM is a 1K x 64-bit Content-addressable Memory (CAM), featuring a 32-bit wide interface. This interface doubles the available I/O bandwidth while maintaining the same powerful architecture and instruction set of the industry standard MU9C1480.

Content-addressable Memories, also known as Associative Memories, operate in the converse way to Random Access Memories. In a RAM, the input to the device is an address, and the output is the data stored at that address. In a CAM, the input is a data sample and the output is a flag to indicate a match and the address of the matching data. As a result, a CAM searches large data bases for matching data in a short,

constant time period, no matter how many entries are in the data base. The ability to search data words up to 64 bits wide allows large address spaces to be searched rapidly and efficiently. A patented architecture links each CAM entry to associated data and makes this data available for use after a successful compare operation.

While the WidePort LANCAM is optimized for WAN and LAN address filtering as well as ATM address translation, it is also well-suited for applications that require high-speed data searching, such as virtual memories, optical and magnetic disk caches, data compressors, data base accelerators, and image processors.

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OPERATIONAL OVERVIEW

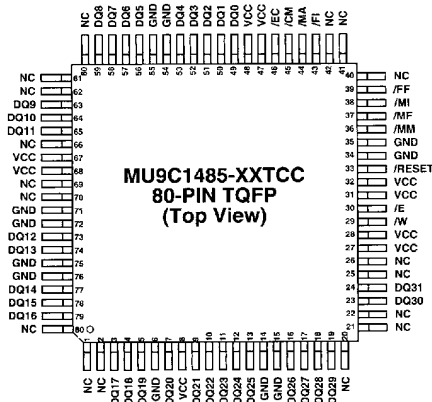
To use the WidePort LANCAM, the user loads a data sample into the Comparand register, which is automatically compared to all valid CAM locations. The device then indicates whether or not one or more of the valid CAM locations contains data that matches the data sample. The status of each CAM location is determined by two validity bits at each memory location. The two bits are encoded to render four validity conditions: Valid, Skip, Empty, and Random Access. The memory can be partitioned into CAM and associated RAM segments on 16-bit boundaries. By using one of the two available mask registers, the CAM/RAM partitioning can effectively be set at any arbitrary size between zero and 64 bits.

The MU9C1485 LANCAM's internal data path is 64 bits wide for rapid internal comparison and data movement. A data translation facility converts between IEEE 802.3 (CSMA/CD "Ethernet") and 802.5 (Token Ring) address formats. Vertical cascading of additional WidePort LANCAMs in a daisy-chain fashion extends the CAM memory depth for large data bases. Cascading requires no external

logic. Loading data automatically triggers a compare, and compares may also be initiated by a command to the device. Associated RAM data is available immediately after a successful compare operation. The Status register reports the results of compares including all flags and addresses. Two mask registers are available and can be used in two different ways: to mask comparisons or to mask data writes. The random access validity flag allows additional masks to be stored in the CAM array where they may be retrieved rapidly.

The device is controlled by a simple four-wire control interface and commands loaded into the Instruction decoder. A powerful instruction set increases the control flexibility and minimizes software overhead. Additionally, dedicated pins for match and multiple-match flags enhance performance when the device is controlled by a state machine. These and other features make the WidePort LANCAM a powerful associative memory that drastically reduces search delays.

PINOUT DIAGRAM



PIN DESCRIPTIONS

Note that signal names that start with a slash ("/") are active LOW. All signals are TTL level signals implemented in CMOS technology. Never leave inputs floating. The CAM architecture draws large currents during compare operations, mandating the use of good layout and bypassing techniques. Refer to the Electrical Characteristics section for more information.

DQ31-DQ0 (Data Bus, Common I/O, TTL)

The DQ31-DQ0 lines convey data, commands and status to and from the MU9C1485. The direction and nature of the information that flows to or from the

device is controlled by the states of /W and /CM, respectively.

/E (Chip Enable, Input, TTL)

The /E input enables the device while LOW, registers the control signals /W, /CM, /EC on its falling edge, and releases them on the rising edge. The Destination and Source Segment counters are clocked on the rising edge of /E.

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PIN DESCRIPTIONS (CONT'D)

/W (Write Enable, Input, TTL)

The /W input selects the direction of data flow during a memory cycle. /W LOW selects a Write cycle, and /W HIGH selects a Read cycle.

/CM (Data/Command Select, Input, TTL)

The /CM input selects whether the input signals on DQ31–DQ0 are data or commands. /CM LOW selects Command cycles, and /CM HIGH selects Data cycles.

/EC (Enable Daisy Chain, Input, TTL)

The /EC signal performs two functions: The /EC input enables the /MF output to show the results of a comparison. If /EC is LOW at the falling edge of /E in a given cycle, the /MF output is enabled. Otherwise, the /MF output is held HIGH. The /EC signal also enables the /MF-/MI daisy-chain, which serves to select the Highest-priority Matching device in a string of WidePort LANCAMs. Table 5 explains the effect of the /EC signal on a device with and without a match. /EC must be HIGH during initialization.

/MF (Match Flag, Output, TTL)

The /MF output goes LOW when one or more valid matches occur during a compare cycle. /MF becomes valid after /E goes HIGH on the cycle that enables the daisy chain (the first cycle that /EC is registered LOW by the previous falling edge of /E). In a daisy-chain, valid match(es) in higher priority devices are passed from the /MI input to /MF. If the daisy chain is enabled but the match flag is disabled in the control register, the /MF output only depends on the /MI input of the device (/MF=/MI). /MF is HIGH if there is no match or when the daisy chain is disabled (/E goes HIGH when /EC was HIGH on the previous falling edge of /E).

/MI (Match Input, Input, TTL)

The /MI input prioritizes devices in vertically cascaded systems. It is connected to the /MF output of the previous (next higher-priority) device in the daisy chain. The /MI pin on the highest-priority device must be tied HIGH.

/MA (Internal Match Flag, Output, TTL)

The /MA output is LOW when one or more valid matches occur during the current or the most-recent compare cycle. The /MA output is not qualified by /EC or /MI, and is solely a reflection of the internal match flag of that specific device.

/MM (Multiple Match Flag, Output, TTL)

The /MM output is LOW when more than one valid match occurs during the current or the most-recent compare cycle. The /MM output is not qualified by /EC or /MI, and is solely a reflection of the internal multiple match flag of that specific device.

/FF (Full Flag, Output, TTL)

If enabled in the control register, the /FF output goes LOW when no empty memory locations exist within the device (or the daisy-chain above the device). If disabled in the control register, the /FF output only depends on the /FI input (/FF = /FI).

/FI (Full Input, Input, TTL)

The /FI input generates a CAM-Memory-System-Full indication in vertically cascaded systems. It is connected to the /FF output of the previous (next-higher priority) device in the daisy chain. The /FI pin on the highest-priority device must be tied LOW.

/RESET (Reset, Input, TTL)

Prior to operation, the /RESET pin must be driven LOW for the period tRLRH after power is applied to the device.

VCC, GND (Positive Power Supply, Ground)

These pins are the power supply connections to the MU9C1485. VCC must meet the requirements in the Operating Conditions Section relative to the GND pin, which is at 0 Volts (system reference potential), for correct operation of the device.

FUNCTIONAL DESCRIPTION

The MU9C1485 WidePort LANCAM is a 1K x 64-bit Content-addressable Memory (CAM) for network address filtering, virtual memory, data compression, cache, and table look-up applications. The MU9C1485 contains 65,536 bits of static CAM, organized as 1024 64-bit Data fields. Each Data field can be partitioned into a CAM and a RAM subfield on 16-bit boundaries. The contents of the memory can be randomly accessed or associatively accessed by the use of a compare. During automatic Comparison cycles, data in the Comparand register is automatically compared with the "Valid" CAM section of the memory array.

The MU9C1485 is designed to minimize the external logic needed for expansion and control. It is controlled by four synchronous control signals, and by commands loaded into an Instruction decoder. The /CM signal is used to indicate whether information present on the 32-bit input bus is to be interpreted as a Data or a Command field. Command cycles allow access to the instruction decoder and 32-bit Status register as well as the various 16-bit registers on the device. Data cycles allow access to the 64-bit Comparand or Mask registers as well as the 64-bit memory array. The 32-bit

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FUNCTIONAL DESCRIPTION (CONT'D)

I/O bus is multiplexed two ways to allow access to these 64-bit wide resources.

Appended to each 64-bit data field in the memory array are two bits of CAM storage to indicate the validity of the location. These two bits are encoded to render four validity conditions: Valid data, Skip, Empty, and Random Access only. Automatic compares are performed between the contents of the Comparand register and the entire contents of the CAM entries marked as Valid data. Forced compares can be performed against any of the Validity bit conditions. An opaque mask can be used to find all the entries marked with a particular Validity condition (an opaque mask is automatic for CMP E instructions, which compare against all "empty" entries.) The Validity bits can then be modified on all matching entries simultaneously.

Two Mask registers on the device can be selected to mask Compares or Data writes. For comparison masking, data stored in the selected Mask register determine which bits of the Comparand are compared against CAM entries. During a Write cycle (including Move instructions,) data in the designated Mask register determines which bits in the destination are written.

The Match line associated with each location is fed into a Priority encoder where multiple matches are resolved, and the address of the Highest-priority match (lowest numbered physical address) is generated. In some applications, knowledge of the existence of multiple matches may be useful and is indicated by the /MM flag in the Status register or the /MM pin on the device.

After a Compare cycle, the Status register contains the address of the highest-priority responding location. The highest-priority responding location is defined as the lowest memory location which matches data in the Comparand register, masked by MR1 or MR2 if selected. The Status register also contains the Page Address value, validity bits of the last read memory location, and flags indicating Match, Multiple Match, and Full conditions. Dedicated Match and Multiple Match flag outputs are also available. These flags independently specify the match condition of a particular device and have no relationship to the daisy-chain operation. Match and Full flag outputs for daisy-chaining are also available, providing system Match and Full indications without external logic.

The Page Address register simplifies vertical expansion in systems using more than one MU9C1485. This register is loaded with address information during system initialization. During a Compare cycle, the ten bits of the Match address are fed to the Status register from the Priority encoder and are concatenated with the Page Address register

value. The Device Select register is used to select a particular device in a vertically cascaded WidePort LANCAM array by setting the Device Select equal to the desired Page address. Setting DS = FFFFH will enable all devices for writing, when /EC has not been asserted. After /EC has been asserted, the device with the highest-priority match will respond to both reads and writes.

The Control register sets up operating conditions within the MU9C1485, including Reset, enable or disable Match Flag, enable or disable Full Flag, CAM/RAM partitioning, disable or select masking conditions, and disable or select address auto-increment or auto-decrement.

Source and Destination Segment counters within the MU9C1485 separately control reading and writing data. These counters specify which half of a 64-bit word is to be read or written over the 32-bit I/O bus. A Segment Control register sets the count limits and start values for both the Source and Destination Segment counters.

Figure 1 shows expansion using a daisy-chain. Note that system flags are generated without the need for external logic. The Page Address register allows each device in the vertically cascaded chain to supply its own address in the event of a match, eliminating the requirement for an external Priority encoder to calculate the complete Match address. The Full flag daisy-chaining allows use of Associative writes which do not use a specific address. Thus a Write at Next Free address operates globally.

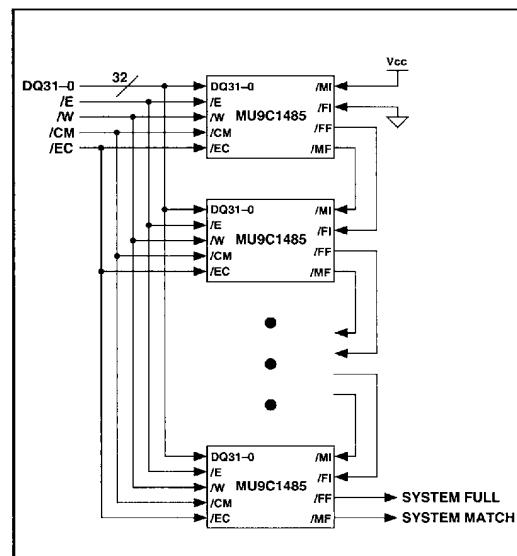


Figure 1: Vertical Cascading

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OPERATIONAL CHARACTERISTICS

Throughout the following, "aaaH" represents a three-digit hexadecimal number "aaa," while "bbB" represents a two-digit binary number "bb." All memory locations are broken into 32-bit segments. Segment 0 corresponds with the lowest order bits (bits 31-0) and Segment 1 corresponds with the highest order bits (bits 63-32).

THE CONTROL BUS

Refer to the Block Diagram for the following discussion. The primary control mechanism for the MU9C1485 is the Control bus which comprises the Chip Enable (/E), the Write Enable (/W), the Command Enable (/CM), and the Enable Daisy Chain (/EC) inputs. The /EC input of the Control bus is responsible for enabling the /MF Match flag output when LOW, and controlling the daisy-chain operation. The secondary control mechanism of the MU9C1485 is by instructions which are decoded by the Instruction decoder. Logical combinations of the Control Bus inputs, coupled with the execution of Select Persistent Source (SPS), Select Persistent Destination (SPD), and Temporary Command Override (TCO) instructions, allow the I/O operations to and from the DQ31-DQ0 lines to the internal resources, as shown in Table 1.

The default source and destination for Data Read and Write cycles is the Comparand register. This default state can be overridden independently by executing a Select Persistent Source or Select Persistent Destination instruction, selecting a different source or destination for data. Subsequent Data Read or Data Write cycles will access that source or destination until another SPS or SPD instruction is executed. The currently selected persistent source or destination can be read back via a TCO PS or PD instruction. The sources and destinations available for persistent access are those resources on the 64-bit bus: Comparand register, Mask Register 1, Mask Register 2, and the Memory array.

The default destination for Command Write cycles is the Instruction decoder, while the default source for Command Read cycles is the Status register. The entire 32-bit Status register is read in a single cycle.

Access to the Control register, the Page Address register, the Segment Control register, the Address register, the Next Free Address register, and Device Select register is by Temporary Command Override (TCO) instructions which are only active for the current instruction in the case of a register write or for one additional cycle in the case of a register read. Each of these 16-bit registers is read out on the DQ15-0 pins. Additionally, the upper 16 bits of the Status register is output on the DQ31-16 pins, except in the case of a Page Address register read where 0s will be read on DQ31-16 instead.

The data and control interfaces to the MU9C1485 are synchronous. During a Write cycle, the Control and Data inputs are registered by the falling edge of /E. When writing to the persistently selected data destination, the Destination Segment counter is clocked by the rising edge of /E. During a Read cycle, the Control inputs are registered by the falling edge of /E, and the Data outputs are enabled while /E is LOW. When reading from the persistently selected data source, the Source Segment counter is clocked by the rising edge of /E.

THE REGISTER SET

A worksheet to assist in decoding the WidePort LANCAM Control register and Segment Control register is included at the back of this document.

Instruction Decoder

The Instruction decoder is the write-only decode logic for instructions and is the default destination for Command Write cycles using the DQ31-DQ16 lines. If the instruction requires an absolute address or register value, the "f" Address flag bit of the instruction is set to a "1", and the data on the DQ15-DQ0 lines are written to the proper register in that same cycle. If the instruction written is a TCO, and the "f" bit is not set, the contents of the register specified by the TCO may be read back by a successive Command Read cycle. The register contents will be present on the DQ15-DQ0 lines.

If the Address flag is set in a memory access instruction, the Address register will automatically be loaded by the absolute address supplied on the DQ15-DQ0 lines. If the Address flag is not set, the memory access occurs at the address currently contained in the Address register. Addresses can be generated in two additional ways. A new address can be forced into the Address register by a TCO instruction that targets the Address register and supplies an absolute address on the DQ15-DQ0 lines. Alternatively, by correctly setting Control register bits CT3 and CT2, the Address register auto-increments or auto-decrements during Data writes or reads to Memory at Address register when either of the Segment counters reaches its end count, after Moves to Memory at Address register, or after VBC Instructions at Address register.

Control Register (CT)

The Control register is composed of a number of switches that configure the WidePort LANCAM, as shown in Table 2. It is written or read via DQ15-0 using a TCO CT instruction. On read cycles, DQ31-16 will be the upper 16 bits of the Status register. If bit 15 of the value written during a TCO CT is a "0", the device is

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OPERATIONAL CHARACTERISTICS (CONT'D)

CycleType	/E	/CM	/W	I/O Status	SPS	SPD	TCO	Operation	Notes
Com Write	L	L	L	IN			✓	Load Instruction decoder	1
				IN			✓	Load Address register	2
				IN			✓	Load Control register	2
				IN			✓	Load Page Address register	2
				IN			✓	Load Segment Control register	2
				IN			✓	Load Device Select register	2
				IN				Deselected	9
Com Read	L	L	H	OUT			✓	Read Next Free Address register	3
				OUT			✓	Read Address register	3
				OUT				Read Status Register bits 31-0	4
				OUT			✓	Read Control Register	3
				OUT			✓	Read Page Address Register	3
				OUT			✓	Read Segment Control Register	3
				OUT			✓	Read Device Select Register	3
				OUT			✓	Read Current Persistent Source or Destination	3,10
				HIGH-Z				Deselected	9
Data Write	L	H	L	IN		✓		Load Comparand Register	5, 8
				IN		✓		Load Mask Register 1	6, 8
				IN		✓		Load Mask Register 2	6, 8
				IN		✓		Write Memory Array at Address	6, 8
				IN		✓		Write Memory Array at Next Free Address	6, 8
				IN		✓		Write Memory Array at Highest-priority Match	6, 8
				IN		✓		Deselected	9
Data Read	L	H	H	OUT	✓			Read Comparand Register	5, 8
				OUT	✓			Read Mask Register 1	7, 8
				OUT	✓			Read Mask Register 2	7, 8
				OUT	✓			Read Memory Array at Address	7, 8
				OUT	✓			Read Memory Array at Highest-priority Match	7, 8
				HIGH-Z				Deselected	9
	H	X	X	HIGH-Z				Deselected	

Notes

1. Default Command Write cycle destination (does not require a TCO instruction).
2. To load a value into a register using a TCO instruction takes one Command Write cycle with the "f" bit equal to "1", and the value to be loaded into the selected register placed in DQ15-DQ0.
3. Reading the contents of a register using a TCO instruction takes two cycles. The first cycle is a Command Write of a TCO instruction with the "f" bit equal to "0". If the next cycle is a Command Read, the value stored in the selected register will be read out on the DQ15-DQ0 lines. Additionally, bits 31-16 of the Status register will be read out on the DQ31-16 lines, except in the case of a Page Address read where 0s will be read on DQ31-16 instead.
4. Default Command Read cycle source (does not require a TCO instruction).
5. Default persistent source and destination on power-up and after Reset. If other resources were sources or destinations, SPD CR or SPS CR restores the Comparand register as the destination or source.
6. Selected by executing a Select Persistent Destination Instruction.
7. Selected by executing a Select Persistent Source Instruction.
8. Access is performed in one or two 32-bit Read or Write cycles. The Segment Control register is used to control the selection of the desired 32-bit segment(s) by establishing the Segment counters' limits and start values.
9. Device is deselected if Device Select register setting does not equal Page Address register setting, unless the Device Select register is set to FFFFH which allows only write access to the device. (Writes to the Device Select register are always active.) Device may also be deselected under various conditions of a locked daisy-chain. Reference Table 5.
10. A TCO PS or TCO PD read back the Instruction decoder bits that were last set to select a persistent source or destination. A Command Read cycle must immediately follow the TCO cycle to read these bits.

Table 1: Input/Output Operations

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OPERATIONAL CHARACTERISTICS (CONT'D)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST	Match Flag	Full Flag	Translation	CAM/RAM Part.	Comp. Mask	AR Inc/Dec	0	0							
R	Enable	Enable	Input Not	64 CAM = "000"	None = "00"	Increment									
E	= "00"	= "00"	Translated	48 CAM = "001"	MR1 = "01"	= "00"									
S	Disable	Disable	= "00"	32 CAM = "010"	MR2 = "10"	Decrement									
E	= "01"	= "01"	Input	16 CAM = "011"	No Change	= "01"									
T	No Change	No Change	Translated	0 CAM = "100"	= "11"	Disable									
=	= "11"	= "11"	= "01"	No Change = "111"		= "10"									
"0"			No Change			No Change									
			= "11"			= "11"									

Table 2: Control Register Bit Assignments

CAM Status	After /RESET Active	Software Reset
Validity bits at all memory locations	Skip = 0, Empty = 1	Same
Match and Full Flag outputs	Enabled	Same
IEEE 802.3-802.5 Input Translation	Not Translated	Same
CAM/RAM Partitioning	64 bits CAM, 0 bits RAM	Same
Comparison Masking	Disabled	Same
Address register auto-increment or -decrement	Disabled	Same
Source and Destination Segment Counters Count Ranges	0 to 1; loaded with 0	Same
Address register and Next Free Address register	Contains all "0"s	Same
Page Address and Device Select registers	Contain all "0"s	Unchanged
Control register after reset (Including CT15)	Contains 0008H	Same
Persistent Destination for Command Writes	Instruction decoder	Same
Persistent Source for Command Reads	Status register	Same
Persistent Source and Destination for Data Reads and Writes	Comparand register	Same

Table 3: Device Control State after Reset

Reset (and all other bits are ignored.) See Table 3 for the reset state. A write to the Control register causes an automatic compare to occur (except in case of a Reset.)

If the Match Flag is disabled via bits 14 and 13, the internal match condition used to determine a daisy-chained device's response is forced HIGH (Internal /MA = 1 in Table 5: Device Select Response), so that Case 6 is not possible, effectively removing the device from the daisy-chain. With the Match Flag disabled, /MF=/MI, and operations directed to Highest-priority Match locations are ignored. Normal operation of the device is with the /MF enabled. The Match Flag Enable field has no effect on the /MA or /MM output pins or Status register bits. These bits always reflect the true state of the device.

If the Full Flag is disabled via bits 12 and 11, the device behaves as if it is full and ignores instructions to Next Free Address. Additionally, writes to the Page

Address register will be disabled. All other instructions operate normally. Additionally, with the /FF disabled, /FF=/FI. Normal operation of the device is with the /FF enabled. The Full Flag Enable field has no effect on the /FL Status register bit. This bit always reflects the true state of the device.

The IEEE Translation control at bits 10 and 9 can be used to enable the translation hardware for writes to 64-bit resources in the device. When translation is enabled, the bits are reordered as shown in Figure 6.

The CAM/RAM partitioning is controlled at bits 8-6, and may be set in 16-bit increments. The CAM portion of each word may be sized from a full 64 bits down to 0 bits. The RAM portion is always extended from the least significant part of the 64-bit word.

Compare masks may be selected by bits 5 and 4. Mask Register 1, Mask Register 2, or no mask at all may be selected to mask compare operations.

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OPERATIONAL CHARACTERISTICS (CONT'D)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0		0			0		0			0			0	
Set Dest. Seg. Limits = "0" No Chng. = "1"	Dest. Count Start Limit	Dest. Count End Limit	Set Source Seg. Limits = "0" No Chng. = "1"	Src. Count Start Limit	Src. Count End Limit	Load Dest. Seg. Count = "0" No Chng. = "1"	Load Dest. Seg. Count = "0" No Chng. = "1"	Dest. Seg. Count Value	Load Src. Seg. Count = "0" No Chng. = "1"	Src. Seg. Count Value					

Note: D15, D10, D5 and D2 read back as "0"s.

Reserved locations D14, D12, D9, D7, D4, and D1 should always be set to "0" and as such will read back as "0"s.

Table 4: Segment Control Register Bit Assignments

The address register behavior is controlled by bits 3 and 2. It may be set to increment, decrement or remain the same after a memory access.

Bits 1 and 0 are reserved. They should always be set to "0"s and will read back as "0"s.

Segment Control Register (SC)

The Segment Control register, as shown in Table 4, is accessed using a TCO SC instruction with the register contents placed on DQ15-0. On read cycles, DQ31-16 will be the upper 16 bits of the Status register.

The Segment Control register contains dual independent incrementing counters with limits; one for data reads and one for data writes. These counters control which 32-bit segment of the 64-bit internal resource is accessed during a particular data cycle on the 32-bit data bus. The actual destination for data writes and source for data reads (called the persistent destination and source) are set independently with SPD and SPS instructions, respectively.

Each of the two counters consists of a start segment, the end segment, and the current segment pointer, each a single bit representing either the lower segment ("0") or the upper segment ("1"). The current segment pointer can be set to either "0" or "1" even if it's outside the range set by the start and end segments.

After a Reset, both Source and Destination counters are set to count from Segment 0 to Segment 1 with an initial value of 0. D15, D10, D5 and D2 always read back as "0"s. Reserved locations D14, D12, D9, D7, D4 and D1 should always be set to "0" and as such will also read back as "0"s.

Page Address Register (PA)

The Page Address register is loaded using a TCO PA instruction with a user selected 16-bit value (not FFFFH) on DQ15-0. During reads of the PA register, DQ31-16 will all be "0". The entry in the PA register is used to give a unique address to the different devices in a daisy-chain. In a daisy-chain, the PA value of each device is loaded using the SFF instruction to advance to the next device. (Reference the section "Setting Page Address Register Values" for details.) A software Reset does not affect the Page Address register.

Case	Internal /EC	Internal /MA	External /MI	Device Select Reg.	Command Write*	Data Write	Command Read	Data Read
1	1	X	X	DS = FFFFH	YES	YES	NO	NO
2	1	X	X	DS = PA	YES	YES	YES	YES
3	1	X	X	DS ≠ FFFFH and DS ≠ PA	NO	NO	NO	NO
4	0	X	0	X	NO	NO	NO	NO
5	0	1	1	X	NO	NO	NO	NO
6	0	0	1	X	YES	YES	YES	YES

*Note: Exceptions are 1) Write to Device Select register is always active in all devices, 2) Write to Page Address register is active in the device with /FI LOW and /FF HIGH; 3) the Set Full Flag (SFF) instruction is active in the device with /FI LOW and /FF HIGH; and, 4) if /MF is disabled in the Control Register, /MA (Internal) is forced HIGH preventing a Case 6 response.

Table 5: Device Select Response

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OPERATIONAL CHARACTERISTICS (CONT'D)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
/MA	/MM	/FL	Skip	Empty	0	Page Address Bits, PA15-PA6									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PA5-PA0						Match Address, AM9-AM0									

Note: Bit 26 is reserved, and as such will read as "0".

Table 6: Status Register Bit Assignments

Device Select Register (DS)

The Device Select register is used to select a specific (target) device using the TCO DS instruction by setting the 16-bit DS value equal to the target's PA value. The DS register is accessed via DQ15-0 with DQ31-16 reading back as the upper 16 bits of the Status register. In a daisy-chain, setting DS = FFFFH will select all devices. However, in this case, the ability to read information out of the device is restricted as shown in Table 5. A software Reset (using the Control register) does not affect the Device Select register.

Address Register (AR)

The Address register points to the CAM Memory location to be operated upon with a M@[AR] or M@aaaH instruction. It can be loaded directly by using a TCO AR instruction or indirectly by using an instruction requiring an absolute address, such as MOV aaaH,CR,V. The AR register is accessed via DQ15-0 with DQ31-16 reading back as the upper 16 bits of the Status register. After being loaded, the Address register value will then be used for the next memory access referencing the Address register. Immediately after this access, the Address register will automatically increment or decrement from that value according to the setting of bits CT3 and CT2 of the Control register. A Reset sets the Address register to zero.

Next Free Address Register (NF)

The Next Free Address register is updated when executing instructions that could potentially affect the validity bits. The Next Free Address register for a particular device can be read via DQ15-0 using a TCO NF instruction. DQ31-16 will read back as the upper 16 bits of the Status register. It stores the address of the first empty location in the CAM memory, and is

Skip	Empty	Validity Condition
0	0	Valid
0	1	Empty
1	0	Skip
1	1	Random

Table 7: Validity Bit Encoding

used as a pointer for M@NF operations. After a Reset, the Next Free Address register is set to zero.

Status Register

The 32-bit Status register, shown in Table 6, is the default source for Command Read cycles. Bit 31 is the internal Match flag, which will go LOW if a match was found in this particular device. Bit 30 is the internal Multiple Match flag, which will go LOW if a Multiple match was detected. Bit 29 is the internal Full flag, which will go LOW if the particular device has no empty memory locations. Bits 28 and 27 are the Skip and Empty validity bits which reflect the validity of the last memory location read or moved to a register, as shown in Table 7. After a Reset, Skip and Empty both read as "1". Bit 26 is reserved and will always read as "0". Bits 25-10 give the Page Address of the device. Bits 9-0 give the match address of the Highest-priority match. After a Reset or a no-match condition, the match address will be all "1"s.

Comparand Register (CR)

The 64-bit Comparand register is the default destination for Data Writes and Reads, using the Segment Control register to select the segment of the Comparand register to be loaded or read out. The Persistent Source and Destination for Data Writes and Reads can be changed to the Mask registers or Memory by SPS and SPD instructions. During an automatic or forced compare, the Comparand register is compared against the CAM portion of all memory locations with the correct validity condition simultaneously. Automatic compares always compare against Valid Memory locations, while forced compares, using CMP instructions, can compare against Memory locations tagged with any specific validity condition.

Mask Registers (MR1, MR2)

The Mask registers can be used in two different ways, either to mask compares or to mask data writes and moves. Either Mask register can be selected in the Control register to mask every compare, or selected by instructions to participate in data writes or moves to and from Memory. If a bit in a 64-bit Mask register is set to a "0", the corresponding bit in the Comparand

■ 6411817 0000439 07T ■

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/W	/CM	Cycle Type	"f" Bit	DQ31-DQ16	DQ15-DQ0
LOW	LOW	Command Write	0	Non-TCO Instruction	X
			1	Non-TCO Instruction	Absolute Address
			0	TCO Instruction (Read Register)*	X
			1	TCO Instruction (Write Register)	Register Contents
LOW	HIGH	Data Write	X	MS Data	LS Data
HIGH	LOW	Command Read	X	Status Register bits 31-16	Status Register bits 15-0
			X	Status Register bits 31-16†	Register Contents*
HIGH	HIGH	Data Read	X	MS Data	LS Data

Notes: * A TCO instruction with the "f" bit set to 0 sets up a register read in the following cycle. The following cycle must be a Command Read cycle, otherwise the register read will be cancelled.

† Upper 16 bits will be Status register bits 31-16, except for a read of the Page Address register, in which case they will be all zeros.

Table 8: I/O Cycles

register will enter into a masked compare operation. If a Mask bit is a "1", the corresponding bit in the Comparand register will not enter into a masked compare operation. Bits set to "0" in the Mask register cause corresponding bits in the destination register or memory location to be updated when masking data writes or moves, while a bit set to "1" will prevent that bit in the destination from being changed.

THE MEMORY ARRAY

Memory Organization

The Memory array is organized as 1024 64-bit locations, each having two Validity bits, the Skip bit and Empty bit. By default all locations are configured to be 64 CAM cells. However, the array can be reconfigured in the Control register to divide each location into a CAM field and a RAM field. The RAM field is assigned to the least-significant portion of each entry. The CAM/RAM partitioning is allowed on 16-bit boundaries, permitting selections of 64 CAM bits, 0 RAM bits; 48 CAM bits, 16 RAM bits; 32 CAM bits, 32 RAM bits; 16 CAM bits, 48 RAM bits; 0 CAM bits, 64 RAM bits. Memory Array bits designated to be RAM bits can be used to store and retrieve Associated data (data associated with a CAM content).

Memory Access

There are two general ways to get data into and out of the memory array, directly or by moving the data via the Comparand or Mask registers.

The first way, through direct reads or writes, is set up by issuing a Set Persistent Destination (SPD) or Set Persistent Source (SPS) command. The addresses for the direct access can be directly supplied, supplied from the address register, supplied from the Next Free Address Register, or supplied as the Highest-priority Match address. Additionally, all the direct writes can be masked by either mask register.

Setting the persistent source or destination to M@aaaH will load the Address register with aaaH. All accesses to the persistent source or destination will be with respect to the address register and will follow the address increment or decrement specified by the Control register. Using M@[AR] will yield the same functionality with the exception that the Address register will not be loaded.

The second way to access the memory array is to move data via the Comparand or Mask registers. This is accomplished by issuing Data Move commands (MOV). Moves using the Comparand register can also be masked by either of the Mask registers.

I/O CYCLES

The MU9C1485 supports four basic I/O cycles: Data Read, Data Write, Command Read, and Command Write. The type of cycle is determined by the states of the /W and /CM control inputs. These signals are registered at the beginning of a cycle by the falling edge of /E. Table 8 shows how the /W and /CM lines select the cycle type and how the data bus is utilized for the various cycle types.

During Read cycles, the DQ31-DQ0 outputs are enabled after /E goes LOW. During Write cycles, the data or command to be written is captured from DQ31-DQ0 at the beginning of the cycle by the falling edge of /E. Figures 2 and 3 show Read and Write cycles respectively. Figure 4 shows typical cycle-to-cycle timing with the Match flag valid at the end of the comparand write cycle, assuming /EC is LOW at the start of this cycle. The Compare operation automatically occurs when the segment counter reaches the end count set in the Segment Control register (for Data writes to the Comparand or Mask registers). If there was a match, the second cycle reads status or associated data, depending on the state of /CM. For cascaded devices, /EC needs to be held LOW in the cycle prior to any cycle which

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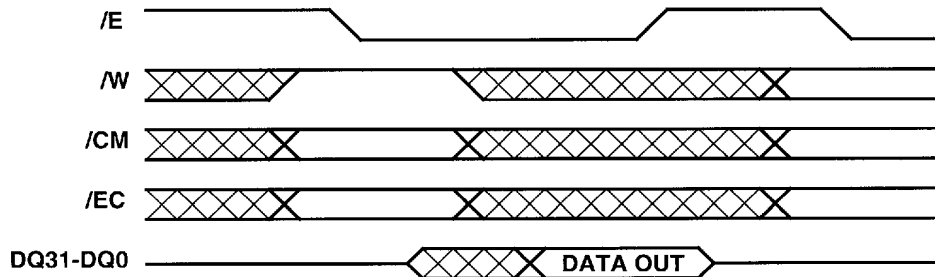


Figure 2: Read Cycle

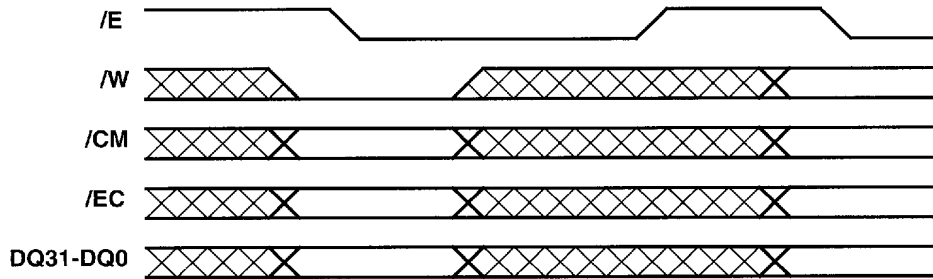


Figure 3: Write Cycle

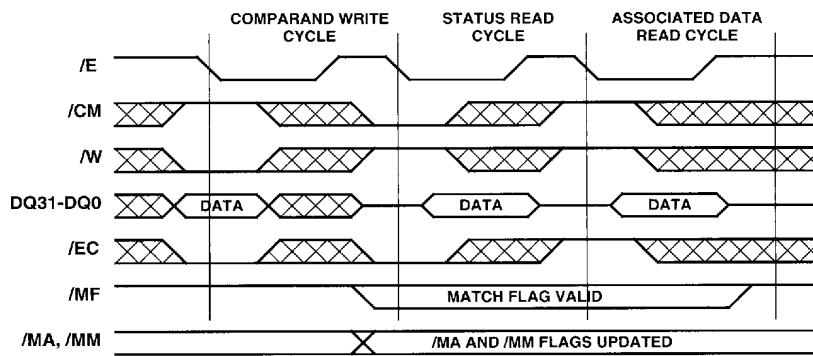


Figure 4: Example Cycle to Cycle Timing

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requires a locked daisy-chain, such as a Status register or associated data read after a match. If there was not a match, the output buffers stay Hi-Z, and the daisy-chain must be unlocked by taking /EC HIGH and asserting /E, for a cycle. Figure 5 shows how the internal /EC timing holds the daisy-chain locking effect over into the next cycle. In a single-chip system, /EC would be tied high and the /MA flag would be used instead of /MF, allowing access to the device regardless of the match condition.

The minimum timings for the /E control signal are given in the Electrical Characteristics section. Note that at minimum timings the /E signal is non-symmetrical, and that different cycle types have different timing requirements as given in Table 10.

COMPARE OPERATIONS

All compare operations available in the WidePort LANCAM are similar in that the data in the Comparand register are compared to all locations in the Memory array simultaneously. There are two ways compares are initiated: Automatic and Forced compares. The mask registers to be used for compares is selected in the Control register.

Automatic compares perform a compare of the contents of the Comparand register against Memory locations that are tagged as "Valid", and occur whenever the following happens:

1. The Destination Segment counter in the Segment Control register reaches its end limit during writes to the Comparand or Mask registers.
2. After a command write of the TCO CT command is executed, i.e. a compare is executed with the new Control register settings.

Forced compares are initiated by CMP instructions using one of the four validity conditions. The forced compare against "Empty" locations automatically masks all 64 bits of data to find all locations with the validity bits set to "Empty", while the other forced compares are only masked as selected in the Control register.

VERTICAL CASCADING

The MU9C1485 can be vertically cascaded to increase system depth. Through the use of flag daisy-chaining, multiple WidePort LANCAMs will respond as an integrated system. The daisy-chain of flags allows all commands to operate globally. For example, operations at the Next Free address or at the Highest-priority Match address will only operate in the device in a string that actually has the first empty location or the first matching location, respectively.

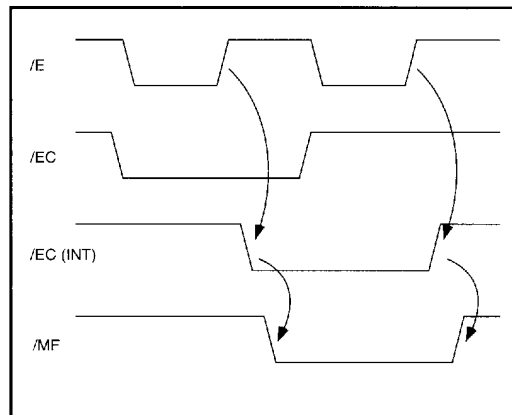


Figure 5: /EC(Int) Timing Diagram

When connected in a daisy-chain, the last device's Full flag and Match flag accurately report the condition for the whole string. By setting the Page Address and Device Select registers to the same value, individual devices in a daisy-chain can be addressed. The ripple delay of the flags when connected in a daisy-chain requires the extension of the /E HIGH time until the logic in all devices has settled out. In a string of "n" devices, the /E HIGH time should be greater than $t_{EHMFV} + (n-1) \cdot t_{MIVMFV}$. A system in which MU9C1485s are vertically cascaded using daisy-chaining of the flags is shown in Figure 1.

LOCKED DAISY-CHAIN

In a locked daisy chain, the highest priority device is the one with /MI HIGH and /MF LOW. Only this device will respond to command and data reads and writes, until the daisy chain has been unlocked by taking /EC HIGH in the next cycle of /E, with the exceptions noted in Table 5. This allows reading from the associated data field of the Highest-priority Match location anywhere in a string of devices, or the Match address from the Status register of the device with the match. It also permits updating the entry stored at the Highest-priority Match location.

Table 5 shows when a device will respond to reads or writes and when it won't based on the state of /EC (int), the internal match condition, and other control inputs. /EC is latched by the falling edge of /E. /EC(int) is registered from the latched /EC signal off the rising edge of /E, so it controls what happens in the next cycle, as shown in Figure 5. When /EC LOW is first taken in a string of WidePort LANCAM devices (and assuming the Device Select registers are set to FFFFH), all devices will respond to that command write or data write. (When DS=FFFFH, none of the devices will respond to a Command Read cycle or a

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Data Read cycle to prevent data bus contention. See Case 1 of Table 5.) The daisy-chain will remain locked in each subsequent cycle as long as /EC is held LOW on the falling edge of /E in the current cycle. When the daisy-chain is locked, only the Highest-priority Match device will respond (See Case 6 of Table 5). If, for example, all of the CAM memory locations were empty, there would be no match, and /MF would stay HIGH. Since none of the devices could then be the Highest-priority Match device, none will respond to reads or writes until the daisy chain is unlocked by taking /EC HIGH and asserting /E for a cycle.

If there is a match between the data in the Comparand register and a location or locations in memory, then only the Highest-priority Match device will respond to any cycle, such as an associated data or Status register read. If there isn't a match, then a NOP with /EC HIGH needs to be inserted before issuing any new instructions, such as Write to Next Free Address instruction to learn the data. Since Next Free operations are controlled by the /FI-/FF daisy-chain, only the device with the first empty location will respond. If an instruction is used to unlock the daisy-chain it will work only on the Highest-priority Match device, if one exists. If none exists, the instruction will have no effect except to unlock the daisy-chain. To read the Status registers of specific devices when there is no match requires the use of the TCO DS command to set DS=PA of each device. Single chip systems can tie /EC HIGH and just use the status register or /MA output to monitor match conditions, as the daisy chain lock-out feature is not needed in this configuration. This will alleviate the need for inserting an additional NOP in the case of a no-match condition.

Full Flag Cascading

The Full Flag daisy-chain cascading is used for three purposes: First, to allow instructions that address Next Free locations to operate globally, second, to provide a system wide Full flag, and third, to allow the loading of the Page Address registers during initialization using the SFF instruction. The full flag logic causes only the device containing the first empty location to respond to Next Free instructions such as "MOV NF,CR,V", which will move the contents of the Comparand register to the first empty location in a string of devices and set that location Valid, so it will be available for the next automatic compare. With devices connected as in Figure 1, the /FF output of the last device in a string provides a full indication for the entire string.

Match Flag Cascading

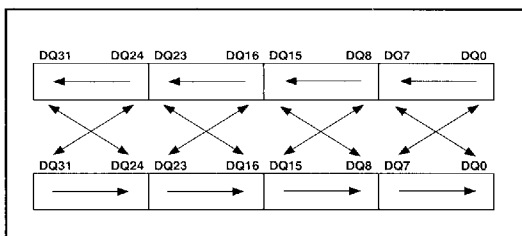


Figure 6: IEEE 802.3/802.5 Format Mapping

The Match Flag daisy-chain cascading is used for three purposes: First, to allow operations on Highest Priority Match addresses to operate globally over the whole string, second, to provide a system wide match flag, and third, to lock out all devices except the one with the Highest-priority match for instructions such as Status reads after a match. The Match flag logic causes only the highest priority device to operate on its Highest-priority Match location and lower priority devices to ignore operations on Highest-priority Match locations. With devices connected as in Figure 1, the /MF output of the last device provides a system match indication for the entire string. The lock-out feature is enabled by the match flag cascading and the use of the /EC control signal as shown in Table 5.

Global vs. Local Access for Cascaded Systems

The Device Select register controls access to devices in the daisy-chain once the Page Address registers have been initialized. Local access into a daisy-chained system works by sending a Device Select value to all Device Select registers which equals the Page Address of the target device, using the TCO DS instruction. Once this is done, only the device which has a match between its Page Address register and its Device Select register will respond to Read or Write cycles.

Loading the value "FFFFH" into the Device Select registers of a string will restore global access as shown in Table 5, with Read cycles being restricted to devices with the Highest-priority Match to eliminate bus contention.

IEEE 802.3/802.5 Format Mapping

To support the symmetrical mapping between the address formats of IEEE 802.3 and IEEE 802.5, the MU9C1485 provides a bit translation facility. Formally expressed, the nth input bit, D(n), maps to the xth output bit, Q(x), through the following expressions:

$$\begin{aligned} D(n) &= Q(7-n) \text{ for } 0 \leq n \leq 7, \\ D(n) &= Q(23-n) \text{ for } 8 \leq n \leq 15 \\ D(n) &= Q(39-n) \text{ for } 16 \leq n \leq 23 \end{aligned}$$

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OPERATIONAL CHARACTERISTICS (CONT'D)

Cycle Type	Opcode	Data Bus		Comments	Notes
		DQ31-16	DQ15-DQ0		
Command Write	TCO DS	0A28H	FFFFH	Target Device Select register and disable local device selection	
Command Write	TCO CT	0A00H	0000H	Target Control register and reset	1
Command Write	TCO PA	0A08H	nnnnH	Target Page Address register and set page for cascaded operation	2
Command Write	SFF	0700H	X	Set Full flag; allows access to next device (repeat previous cycle plus this one for each device in chain)	2
	•				
Command Write	TCO CT	0A00H	0000H	Target Control register and reset Full flags, but not Page Address.	1
Command Write	TCO CT	0A00H	8080H	Target Control register and give initial values	3,4
Command Write	TCO SC	0A10H	2808H	Target Segment Counter and set destination to only use upper seg. and source to only use lower seg.	4
Command Write	SPS M@HM	0005H	X	Set Persistent Source to Memory at the Highest Priority Match	5

Notes

1. Toggling the /RESET pin generates the same effect as this reset of the Control register, but good programming practice dictates a software reset for initialization to account for all possible conditions.
2. This instruction may be omitted for a single MU9C1485 application. The last SFF will cause the /FF pin in the last chip in a daisy chain to go LOW. In a daisy chain, DS needs to be set equal to PA to read out of a particular chip prior to a match condition.
3. Typical WidePort LANCAM control environment: Enable match flag; Enable full flag; 32 CAM bits/32 RAM bits; Disable comparison masking; and Enable address increment.
This example translates to 8080H. See Table 2 for Control register bit assignments.
4. Use Worksheet to help determine Segment Counter and Control register values.
5. Setting the persistent source to the Memory at Highest Priority match allows a compare operation followed by a read of associated data when a match is found. Note that the persistent destination is set to the Comparand register by the reset.

Table 9: Example Initialization Routine

$$D(n) = Q(55-n) \text{ for } 24 \leq n \leq 31$$

Setting Control register bits 10 and 9 selects whether to persistently translate, or persistently not to translate, the data written onto the 64-bit internal bus. The default condition after a Reset command is not to translate the incoming data. Figure 6 shows the bit mapping between the two formats.

INITIALIZING THE WidePort LANCAM

Initialization of the MU9C1485 is required to configure the various registers on the device. And since a Control register reset establishes the operating conditions shown in Table 2, restoration of operating

conditions better suited for the application may be required after a reset.

Setting Page Address Register Values

In a vertically cascaded system, the user must set the individual Page Address registers to unique values by using the Page Address initialization mechanism. Each Page Address register must contain a unique value to prevent bus contention. This process allows individual device selection. The Page Address register initialization works as follows: Writes to Page Address registers are only active for devices with /FI LOW and /FF HIGH. At initialization, all devices are empty, thus the top device in the string will respond to a TCO PA

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OPERATIONAL CHARACTERISTICS (CONT'D)

instruction, and load its PA register. To advance to the next device in the string, a Set Full Flag (SFF) instruction is used, which is also only active for the device with /FI LOW and /FF HIGH. The SFF instruction changes the first device's /FF to LOW, although the device really is empty, which allows the next device in the string to respond to the TCO PA instruction and load its PA register. The initialization proceeds through the chain in a similar manner filling all the PA registers in turn. Each device must have a unique Page Address value stored in its PA register, or contention will result. After all the PA registers are filled, the entire string is reset through the Control register, which does not change the values stored in the individual PA registers. After the reset, the Device Select registers are usually set to FFFFH to enable operation as shown in Case 1 of Table 5. The Control registers and the Segment Control registers are now also set to their normal operating values for the application.

Vertically Cascaded System Initialization

Table 9 shows an example of code that initializes a daisy-chained string of WidePort LANCAM devices. The Initialization example shows how to set the Page

Address registers of each of the devices in the chain through the use of the Set Full Flag instruction, and how the Control registers and Segment counters of all the WidePort LANCAM devices are set for a typical application. Each Page Address register must contain a unique value (not FFFFH) to prevent bus contention.

For typical daisy-chain operation, data are loaded into the Comparand registers of all the devices in a string simultaneously by setting DS=FFFFH. Since reading is prohibited when DS=FFFFH except for the device with a match, for a diagnostic operation you need to select a specific device by setting DS=PA for the desired device to be able to read from it. Refer to Table 5 for pre-conditions for reading and writing.

Initialization for a single WidePort LANCAM is similar. The Device Select register in this case is usually set to equal the Page Address register for normal operations. Also, the dedicated /MA flag output can be used instead of /MF, allowing /EC to be tied HIGH. This will disable the operation of the daisy-chain and eliminate the need to insert a NOP after a no-match, enhancing application performance.

INSTRUCTION SET DESCRIPTIONS

Instruction: Select Persistent Source (SPS)

Binary Op-Code: 0000 f000 0000 0sss*
f **Address Field Flag†**
sss **Selected Source**

This instruction selects a persistent source for Data Reads, which remains the source for Data Reads until another SPS instruction or a Reset occurs. The Comparand register is the default persistent source after the /RESET pin is asserted or after a software reset. SPS M@aaaH will load the Address register in preparation for the first access to the persistent source, and subsequent accesses will be with respect to the Address register.

Instruction: Select Persistent Destination (SPD)

Binary Op-Code: 0000 f001 mmdd dvvv*
f **Address Field Flag†**
mm **Mask Register Select**
ddd **Selected Destination**
vvv **Validity Setting for memory location destinations**

This instruction selects a persistent destination for Data Writes, which remains the destination for Data Writes until another SPD instruction or a Reset occurs. The Comparand register is the default destination for Data Writes after the /RESET pin is asserted or after a software reset. SPD M@aaaH will load the Address register in preparation for the first access to the persistent destination, and all subsequent accesses

will be with respect to the Address register. When the destination is the Comparand register or the Memory array, the writing of data may be masked by either Mask Register 1 or 2. In this case, only those bits in the destination that correspond to "0s" in the Mask register will be modified. An automatic compare will occur after writing to the Comparand or Mask registers, but not after writing to Memory.

Instruction: Temporary Command Override (TCO)

Binary Op-Code: 0000 f010 00dd d000*
f **Address Field Flag†**
ddd **Register selected as source or destination for only the next Command Read or Write cycle.**

The TCO instruction temporarily redirects the DQ bus for register access. If f=1, a register write will be performed with the data on DQ15-DQ0. If f=0, a subsequent command read can be used to read the register contents via DQ15-DQ0. During register reads, DQ31-DQ16 will contain the upper 16-bits of the Status register, except in the case of a Page Address register read where these bits are "0"s. After the access, subsequent Command Read or Write cycles revert to reading the Status register and writing to the Instruction decoder. All registers but the NF, PS and PD are available for write access. All registers are available for read access. The complete Status register is only available via non-TCO Command Read access.

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INSTRUCTION SET DESCRIPTIONS (CONT'D)

Instruction: Data Move (MOV)

Binary Op-Code: 0000 f011 mmdd dsss or
0000 f011 mmdd dvss*
f Address Field Flag†
mm Mask Register select
ddd Destination of Data
sss Source of Data
v Validity setting if destination is a memory location

The MOV instruction performs a 64-bit move of the data in the selected source to the selected destination. Data transfers between the Memory array and the Comparand register may be masked by either Mask Register 1 or Mask Register 2, in which case, only those bits in the destination which correspond to bits containing 0's in the selected Mask register will be changed. A Memory location used as a destination for a MOV instruction will be set to Valid or left unchanged, depending on the setting of the "v" bit. If the source and destination are the same register, no net change occurs (a NOP).

Instruction: Validity Bit Control (VBC)

Binary Op-Code: 0000 f100 00dd dvvv*
f Address Field Flag†
ddd Destination of data
vvv Validity setting for Memory location

The VBC instruction sets the Validity bits at the selected memory location to the selected state. This feature can be used in finding multiple matches, for

example, by using a repetitive sequence of CMP V through a Mask of all "1s", followed by a VBC HM, S.

Instruction: Compare (CMP)

Binary Op-Code: 0000 0101 0000 0vvv*
vvv Validity condition

A CMP V, S, or R instruction forces a Comparison of Valid, Skipped, or Random entries against the Comparand register through a Mask register, if one is selected. During a CMP E instruction, the compare is only done on the Validity bits and all data bits are automatically masked.

Instruction: Set Full Flag (SFF)

Binary Op-Code: 0000 0111 0000 0000*

The SFF instruction is a special instruction used to force the Full flag LOW to permit setting the Page Address register in vertically cascaded systems.

Notes:

§ Instruction cycle lengths given in Table 10.

* Instruction Op-Codes are loaded on the DQ31-DQ16 lines.

† If f=1, the instruction requires an absolute address (or register contents for TCOs) to be supplied on the DQ15-DQ0 lines. Supplied addresses will update the Address register to the "aaaH" value supplied. During instructions involving M@[AR] or M@aaaH, the Address register will be incremented or decremented depending on the setting in the Control register.

CYCLE LENGTH	CYCLE TYPE			
	Command Write	Command Read	Data Write	Data Read
Short	MOV reg, reg TCO reg (except CT) SPS SPD NOP		Comparand register (not last segment) Mask register (not last segment)	
Medium	MOV reg, mem TCO CT (reset) VBC (NF Address unresolved)	Status register or read register after TCO command	Memory Array (NF Address unresolved)	Comparand register Mask register
Long	MOV mem, reg TCO CT (non-reset) CMP SFF VBC (NF Address resolved)		Memory array (NF Address resolved) Comparand register (last segment) Mask register (last segment)	Memory array

Note: The specific timing requirements for Short, Medium and Long cycles are given in the Switching Characteristics section under the tELEH parameter.

Table 10: Instruction Cycle Lengths

6411817 0000446 20T

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INSTRUCTION SET SUMMARY

MNEMONIC FORMAT

INS dst,src[msk],val

INS: Instruction mnemonic.
dst: Destination of the data.
src: Source of the data.
msk: Mask register used.
val: Validity condition set at the location written.

Instruction: Select Persistent Source

Operation	Mnemonic	Op-Code
Comparand Register	SPS CR	0000H
Mask Register 1	SPS MR1	0001H
Mask Register 2	SPS MR2	0002H
Memory Array at Address Reg	SPS M@[AR]	0004H
Memory Array at Address	SPS M@aaaH	0804H
Memory at Highest-priority Match	SPS M@HM	0005H

Instruction: Select Persistent Destination

Operation	Mnemonic	Op-Code
Comparand Register	SPD CR	0100H
Masked by MR1	SPD CR[MR1]	0140H
Masked by MR2	SPD CR[MR2]	0180H
Mask Register 1	SPD MR1	0108H
Mask Register 2	SPD MR2	0110H
Memory at Address Reg set Valid	SPD M@[AR],V	0124H
Masked by MR1	SPD M@[AR][MR1],V	0164H
Masked by MR2	SPD M@[AR][MR2],V	01A4H
Memory at Address Reg set Empty	SPD M@[AR],E	0125H
Masked by MR1	SPD M@[AR][MR1],E	0165H
Masked by MR2	SPD M@[AR][MR2],E	01A5H
Memory at Address Reg set Skip	SPD M@[AR],S	0126H
Masked by MR1	SPD M@[AR][MR1],S	0166H
Masked by MR2	SPD M@[AR][MR2],S	01A6H
Memory at Address Reg set Random	SPD M@[AR],R	0127H
Masked by MR1	SPD M@[AR][MR1],R	0167H
Masked by MR2	SPD M@[AR][MR2],R	01A7H
Memory at Address set Valid	SPD M@aaaH,V	0924H
Masked by MR1	SPD M@aaaH[MR1],V	0964H
Masked by MR2	SPD M@aaaH[MR2],V	09A4H
Memory at Address set Empty	SPD M@aaaH,E	0925H
Masked by MR1	SPD M@aaaH[MR1],E	0965H
Masked by MR2	SPD M@aaaH[MR2],E	09A5H
Memory at Address set Skip	SPD M@aaaH,S	0926H
Masked by MR1	SPD M@aaaH[MR1],S	0966H
Masked by MR2	SPD M@aaaH[MR2],S	09A6H
Memory at Address set Random	SPD M@aaaH,R	0927H
Masked by MR1	SPD M@aaaH[MR1],R	0967H
Masked by MR2	SPD M@aaaH[MR2],R	09A7H
Memory at Highest-prio. Match, Valid	SPD M@HM,V	012CH
Masked by MR1	SPD M@HM[MR1],V	016CH
Masked by MR2	SPD M@HM[MR2],V	01ACH
Memory at Highest-prio. Match, Emp.	SPD M@HM,E	012DH
Masked by MR1	SPD M@HM[MR1],E	016DH
Masked by MR2	SPD M@HM[MR2],E	01ADH
Memory at Highest-prio. Match, Skip	SPD M@HM,S	012EH
Masked by MR1	SPD M@HM[MR1],S	016EH
Masked by MR2	SPD M@HM[MR2],S	01AEH

Instruction: Select Persistent Destination (Cont'd)

Operation	Mnemonic	Op-Code
Memory at High-prio. Match, Random	SPD M@HM,R	012FH
Masked by MR1	SPD M@HM[MR1],R	016FH
Masked by MR2	SPD M@HM[MR2],R	01AFH
Memory at Next Free Addr., Valid	SPD M@NF,V	0134H
Masked by MR1	SPD M@NF[MR1],V	0174H
Masked by MR2	SPD M@NF[MR2],V	01B4H
Memory at Next Free Addr., Empty	SPD M@NF,E	0135H
Masked by MR1	SPD M@NF[MR1],E	0175H
Masked by MR2	SPD M@NF[MR2],E	01B5H
Memory at Next Free Addr., Skip	SPD M@NF,S	0136H
Masked by MR1	SPD M@NF[MR1],S	0176H
Masked by MR2	SPD M@NF[MR2],S	01B6H
Memory at Next Free Addr., Random	SPD M@NF,R	0137H
Masked by MR1	SPD M@NF[MR1],R	0177H
Masked by MR2	SPD M@NF[MR2],R	01B7H

Instruction: Temporary Command Override

Operation	Mnemonic	Op-Code
Control Register	TCO CT	0n00H*
Page Address Register	TCO PA	0n08H*
Segment Control Register	TCO SC	0n10H*
Read Next Free Address	TCO NF	0218H
Address Register	TCO AR	0n20H*
Device Select Register	TCO DS	0n28H*
Read Persistent Source	TCO PS	0230H
Read Persistent Destination	TCO PD	0238H

*Note: n = 2 for register read access, n = A for register write access

Instruction: Data Move

Operation	Mnemonic	Op-Code
Comparand Register from:		
No Operation	NOP	0300H
Mask Register 1	MOV CR,MR1	0301H
Mask Register 2	MOV CR,MR2	0302H
Memory at Address Reg	MOV CR,[AR]	0304H
Masked by MR1	MOV CR,[AR][MR1]	0344H
Masked by MR2	MOV CR,[AR][MR2]	0384H
Memory at Address	MOV CR,aaaH	0B04H
Masked by MR1	MOV CR,aaaH[MR1]	0B44H
Masked by MR2	MOV CR,aaaH[MR2]	0B84H
Memory at Highest-prio Match	MOV CR,HM	0305H
Masked by MR1	MOV CR,HM[MR1]	0345H
Masked by MR2	MOV CR,HM[MR2]	0385H
Mask Register 1 from:		
Comparand Register	MOV MR1,CR	0308H
No Operation	NOP	0309H
Mask Register 2	MOV MR1,MR2	030AH
Memory at Address Reg	MOV MR1,[AR]	030CH
Memory at Address	MOV MR1,aaaH	0B0CH
Memory at Highest-prio Match	MOV MR1,HM	030DH
Mask Register 2 from:		
Comparand Register	MOV MR2,CR	0310H
Mask Register 1	MOV MR2,MR1	0311H
No Operation	NOP	0312H
Memory at Address Reg	MOV MR2,[AR]	0314H
Memory at Address	MOV MR2,aaaH	0B14H
Memory at Highest-prio Match	MOV MR2,HM	0315H

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INSTRUCTION SET SUMMARY (CONT'D)

Instruction: Data Move (Cont'd)

Operation	Mnemonic	Op-Code
Memory at Address Register, No Change to Validity bits, from:		
Comparand Register	MOV [AR],CR	0320H
Masked by MR1	MOV [AR],CR[MR1]	0360H
Masked by MR2	MOV [AR],CR[MR2]	03A0H
Mask Register 1	MOV [AR],MR1	0321H
Mask Register 2	MOV [AR],MR2	0322H
Memory at Address Register, Location set Valid, from:		
Comparand Register	MOV [AR],CR,V	0324H
Masked by MR1	MOV [AR],CR[MR1],V	0364H
Masked by MR2	MOV [AR],CR[MR2],V	03A4H
Mask Register 1	MOV [AR],MR1,V	0325H
Mask Register 2	MOV [AR],MR2,V	0326H
Memory at Address, No Change to Validity bits, from:		
Comparand Register	MOV aaaH,CR	0B20H
Masked by MR1	MOV aaaH,CR[MR1]	0B60H
Masked by MR2	MOV aaaH,CR[MR2]	0BA0H
Mask Register 1	MOV aaaH,MR1	0B21H
Mask Register 2	MOV aaaH,MR2	0B22H
Memory at Address, Location set Valid, from:		
Comparand Register	MOV aaaH,CR,V	0B24H
Masked by MR1	MOV aaaH,CR[MR1],V	0B64H
Masked by MR2	MOV aaaH,CR[MR2],V	0BA4H
Mask Register 1	MOV aaaH,MR1,V	0B25H
Mask Register 2	MOV aaaH,MR2,V	0B26H
Memory at Highest-priority Match, No Change to Validity bits, from:		
Comparand Register	MOV HM,CR	0328H
Masked by MR1	MOV HM,CR[MR1]	0368H
Masked by MR2	MOV HM,CR[MR2]	03A8H
Mask Register 1	MOV HM,MR1	0329H
Mask Register 2	MOV HM,MR2	032AH
Memory at Highest-priority Match, Location set Valid, from:		
Comparand Register	MOV HM,CR,V	032CH
Masked by MR1	MOV HM,CR[MR1],V	036CH
Masked by MR2	MOV HM,CR[MR2],V	03ACH
Mask Register 1	MOV HM,MR1,V	032DH
Mask Register 2	MOV HM,MR2,V	032EH
Memory at Next Free Address, No Change to Validity bits, from:		
Comparand Register	MOV NF,CR	0330H
Masked by MR1	MOV NF,CR[MR1]	0370H
Masked by MR2	MOV NF,CR[MR2]	03B0H
Mask Register 1	MOV NF,MR1	0331H
Mask Register 2	MOV NF,MR2	0332H

Instruction: Data Move (Cont'd)

Operation	Mnemonic	Op-Code
Memory at Next Free Address, Location set Valid, from:		
Comparand Register	MOV NF,CR,V	0334H
Masked by MR1	MOV NF,CR[MR1],V	0374H
Masked by MR2	MOV NF,CR[MR2],V	03B4H
Mask Register 1	MOV NF,MR1,V	0335H
Mask Register 2	MOV NF,MR2,V	0336H

Instruction: Validity Bit Control

Operation	Mnemonic	Op-Code
Set Validity bits at Address Register		
Set Valid	VBC [AR],V	0424H
Set Empty	VBC [AR],E	0425H
Set Skip	VBC [AR],S	0426H
Set Random Access	VBC [AR],R	0427H
Set Validity bits at Address		
Set Valid	VBC aaaH,V	0C24H
Set Empty	VBC aaaH,E	0C25H
Set Skip	VBC aaaH,S	0C26H
Set Random Access	VBC aaaH,R	0C27H
Set Validity bits at Highest-priority Match		
Set Valid	VBC HM,V	042CH
Set Empty	VBC HM,E	042DH
Set Skip	VBC HM,S	042EH
Set Random Access	VBC HM,R	042FH
Set Validity bits at All Matching Locations		
Set Valid	VBC ALM,V	043CH
Set Empty	VBC ALM,E	043DH
Set Skip	VBC ALM,S	043EH
Set Random Access	VBC ALM,R	043FH

Instruction: Compare

Operation	Mnemonic	Op-Code
Compare Valid Locations	CMP V	0504H
Compare Empty Locations	CMP E	0505H
Compare Skipped Locations	CMP S	0506H
Compare Random Access Locations	CMP R	0507H

Instruction: Special Instructions

Operation	Mnemonic	Op-Code
Set Full Flag	SFF	0700H

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5 to 7.0 Volts
Voltage on all Other Pins	-0.5 to VCC+0.5 Volts (-2.0 Volts for 10 ns, measured at the 50% point)
Temperature Under Bias	-40°C to +85°C
Storage Temperature	-55°C to +125°C
DC Output Current	20 mA (per Output, one at a time, one second duration)

Stresses exceeding those listed under Absolute Maximum Ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

All voltages are referenced to GND.

OPERATING CONDITIONS (voltages referenced to GND at the device pin)

Symbol	Parameter	Min	Typical	Max	Units	Notes
V _{CC}	Operating Supply Voltage	4.75	5.0	5.25	Volts	
V _{IH}	Input Voltage Logic "1"	2.2		V _{CC} +0.5	Volts	
V _{IL}	Input Voltage Logic "0"	-0.5		0.8	Volts	1, 2
T _A	Ambient Operating Temperature	0		70	°C	Still Air

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typical	Max	Units	Notes
I _{CC}	Average Power Supply Current		150	275	mA	3
I _{CC} (SB)	Stand-by Power Supply Current		TBD		mA	E = HIGH
V _{OH}	Output Voltage Logic "1"	2.4			Volts	I _{OH} = -2.0 mA
V _{OL}	Output Voltage Logic "0"			0.4	Volts	I _{OL} = 4.0 mA
I _{Iz}	Input Leakage Current	-2		2	μA	V _{SS} ≤ V _{IN} ≤ V _{CC}
I _{OZ}	Output Leakage Current	-10		10	μA	V _{SS} ≤ V _{OUT} ≤ V _{CC} ; DQ _n = High Impedance

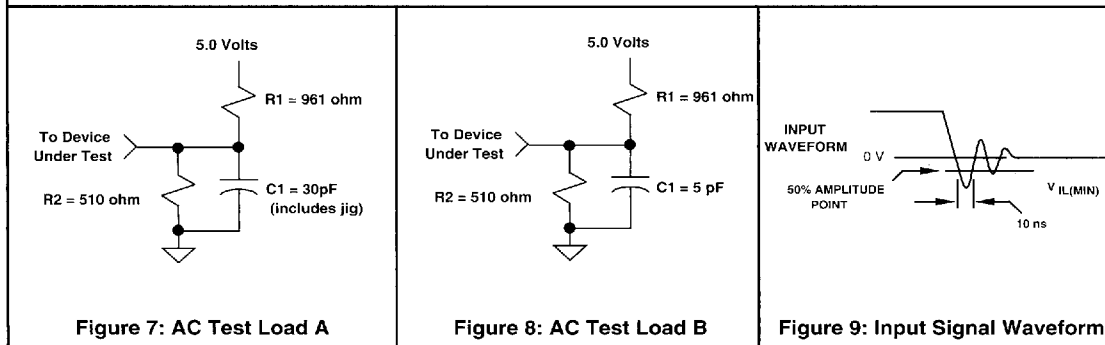
CAPACITANCE

Symbol	Parameter	Max	Units	Notes
C _{IN}	Input Capacitance	6	pF	f = 1 MHz, V _{IN} = 0 V.
C _{OUT}	Output Capacitance	7	pF	f = 1 MHz, V _{OUT} = 0 V.

AC TEST CONDITIONS

Input Signal Transitions	0.0 to 3.0 volts
Input Signal Rise Time	< 3 ns
Input Signal Fall Time	< 3 ns
Input Timing Reference Level	1.5 volts
Output Timing Reference Level	1.5 volts

SWITCHING TEST FIGURES



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SWITCHING CHARACTERISTICS (see Note 3)						
No	Symbol	Parameter (all times in nanoseconds)	-90		-12	
			Min	Max	Min	Max
1	tELEL	Chip Enable Compare Cycle Time	90		120	
2	tELEH	Chip Enable LOW Pulse Width				
		Short Cycle:	25		35	4
		Medium Cycle:	50		75	5
		Long Cycle:	75		100	6
3	tEHEL	Chip Enable HIGH Pulse Width	15		20	
4	tCVEL	Control Input to Chip Enable LOW Set-up Time	0		0	9
5	tELCX	Control Input from Chip Enable LOW Hold Time	10		15	9
6	tELQX	Chip Enable LOW to Outputs Active	3		3	10
7	tELQV	Chip Enable LOW to Outputs Valid		50		70
				75		85
8	tEHQZ	Chip Enable HIGH to Outputs High-Z	3	15	3	20
9	tDVEL	Data to Chip Enable LOW Set-up Time	0		0	
10	tELDX	Data from Chip Enable LOW Hold Time	10		15	
11	tFIVEL	Full In Valid to Chip Enable LOW Set-up Time	0		0	
12	tFIVFFV	Full In Valid to Full Flag Valid		7		8
13	tELFFV	Chip Enable LOW to Full Flag Valid		75		90
14	tMIVEL	Match In Valid to Chip Enable LOW Set-up Time	0		0	
15	tEHMFV	Chip Enable HIGH to /MF, /MA, /MM Invalid	0		0	
16	tMIVMFV	Match In Valid to /MF Valid		7		8
17	tEHMFV	Chip Enable HIGH to /MF, /MA, /MM Valid		25		30
18	tRLRH	Reset LOW Pulse Width	100		100	

NOTES

- 1.0V for a duration of 10 ns measured at the 50% amplitude points for Input-only lines (Figure 9).
- Common I/O lines are clamped, so that signal transients cannot fall below -0.5V.
- Maximum ICC references a sequence of two memory reads followed by a non-matching compare with tELEL=tELEL (minimum). Typical ICC references a nominal operation sequence which includes matching and non-matching compares, data writes and memory reads with tELEH=tEHEL=tELEH (minimum).
- Applies to a Data Write to the Comparand or Mask registers (without a Compare), or a Command Write to a Register (except a Control register Reset), a TCO instruction (i.e. single cycle TCO register write, or first of two cycle TCO register read), or a MOV between registers (e.g., a NOP).
- Applies to a Command Write of a VBC instruction (NF Address unresolved), a MOV to the Comparand or Mask registers from Memory, or a Control register Reset, a Command Read from a register (i.e. a Status register read or second cycle of TCO register read), a Data Read from the Comparand or Mask registers, or a Data Write to Memory (NF Address unresolved).
- Applies to any Compare Cycle (a Data Write to the last segment of the Comparand or Mask registers, a Command Write of a CMP instruction or a non-resetting value to the Control register), a Data Read from Memory, a Data Write to Memory (NF Address resolved), a Command Write of a SFF instruction, a VBC instruction (NF Address resolved), or a MOV to Memory from the Comparand or Mask registers.
- Applies to a Command Read from a register (e.g., a Status Read), or a Data Read from the Comparand or Mask registers.
- Applies to a Data Read from Memory.
- Control signals are /W, /CM and /EC.
- With load specified in Figure 7.
- With load specified in Figure 8.

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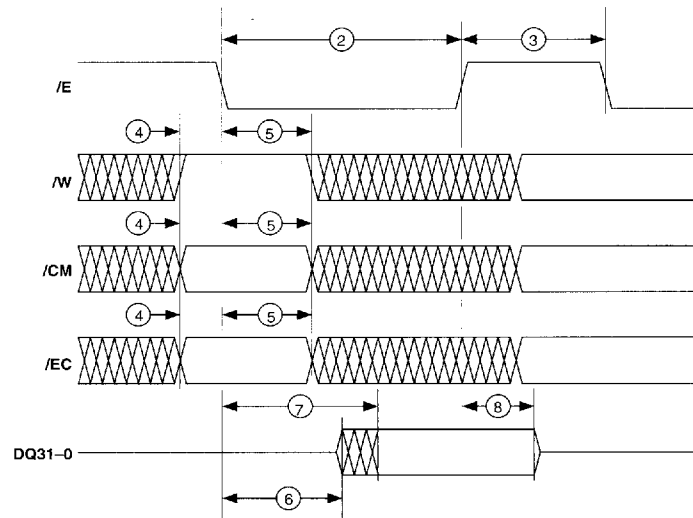
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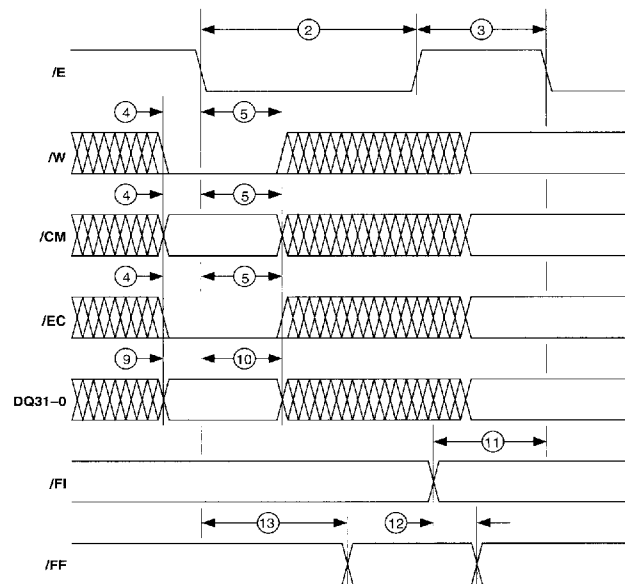
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TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE

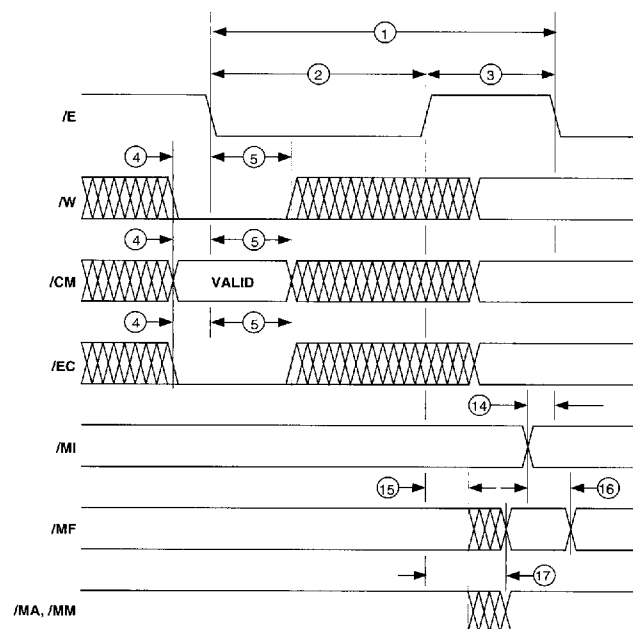


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TIMING DIAGRAMS (CONT'D)

COMPARE CYCLE



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BINARY															
CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Match Flag		Full Flag		Translation		CAM/RAM Partitioning		Masking		Address Inc/Dec					
Enable ="00"		Enable ="00"		Input Not Translated ="00"		64 CAM ="000"		Off ="00"		Increment ="00"					
Disable ="01"		Disable ="01"		Input Translated ="01"		48 CAM ="001"		MR1 ="01"		Decrement ="01"					
No change ="11"		No change ="11"		No Change ="11"		32 CAM ="010"		MR2 ="10"		Disable ="10"					
						16 CAM ="011"		No change ="11"		No change ="11"					
						0 CAM ="100"									
						No Change ="111"									
HEXADECIMAL															
[]				[]				[]				[]			
CONTROL REGISTER															

BINARY																			
SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0				
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
Set Dest. Seg. Limits ="0"		Dest. Count Start Limit		Dest. Count End Limit		Set Src. Seg. Limits ="0"		Src. Count Start Limit		Src. Count End Limit		Load Dest. Seg. Count ="0"		Dest. Seg. Count Value		Load Src. Seg. Count ="0"		Src. Seg. Count Value	
No Chng. ="1"						No Chng. ="1"						No Chng. ="1"				No Chng. ="1"			
HEXADECIMAL																			
[]				[]				[]				[]							
SEGMENT CONTROL REGISTER																			

BINARY	HEX	BINARY	HEX	BINARY	HEX	BINARY	HEX
0000	0	0100	4	1000	8	1100	C
0001	1	0101	5	1001	9	1101	D
0010	2	0110	6	1010	A	1110	E
0011	3	0111	7	1011	B	1111	F

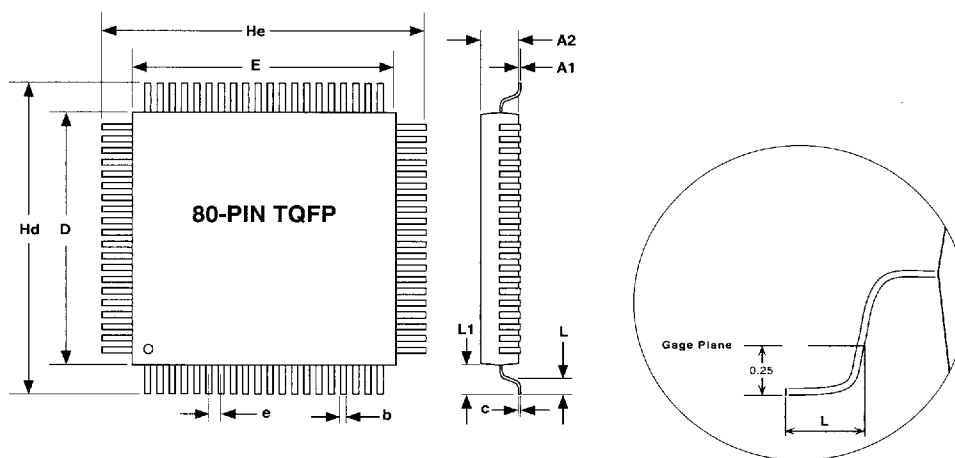
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ORDERING INFORMATION

PART NUMBER	CYCLE TIME	PACKAGE	TEMPERATURE RANGE
MU9C1485-90TCC	90ns	80-PIN TQFP	0-70°C
MU9C1485-12TCC	120ns	80-PIN TQFP	0-70°C

PACKAGE OUTLINE



Dimensions are in mm.

Lead Count	Dim. A1	Dim. A2	Dim. b	Dim. c	Dim. D	Dim. E	Dim. e	Dim. Hd	Dim. He	Dim. L	Dim. L1
80	0.05 0.15	1.35 1.45	0.22 0.38	0.08 0.20	13.90 14.10	13.90 14.10	0.65 nom	15.90 16.10	15.90 16.10	0.45 0.75	1.00 nom

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