MPC2004
MPC2005

Advance Information

256KB and 512KB BurstRAM™ Secondary Cache Modules for PowerPC™ PReP/CHRP Platforms

The MPC2004 and MPC2005 are designed to provide burstable, high performance 256KB/512KB L2 cache for the PowerPC 60x microprocessor family in conformance with the PowerPC Reference Platform (PReP) and the PowerPC Common Hardware Reference Platform (CHRP) specifications. The modules are configured as 32K x 72 and 64K x 72 bits in a 182 (91 x 2) pin DIMM format. Each module uses four of Motorola's 5 V 32K x 18 or 64K x 18 BurstRAMs and a 5 V cache tag RAM configured as 16K x 12 for tag field plus 16K x 2 for valid and dirty status bits.

Bursts can be initiated with the $\overline{\text{SRAMADS}}$ signal. Subsequent burst addresses are generated internal to the BurstRAM by the $\overline{\text{SRAMCNTEN}}$ signal.

Write cycles are internally self timed and are initiated by the rising edge of the clock (CLKx) inputs. Eight write enables are provided for byte write control.

Presence detect pins are available for auto configuration of the cache control. A serial EEPROM is optional to provide more in–depth description of the cache module.

The module family pinout will support 5 V and 3.3 V components for a clear path to lower voltage and power savings. Both power supplies must be connected.

These cache modules are plug and pin compatible with the MPC2006, a 1MB synchronous module also designed for the PReP and CHRP specifications. They are also compatible with the MPC2007 and MPC2009, 256KB and 1MB respectively, asynchronous cache modules.

- PowerPC–style Burst Counter on Chip
- Flow–Through Data I/O
- Module Requires Both 3.3 V and 5 V Power Supplies
- Multiple Clock Pins for Reduced Loading
- All Cache Data and Tag I/Os are LVTTL (3.3 V) Compatible
- Three State Outputs
- Byte Write Capability
- Fast Module Clock Rates: 66 MHz
- Fast SRAM Access Times: 10 ns for Tag RAM Match
9 ns for Data RAM
- Decoupling Capacitors for Each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- 182 Pin Card Edge Module
- Burndy Connector, Part Number: ELF182JSC–3Z50

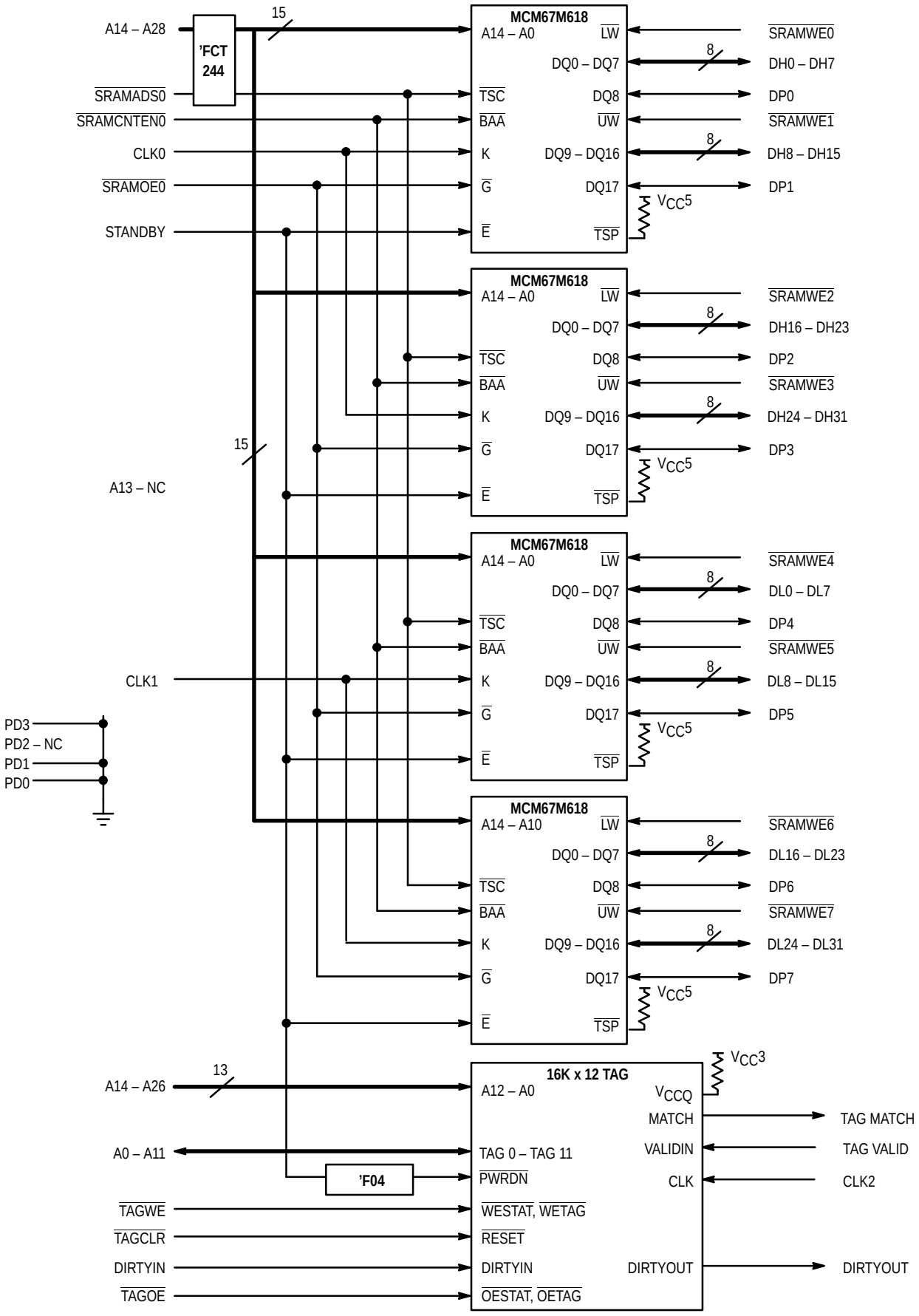
5/95

PIN ASSIGNMENT
182–LEAD DIMM
TOP VIEW – CASE TBD

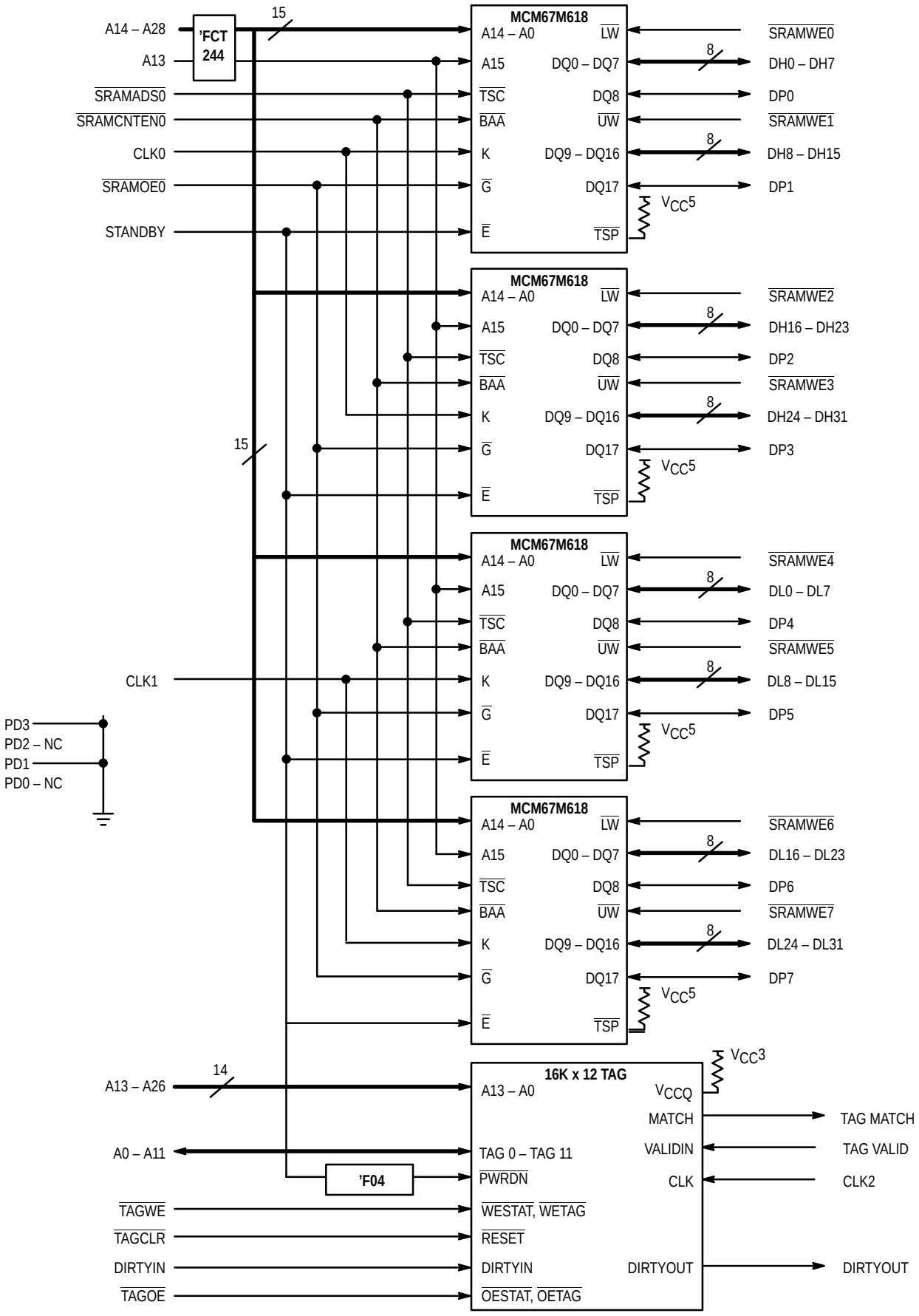
GND	92	1	GND
PD1/IDSDATA	93	2	PD0/IDSCLK
PD3	94	3	PD2
DH31	95	4	DH30
DH29	96	5	DH28
DH27	97	6	DH26
DH25	98	7	DH24
$V_{CC}3$	99	8	$V_{CC}3$
$\overline{\text{SRAMWE3}}$	100	9	DP3
DH23	101	10	DH22
DH21	102	11	DH20
DH18	103	12	DH19
GND	104	13	GND
DH16	105	14	DH17
$\overline{\text{SRAMWE2}}$	106	15	DP2
DH14	107	16	DH15
DH13	108	17	DH12
$V_{CC}5$	109	18	$V_{CC}5$
DH10	110	19	DH11
DH8	111	20	DH9
$\overline{\text{SRAMWE1}}$	112	21	DP1
DH6	113	22	DH7
$V_{CC}3$	114	23	$V_{CC}3$
DH4	115	24	DH5
GND	116	25	DH3
CLK0	117	26	DH2
GND	118	27	DH0
DH1	119	28	DP0
$\overline{\text{SRAMWE0}}$	120	29	GND
DL31	121	30	CLK1
DL30	122	31	GND
GND	123	32	DL28
DL29	124	33	DL26
DL27	125	34	DL24
DL25	126	35	DP7
$V_{CC}5$	127	36	$V_{CC}5$
$\overline{\text{SRAMWE7}}$	128	37	DL22
DL23	129	38	DL20
DL21	130	39	DL18
DL19	131	40	DL16
GND	132	41	GND
DL17	133	42	DP6
$\overline{\text{SRAMWE6}}$	134	43	DL14
DL15	135	44	DL12
DL13	136	45	DL11
GND	137	46	GND
DL10	138	47	DL9
DL8	139	48	DP5
$\overline{\text{SRAMWE5}}$	140	49	DL7
DL6	141	50	DL4
$V_{CC}3$	142	51	$V_{CC}3$
DL5	143	52	DL3
DL2	144	53	DL1
GND	145	54	DL0
(CLK3) NC	146	55	GND
GND	147	56	CLK2
(CLK4) NC	148	57	GND
GND	149	58	DP4
$\overline{\text{SRAMWE4}}$	150	59	$\overline{\text{SRAMOE0}}$
(SRAMALE) NC	151	60	NC ($\overline{\text{SRAMOE1}}$)
$V_{CC}3$	152	61	$V_{CC}3$
(ADDR1A) NC	153	62	NC (ADDR0A)
(ADDR1B) NC	154	63	NC (ADDR0B)
$\overline{\text{SRAMCNTEN0}}$	155	64	$\overline{\text{SRAMADS0}}$
($\overline{\text{SRAMCNTEN1}}$) NC	156	65	NC ($\overline{\text{SRAMADS1}}$)
$V_{CC}5$	157	66	$V_{CC}5$
$V_{CC}5$	158	67	$V_{CC}5$
A27	159	68	A28
A24	160	69	A26
A22	161	70	A25
A20	162	71	A23
GND	163	72	GND
A18	164	73	A21
A16	165	74	A19
A15	166	75	A17
A14	167	76	A13 (See Note 1)
$V_{CC}3$	168	77	$V_{CC}3$
A10	169	78	NC (A12)
A8	170	79	A11
A6	171	80	A9
GND	172	81	GND
A4	173	82	A7
A2	174	83	A5
A1	175	84	A3
RESERVED	176	85	A0
$V_{CC}5$	177	86	$V_{CC}5$
TAG VALID	178	87	$\overline{\text{TAGCLR}}$
$\overline{\text{TAGWE}}$	179	88	TAG MATCH
STANDBY	180	89	$\overline{\text{TAGOE}}$
DIRTYOUT	181	90	DIRTYIN
GND	182	91	GND

NOTES:
1. This pin on the MPC2004 is a No Connect (NC).
2. Signal names in (parentheses) are NC on MPC2004 and MPC2005, but are actual signals on other modules in the MPC200x family.
3. All power pins ($V_{CC}5$, $V_{CC}3$) must be connected to appropriate supplies.

MPC2004 (32K x 72) BurstRAM MEMORY BLOCK DIAGRAM



MPC2005 (64K x 72) BurstRAM MODULE BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
68, 69, 70, 71, 73, 74, 75, 76, 78, 79, 80, 82, 83, 84, 85, 159, 160, 161, 162, 164, 165, 166, 167, 169, 170, 171, 173, 174, 175	A0 – A28	Input	Address Inputs – (MSB:0, LSB:28)
62, 63	ADDR0A, ADDR0B	Input	Least significant address bit when asynchronous SRAMs are used.
153, 154	ADDR1A, ADDR1B	Input	Next to least significant address bit when asynchronous SRAMs are used.
30, 56, 117, 146, 148	CLK0 – CLK4	Input	Clock Inputs – CLK2 is for Tag RAM, CLK0, 1, 3, and 4 are for SRAMs. For 1MB use all the clocks. For 512KB or less us CLK0–CLK2 only.
4, 5, 6, 7, 10, 11, 12, 14, 16, 17, 19, 20, 22, 24, 25, 26, 27, 95, 96, 97, 98, 101, 102, 103, 105, 107, 108, 110, 111, 113, 115, 119	DH0 – DH31	I/O	High Data Bus – (MSB:0, LSB:31)
32, 33, 34, 37, 38, 39, 40, 43, 44, 45, 47, 49, 50, 52, 53, 54, 121, 122, 124, 125, 126, 129, 130, 131, 133, 135, 136, 138, 139, 141, 143, 144	DL0 – DL31	I/O	Low Data Bus – (MSB:0, LSB:31)
9, 15, 21, 28, 35, 42, 48, 58	DP0 – DP7	I/O	Data Parity Bus – (MSB:0, LSB:7)
3, 94	PD2, PD3	Output	Presence detect bits 2 and 3.
2	PD0/IDSCLK	Input	Presence detect bit 0/EEPROM serial clock.
93	PD1/IDSDATA	I/O	Presence detect bit 1/EEPROM serial data.
64, 65	$\overline{\text{SRAMADS0}}$, $\overline{\text{SRAMADS1}}$	Input	SRAM Address Strobe – For 512KB or less us $\overline{\text{SRAM}}$ $\overline{\text{ADS0}}$ only.
151	SRAM ALE	Input	SRAM Address Latch Enable – Use for asynchronous SRAM only.
155, 156	$\overline{\text{SRAMCNTEN0}}$, $\overline{\text{SRAMCNTEN1}}$	Input	SRAM Count Enables – For 512KB or less use $\overline{\text{SRAM}}$ $\overline{\text{CNT}}$ $\overline{\text{EN0}}$ only.
59, 60	$\overline{\text{SRAMOE0}}$, $\overline{\text{SRAMOE1}}$	Input	SRAM Output Enables – For 512KB or less use $\overline{\text{SRAM}}$ $\overline{\text{OE0}}$ only.
100, 106, 112, 120, 128, 134, 140, 150	$\overline{\text{SRAMWE0}}$ – $\overline{\text{SRAMWE7}}$	Input	SRAM Write Enables – (MSB:0, LSB:7)
87	$\overline{\text{TAGCLR}}$	Input	Tag RAM clear.
88	TAG MATCH	Output	Tag RAM match indication.
178	TAG VALID	Input	Tag RAM valid bit.
179	$\overline{\text{TAGWE}}$	Input	Tag RAM write enable.
89	$\overline{\text{TAGOE}}$	Input	Tag RAM output enable.
90	DIRTYIN	Input	Dirty input bit.
181	DIRTYOUT	Output	Dirty output bit.
180	STANDBY	Input	Standby pin. Reduces standby power consumption.
176	RESERVED		Reserved pin.
8, 23, 51, 61, 77, 99, 114, 142, 152, 168	$V_{CC}3$	Input	+ 3.3 V power supply.

Pin Locations	Symbol	Type	Description
18, 36, 66, 67, 86, 109, 127, 157, 158, 177	$V_{CC}5$	Input	+ 5 V power supply.
1, 13, 29, 31, 41, 46, 55, 57, 72, 81, 91, 92, 104, 116, 118, 123, 132, 137, 145, 147, 149, 163, 172, 182	GND	Input	Ground

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