MICRONAS

DA3120.000

MAS3120

MICROPROCESSOR–COMPATIBLE 12–BIT MDAC

DESCRIPTION

The MAS3120 is a 12–bit monolithic CMOS multiplying digital–to–analog converter where excellent linearity is achieved without laser trimming. The DAC features internal matched feedback resistors both for unipolar and bipolar operation and a decoded DAC architecture.

The MAS3120 has been designed for great flexibility in connecting to bus oriented systems. The 12 data inputs are organized into 3 independent addressable 4–bit input registers such that the MAS3120 can be connected to either a 4, 8 or 16–bit data bus. The 12–bit DAC register that follows the input registers is updated by taking LDAC high.

The MAS3120 is speed compatible with most microprocessors and it accepts TTL and 5V CMOS logic level inputs. It is offered in temperature range: −25°C to +85°C. The MAS3120 is packaged in a 28–pin PDIP packages and is also available in die form.

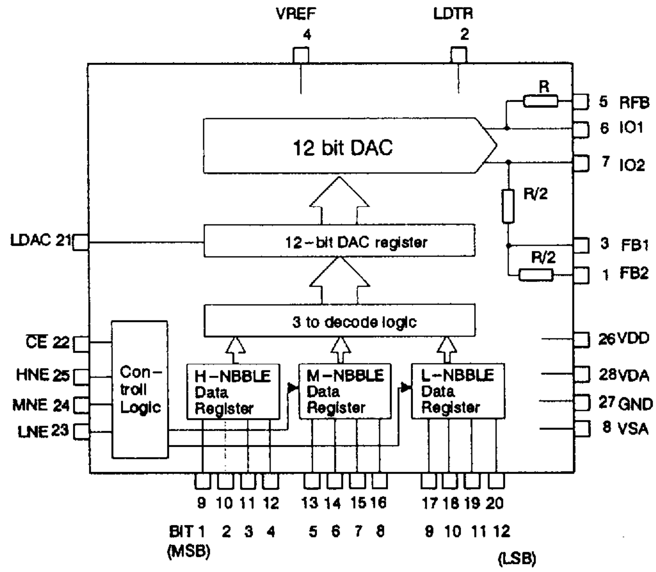
FEATURES

- 12–bit linearity over full temperature range
- No laser trimming
- Monolithic CMOS construction
- Double–Buffered digital inputs
- High stability
- All 4096 codes tested
- Direct replacement for HS3120 and MP7622
- 28–pin PDIP

APPLICATION

- µp–based control systems
- Bus structured instrumentation
- Process and industrial controllers

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

VDD=+15V, VREF=10V, GND = VSA = IO2 = FB1 = FB2 = LDTR = 0V, Unipolar unless otherwise specified.

		Ta=+25°C			Tmin−Tmax		
Parameter	Symbol	MIN	TYP	MAX	Limits	Units	Test Conditions/Comments
STATIC PERFORMANCE							
Resolution	N	12			12	Bits	
Integral Nonlinearity[1]	INL			±1/2	±1/2	LSB	Relative accuracy 12 bits
Differential Nonlinearity[2]	DNL			±1	±1	LSB	Monotonic to 12 bits
Gain error	Gfse			±6	±6	LSB	Measured Using Internal Rfb DAC Register Loaded With All 1's
Output Leakage Current	Ilkg			10	50	nA	
at IO1 (pin 6)				10	50	nA	
TEMPERATURE STABILITY							
Gain error TC	TCGfse				±2.0	ppm/°C	
Integral Nonlinearity TC	TCINL				±0.2	ppm/°C	
Differential Nonlinearity TC	TCDNL				±0.2	ppm/°C	
REFERENCE INPUT							
Input Resistance	Rref	5	8	12		kΩ	
Voltage Range[3]					±25	V	
DIGITAL INPUTS							Unipolar Coding: Binary
Input High Voltage	VIH	2.4		VDD	2.4	V	Bipolar Coding: Offset Binary
Input Low Voltage	VIL	−0.3		0.8	0.8	V	
Input Current[4]	Iin			±1	±10	μA	
Input Capacitance[3]	Cin			8	8	pF	
SWITCHING CHARACTERISTICS							
Strobe Width	t_{SW}	60	40		90	ns	LDAC, $\overline{CE}$, HNE, MNE, LNE inputs
Data Setup Time	t_{DS}	60	40		90	ns	BIT1−BIT12
Data Hold Time	t_{DH}	40	30		60	ns	BIT1−BIT12
POWER SUPPLY							
Voltage Range	VDD	+5	+15	+16		V	Accuracy guaranteed only at +15V
Supply Current	IDD		2.0	2.5	2.5	mA	VIN <0.8V or >3.5V
	IDD		0.2	0.5	0.5	mA	VIN=0V or >5V
TEMPERATURE RANGE		−25		+85		°C	

NOTES:
1. End−Point linearity.
2. Differential Nonlinearity DNL is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.
3. Guaranteed by design but not production tested.
4. Logic inputs are MOS gates. Iin typical is less than 1 nA at 25°C.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are subject to sample testing only.
VDD=+15V, VREF=10V, IO1=IO2=AGND=0V except where stated. Output Amp is HOS−050.

		Ta=+25°C			Tmin−Tmax		
Parameter	Symbol	Min	TYP	MAX	Limits	Units	Test Conditions/Comments
PROPAGATION DELAY From bits input From $\overline{CE}$ From LDAC	t_{PD}		 150 150 100			 ns ns ns	IO1 load R=100Ω, Cext=13pF All Data Inputs 0V to VDD or VDD to 0V From 50% digital input change to 90% of final analog output.
CURRENT SETTLING TIME Major Code Transition Full Scale Transition	ts		 1.0 2.0			 us us	Settling to+/−0.012% FSR (strobed). 011111111111 to 100000000000 or 100000000000 to 011111111111 All Data Inputs 0V to VDD or VDD to 0V
OUTPUT CAPACITANCE CIO1 (Pin 6) CIO2 (Pin 7) CIO1 (Pin 6) CIO2 (Pin 7)	Co		 53 10 21 46			 pF pF pF pF	 Digital inputs VIH Digital inputs VIH Digital inputs VIL Digital inputs VIL
DIGITAL TO ANALOG GLITCH ENERGY	Q		20 200			nVs nVs	VREF = 0V; Data Latched VREF = 0V; Data not Latched
MULTIPLYING FEEDTHROUGH ERROR AT IO1	FT		2.0 0.2			mVpp mVpp	VREF= 20Vpp; f=10kHz sine wave VREF=20Vpp, f=1kHz sine wave
POWER SUPPLY REJECTION RATIO	PSRR		±0.002			%/%	VDD = 14 to 16V

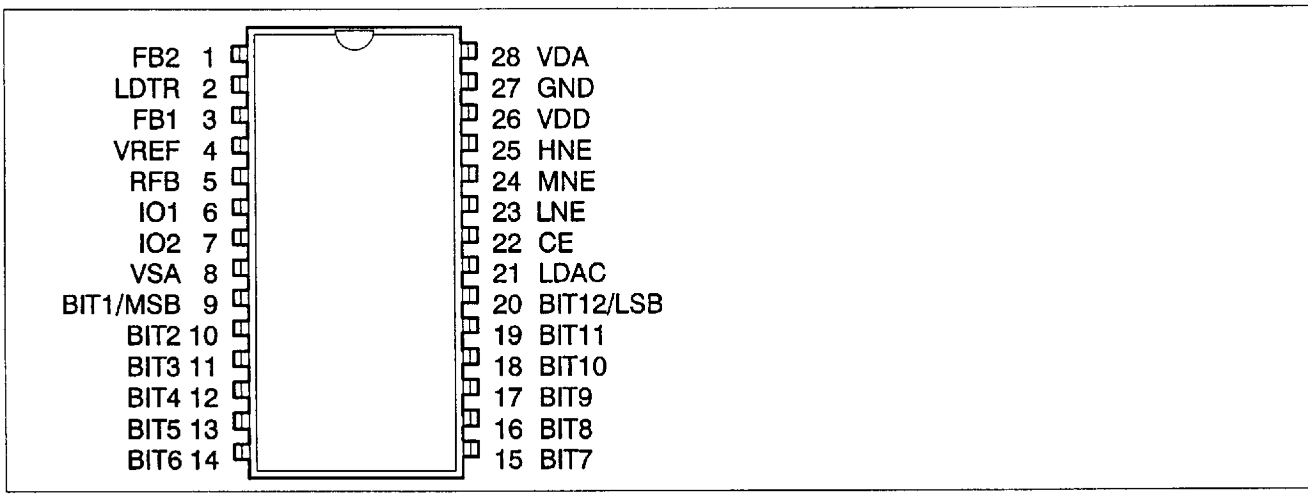
ABSOLUTE MAXIMUM RATINGS

(TA=25°C unless otherwise noted)

VDD to GND .... −0.3V, +17V
Digital Input Voltage to GND .... −0.3V, VDD +0.3V
VREF or RFB to GND .... ±25V
Output Voltage (Pin 6, Pin 7) .... −0.3V, VDD+0.3V
Power Dissipation (Any Package) to +75°C .... 450 mW
Derates above 75°C by .... 6 mW/°C
Dice Junction Temperature .... +150°C
Storage Temperature .... −65°C to +150°C

CAUTION:
1. Do not apply voltages higher than VDD or less than GND potential on any terminal other than VREF or RFB.
2. The digital inputs are diode clamp protected against ESD damage. However, permanent damage may occur on unprotected units from high−energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti−static handling procedures.
4. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

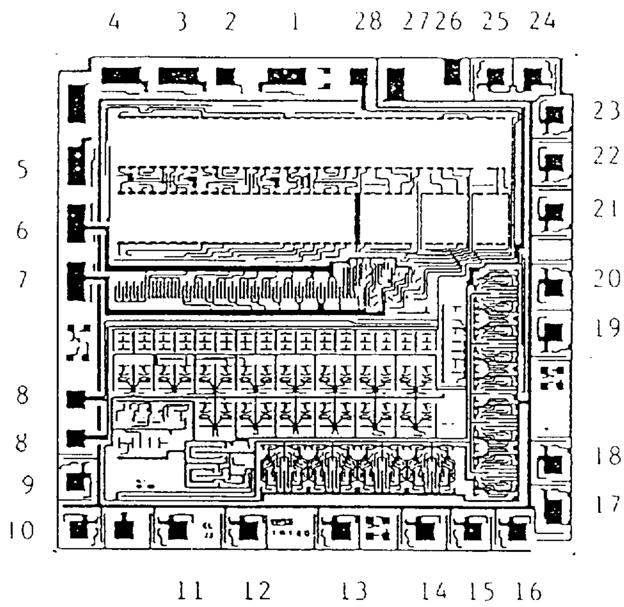
PIN CONFIGURATION



PIN DESCRIPTION

Pin name	Pin No.	I/O	Function
FB2	1	I	Feedback Resistor 2
LDTR	2	I	Ladder Termination Resistor
FB1	3	I	Feedback Resistor 1
VREF	4	I	Reference Voltage
RFB	5	I	Feedback Resistor
IO1	6	O	Current Output
IO2	7	O	Current Output
VSA	8	P	Analog Ground
BIT1	9	I	Data BIT1, MSB
BIT2	10	I	Data BIT2
BIT3	11	I	Data BIT3
BIT4	12	I	Data BIT4
BIT5	13	I	Data BIT5
BIT6	14	I	Data BIT6
BIT7	15	I	Data BIT7
BIT8	16	I	Data BIT8
BIT9	17	I	Data BIT9
BIT10	18	I	Data BIT19
BIT11	19	I	Data BIT11
BIT12	20	I	Data BIT12, LSB
LDAC	21	I	Latch DAC, Active High
$\overline{CE}$	22	I	Chip Select, Active Low
LNE	23	I	Low Nibble Enable, Active High
MNE	24	I	Medium Nibble Enable, Active High
HNE	25	I	High Nibble Enable, Active High
VDD	26	P	Digital Positive Power Supply
GND	27	G	Digital Ground
VDA	28	P	Analog Positive Power Supply

DICE CHARACTERISTICS



1. FB2
2. LDTR
3. FB1
4. VREF
5. RFB
6. IO1
7. IO2
8. VSA
9. BIT1, MSB
10. BIT2
11. BIT3
12. BIT4
13. BIT5
14. BIT6
15. BIT7
16. BIT8
17. BIT9
18. BIT10
19. BIT11
20. BIT12, LSB
21. LDAC
22. $\overline{\text{CE}}$
23. LNE
24. MNE
25. HNE
26. VDD
27. GND
28. VDA

WAFER TEST LIMITS

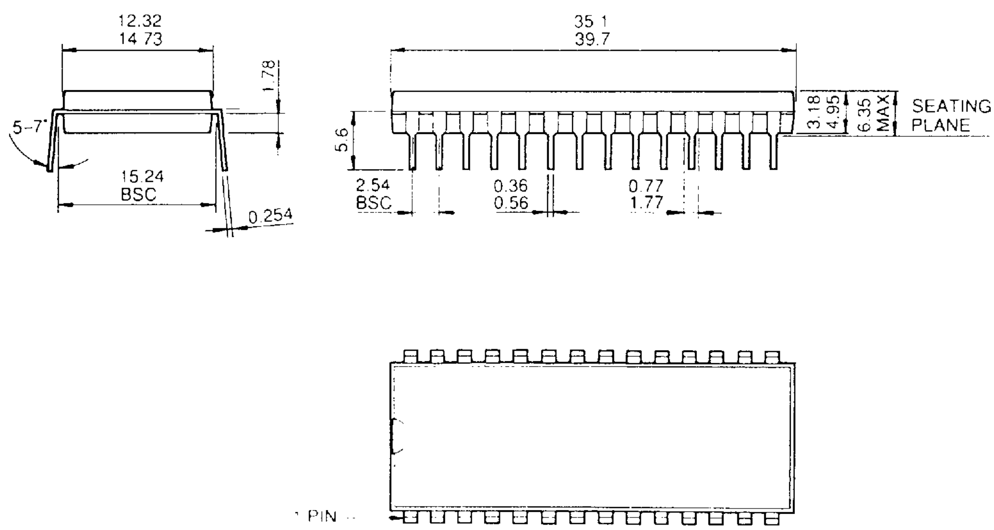
TA=+25°C, VDD=+15V, VREF= +10V, IO1=IO2=GND=0V

Parameter	Symbol	Limits	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Integral Nonlinearity[1]	INL	±1/2	LSB	
Differential Nonlinearity[2]	DNL	±1	LSB	
Gain error	Gfse	±10	LSB	Measured Using Internal Rfb DAC Register Loaded With All 1's
Output Leakage Current at IO1 (pin 6)	Ilkg	±10	nA	
REFERENCE INPUT				
Input Resistance	Rref	5/12	kΩ	Pad 4
DIGITAL INPUTS				
Input High Voltage	VIH	2.4	V	
Input Low Voltage	VIL	0.8	V	
Input Current	Iin	±1	µA	VIN=0V or VDD
SWITCHING CHARACTERISTICS				
Strobe Width	tST	60	ns	LDAC, $\overline{\text{CE}}$, HNE, MNE, LNE Inputs
Data Set-up Time	tDS	60	ns	
Data Hold Time	tDH	40	ns	
POWER SUPPLY				
Supply Current	IDD	2.5	mA	VIN<0.8V or >3.5V
	IDD	1.0	mA	VIN=0V or 5V to VDD

NOTES:
1. Integral Nonlinearity is measured as the arithmetic mean value of the magnitudes of the greatest positive deviation and the greatest negative deviation from the theoretical value of any given input combination.
2. Differential Nonlinearity DNL is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.

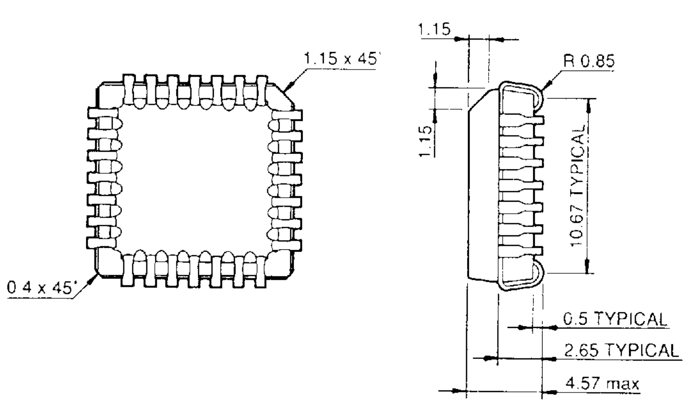
PACKAGE OUTLINES

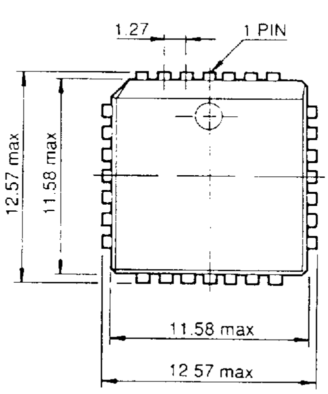
28LEAD PDIP OUTLINE (600 MIL BODY)



ALL DIMENSIONS IN mm

28LEAD PLCC OUTLINE





ALL DIMENSIONS IN mm

ORDERING INFORMATION

Product code	Product	Package	Comments
MAS3120N	µP–Compatible 14–bit DAC	28 Pin PDIP	
MAS3120P	µP–Compatible 14–bit DAC	28 Pin PLCC	

LOCAL DISTRIBUTOR

MICRONAS CONTACTS

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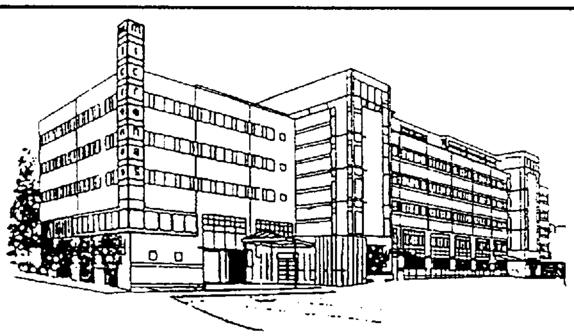
♦ HEAD OFFICE / FACTORY



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