Integrated Device Technology, Inc.

CMOS SyncFIFO™ 64 x 8, 256 x 8, 512 x 8, 1,024 x 8, 2,048 x 8 and 4,096 x 8

IDT72420
IDT72200
IDT72210
IDT72220
IDT72230
IDT72240

FEATURES:

- 64 x 8-bit organization (IDT72420)
- 256 x 8-bit organization (IDT72200)
- 512 x 8-bit organization (IDT72210)
- 1,024 x 8-bit organization (IDT72220)
- 2,048 x 8-bit organization (IDT72230)
- 4,096 x 8-bit organization (IDT72240)
- 10 ns read/write cycle time (IDT72420/72200/72210/72220/72230/72240)
- Read and write clocks can be asynchronous or coincidental
- Dual-Ported zero fall-through time architecture
- Empty and Full flags signal FIFO status
- Almost-empty and almost-full flags set to Empty+7 and Full-7, respectively
- Output enable puts output data bus in high-impedance state
- Produced with advanced submicron CMOS technology
- Available in 28-pin 300 mil plastic DIP and 300 mil ceramic DIP
- For surface mount product please see the IDT72421/72201/72211/72221/72231/72241 data sheet
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (–40°C to +85°C) is available

DESCRIPTION:

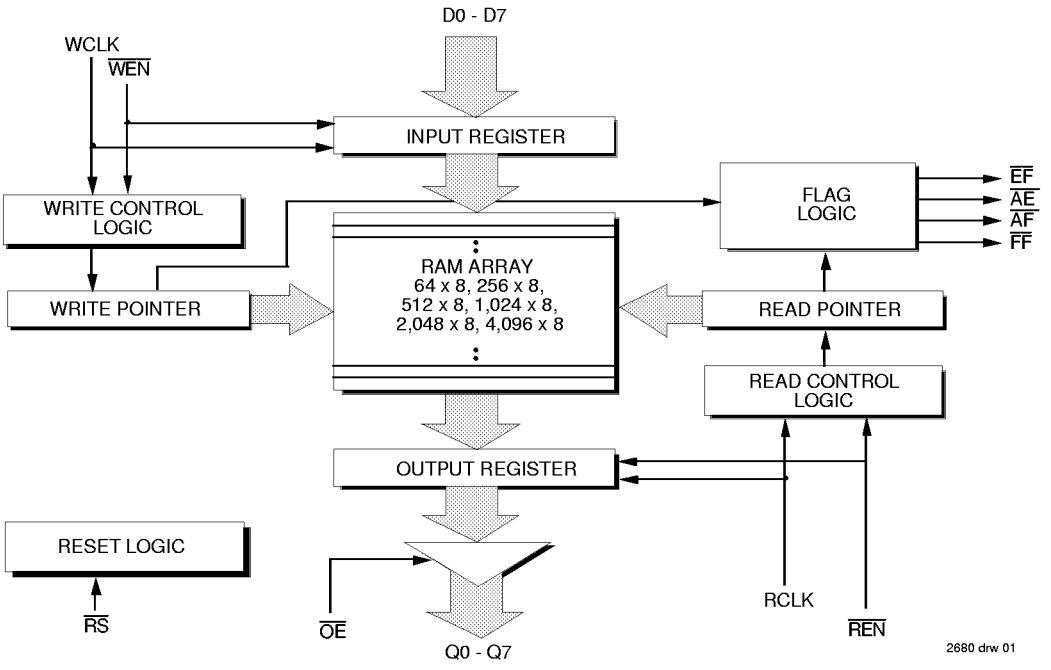
The IDT72420/72200/72210/72220/72230/72240 SyncFIFO™ are very high-speed, low-power First-In, First-Out (FIFO) memories with clocked read and write controls. These devices have a 64, 256, 512, 1,024, 2,048, and 4,096 x 8-bit memory array, respectively. These FIFOs are applicable for a wide variety of data buffering needs, such as graphics, Local Area Networks (LANs), and interprocessor communication.

These FIFOs have 8-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and a write enable pin (WEN). Data is written into the Synchronous FIFO on every clock when WEN is asserted. The output port is controlled by another clock pin (RCLK) and a read enable pin (REN). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual clock operation. An output enable pin (OE) is provided on the read port for three-state control of the output.

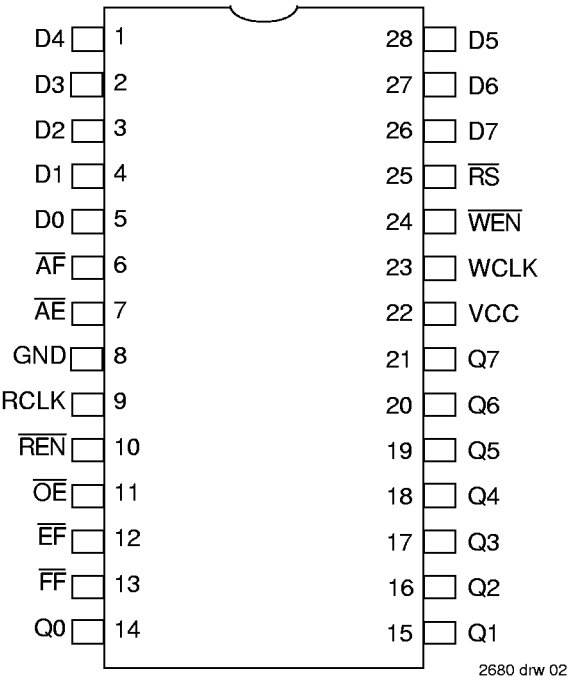
These Synchronous FIFOs have two end-point flags, Empty (EF) and Full (FF). Two partial flags, Almost-Empty (AE) and Almost-Full (AF), are provided for improved system control. The partial (AE) flags are set to Empty+7 and Full-7 for AE and AF respectively.

These FIFOs are fabricated using IDT's high-speed submicron CMOS technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PLASTIC THIN DIP (P28-2, order code: TP)
SIDEBRAZE THIN DIP (C28-1, order code: TC)
TOP VIEW

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D_0 - D_7	Data Inputs	I	Data inputs for a 8-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set LOW, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{AF}$ go HIGH, and $\overline{AE}$ and $\overline{EF}$ go LOW. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK when $\overline{WEN}$ is asserted.
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition of WCLK. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
Q_0 - Q_7	Data Outputs	O	Data outputs for a 8-bit bus.
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK when $\overline{REN}$ is asserted.
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high-impedance state.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{AE}$	Almost-Empty Flag	O	When $\overline{AE}$ is LOW, the FIFO is almost empty based on the offset Empty+7. $\overline{AE}$ is synchronized to RCLK.
$\overline{AF}$	Almost-Full Flag	O	When $\overline{AF}$ is LOW, the FIFO is almost full based on the offset Full-7. $\overline{AF}$ is synchronized to WCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
V_{CC}	Power		One +5 volt power supply pin.
GND	Ground		One 0 volt ground pin.

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–55 to +125	–65 to +135	°C
I_{OUT}	DC Output Current	–50 to +50	–50 to +50	mA

2680 tbl 02

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}	Input Low Voltage Commercial & Military	—	—	0.8	V
T_A	Operating Temperature Commercial	0	—	70	°C
T_A	Operating Temperature Military	–55	—	125	°C

2680 tbl 03

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

Symbol	Parameter	IDT72420 IDT72200 IDT72210 IDT72220 IDT72230 IDT72240 Commercial t_{CLK} = 10, 12, 15, 25, 35 ns Min.	Typ.	Max.	IDT72420 IDT72200 IDT72210 IDT72220 IDT72230 IDT72240 Military t_{CLK} = 20, 25, 50 ns Min.	Typ.	Max.	Units
I_{LI}(1)	Input Leakage Current (any input)	–1	—	1	–10	—	10	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = –2 mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	—	0.4	—	—	0.4	V
I_{CC1}(3,4,5,7)	Active Power Supply Current	—	—	50	—	—	50	mA
I_{CC2}(3,6,7)	Standby Current	—	—	5	—	—	8	mA

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NOTES:

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Tested with outputs open (I_{OUT} = 0).
4. RCLK and WCLK toggle at 20 MHz and data inputs switch at 10 MHz.
5. Typical I_{CC1} = 1.7 + 0.7*fs + 0.02*C_L*fs (in mA).
   These equations are valid under the following conditions:
   V_{CC} = 5V, T_A = 25°C, fs = WCLK frequency = RCLK frequency (in MHz, using TTL levels), data switching at fs/2, C_L = capacitive load (in pF).
6. All Inputs = V_{CC} - 0.2V or GND + 0.2V, except RCLK and WCLK, which toggle at 20 MHz.
7. The I_{CC1} and I_{CC2} parameters are improved as compared to previous data sheets. **To order product for new designs that require the measurements shown in this data sheet, please specify die revision "W" (see Ordering Information).**

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to + 70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

		Commercial						Military		Com'l & Mil.		Com'l		Military		
		72420L10 72200L10 72210L10 72220L10 72230L10 72240L10		72420L12 72200L12 72210L12 72220L12 72230L12 72240L12		72420L15 72200L15 72210L15 72220L15 72230L15 72240L15		72420L20 72200L20 72210L20 72220L20 72230L20 72240L20		72420L25 72200L25 72210L25 72220L25 72230L25 72240L25		72420L35 72200L35 72210L35 72220L35 72230L35 72240L35		72420L50 72200L50 72210L50 72220L50 72230L50 72240L50		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
fS	Clock Cycle Frequency	—	100	—	83.3	—	66.7	—	50	—	40	—	28.6	—	20	MHz
tA	Data Access Time	2	6.5	2	8	2	10	2	12	2	15	2	20	3	25	ns
tCLK	Clock Cycle Time	10	—	12	—	15	—	20	—	25	—	35	—	50	—	ns
tCLKH	Clock High Time	4.5	—	5	—	6	—	8	—	10	—	14	—	20	—	ns
tCLKL	Clock Low Time	4.5	—	5	—	6	—	8	—	10	—	14	—	20	—	ns
tDS	Data Set-up Time	3	—	3	—	4	—	5	—	6	—	7	—	10	—	ns
tDH	Data Hold Time	0.5	—	0.5	—	1	—	1	—	1	—	2	—	2	—	ns
tENS	Enable Set-up Time	3	—	3	—	4	—	5	—	6	—	7	—	10	—	ns
tENH	Enable Hold Time	0.5	—	0.5	—	1	—	1	—	1	—	2	—	2	—	ns
tRS	Reset Pulse Width[1]	10	—	12	—	15	—	20	—	15	—	35	—	50	—	ns
tRSS	Reset Set-up Time	8	—	9	—	10	—	20	—	15	—	20	—	50	—	ns
tRSR	Reset Recovery Time	8	—	9	—	10	—	20	—	15	—	20	—	50	—	ns
tRSF	Reset to Flag and Output Time	—	10	—	12	—	15	—	20	—	25	—	35	—	50	ns
tOLZ	Output Enable to Output in Low-Z[2]	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	2	6	3	7	3	8	3	10	3	13	3	15	3	23	ns
tOHZ	Output Enable to Output in High-Z[2]	2	6	3	7	3	8	3	10	3	13	3	15	3	23	ns
tWFF	Write Clock to Full Flag	—	6.5	—	8	—	10	—	12	—	15	—	20	—	30	ns
tREF	Read Clock to Empty Flag	—	6.5	—	8	—	10	—	12	—	15	—	20	—	30	ns
tAF	Write Clock to Almost-Full Flag	—	6.5	—	8	—	10	—	12	—	15	—	20	—	30	ns
tAE	Read Clock to Almost-Empty Flag	—	6.5	—	8	—	10	—	12	—	15	—	20	—	30	ns
tSKEW1	Skew time between Read Clock & Write Clock for Empty Flag & Full Flag	4	—	5	—	6	—	8	—	10	—	12	—	15	—	ns
tSKEW2	Skew time between Read Clock & Write Clock for Almost-Empty Flag & Almost-Full Flag	10	—	12	—	15	—	16	—	18	—	20	—	45	—	ns

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NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}[2]	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}[1, 2]	Output Capacitance	V_{OUT} = 0V	10	pF

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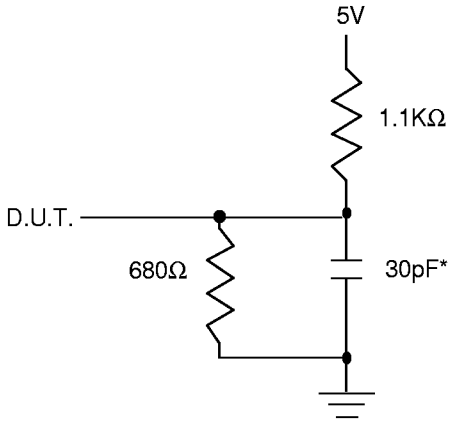
NOTES:
1. With output deselected. ($\overline{OE} \geq V_{IH}$)
2. Characterized values, not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2680 tbl 09



2680 drw 03

or equivalent circuit

Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

INPUTS:

Data In (D_0–D_7) — Data inputs for 8-bit wide data.

CONTROLS:

Reset ($\overline{RS}$) — Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. The Full Flag ($\overline{FF}$) and Almost Full Flag ($\overline{AF}$) will be reset to HIGH after t_{RSF}. The Empty Flag ($\overline{EF}$) and Almost Empty Flag ($\overline{AE}$) will be reset to LOW after t_{RSF}. During reset, the output register is initialized to all zeros.

Write Clock (WCLK) — A write cycle is initiated on the LOW-to-HIGH transition of the write clock (WCLK). Data set-up and hold times must be met in respect to the LOW-to-HIGH transition of the write clock (WCLK). The Full Flag ($\overline{FF}$) and Almost Full Flag ($\overline{AF}$) are synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

The write and read clocks can be asynchronous or coincident.

Write Enable ($\overline{WEN}$) — When Write Enable ($\overline{WEN}$) is LOW, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

When Write Enable ($\overline{WEN}$) is HIGH, the input register holds the previous data and no new data is allowed to be loaded into the register.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go HIGH after t_{WFF}, allowing a valid write to begin. Write Enable ($\overline{WEN}$) is ignored when the FIFO is full.

Read Clock (RCLK) — Data can be read on the outputs on the LOW-to-HIGH transition of the read clock (RCLK). The Empty Flag ($\overline{EF}$) and Almost-Empty Flag ($\overline{AE}$) are synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

The write and read clocks can be asynchronous or coincident.

Read Enable ($\overline{REN}$) — When Read Enable ($\overline{REN}$) is LOW, data is read from the RAM array to the output register on the LOW-to-HIGH transition of the read clock (RCLK).

When Read Enable ($\overline{REN}$) is HIGH, the output register holds the previous data and no new data is allowed to be loaded into the register.

When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go HIGH after t_{REF} and a valid read can begin. Read Enable ($\overline{REN}$) is ignored when the FIFO is empty.

Output Enable ($\overline{OE}$) — When Output Enable ($\overline{OE}$) is enabled (LOW), the parallel output buffers receive data from the output register. When Output Enable ($\overline{OE}$) is disabled (HIGH), the Q output data bus is in a high-impedance state.

OUTPUTS:

Full Flag ($\overline{FF}$) — The Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operation, when the device is full. If no reads are performed after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go LOW after 64 writes for the IDT72420, 256 writes for the IDT72200, 512 writes for the IDT72210, 1,024 writes for the IDT72220, 2,048 writes for the IDT72230, and 4,096 writes for the IDT72240.

The Full Flag ($\overline{FF}$) is synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

Empty Flag ($\overline{EF}$) — The Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty.

The Empty Flag ($\overline{EF}$) is synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

Almost Full Flag ($\overline{AF}$) — The Almost Full Flag ($\overline{AF}$) will go LOW when the FIFO reaches the Almost-Full condition. If no reads are performed after Reset ($\overline{RS}$), the Almost Full Flag ($\overline{AF}$) will go LOW after 57 writes for the IDT72420, 249 writes for the IDT72200, 505 writes for the IDT72210, 1,017 writes for the IDT72220, 2,041 writes for the IDT72230 and 4,089 writes for the IDT72240.

The Almost Full Flag ($\overline{AF}$) is synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

Almost Empty Flag ($\overline{AE}$) — The Almost Empty Flag ($\overline{AE}$) will go LOW when the FIFO reaches the Almost-Empty condition. If no reads are performed after Reset ($\overline{RS}$), the Almost Empty Flag ($\overline{AE}$) will go HIGH after 8 writes for the IDT72420, IDT72200, IDT72210, IDT72220, IDT72230 and IDT72240.

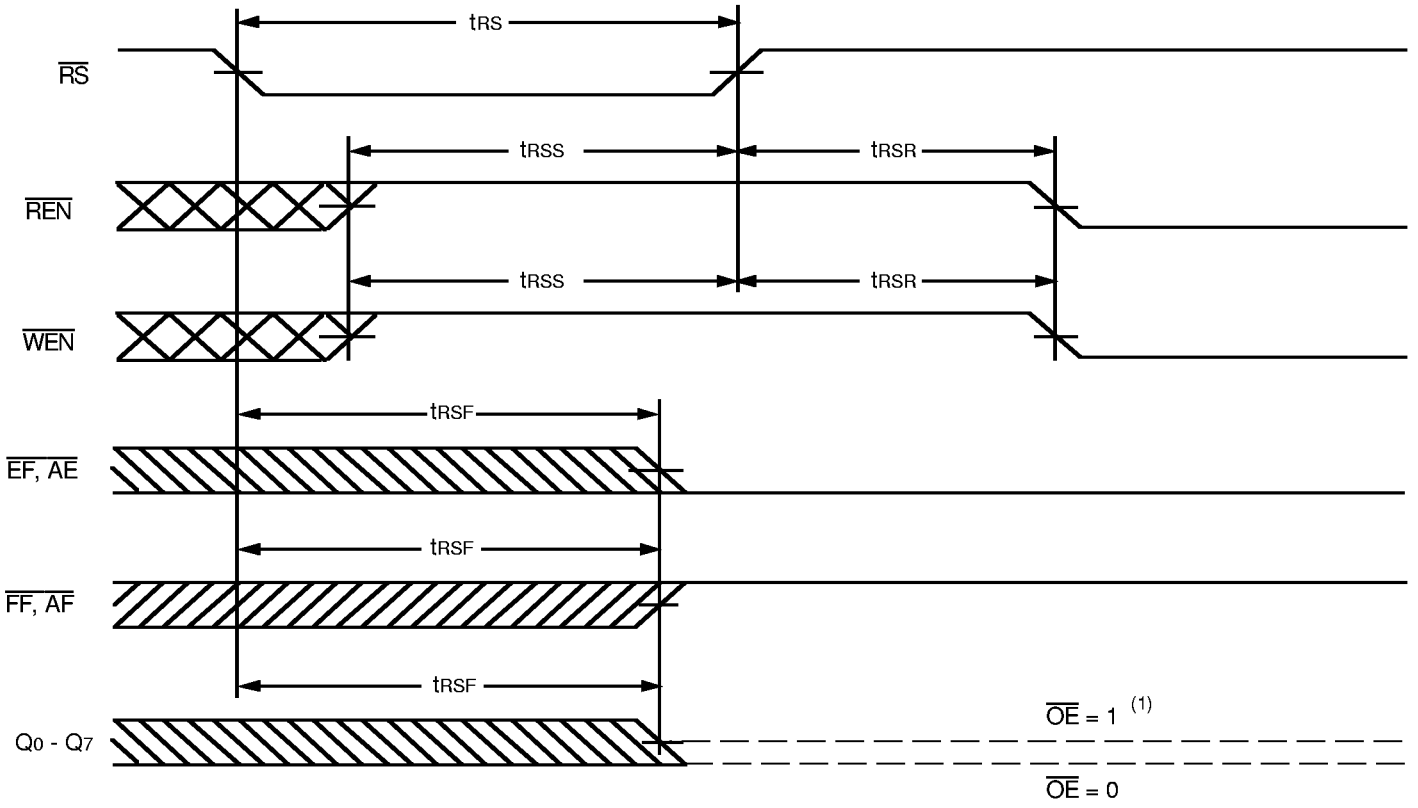
The Almost Empty Flag ($\overline{AE}$) is synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

Data Outputs (Q_0–Q_7) — Data outputs for a 8-bit wide data.

TABLE 1: STATUS FLAGS

Number of Words in FIFO						$\overline{FF}$	$\overline{AF}$	$\overline{AE}$	$\overline{EF}$
IDT72420	IDT72200	IDT72210	IDT72220	IDT72230	IDT72240				
0	0	0	0	0	0	H	H	L	L
1 to 7	1 to 7	1 to 7	1 to 7	1 to 7	1 to 7	H	H	L	H
8 to 56	8 to 248	8 to 504	8 to 1,016	8 to 2,040	8 to 4,088	H	H	H	H
57 to 63	249 to 255	505 to 511	1,017 to 1,023	2,041 to 2,047	4,089 to 4,095	H	L	H	H
64	256	512	1,024	2,048	4,096	L	L	H	H

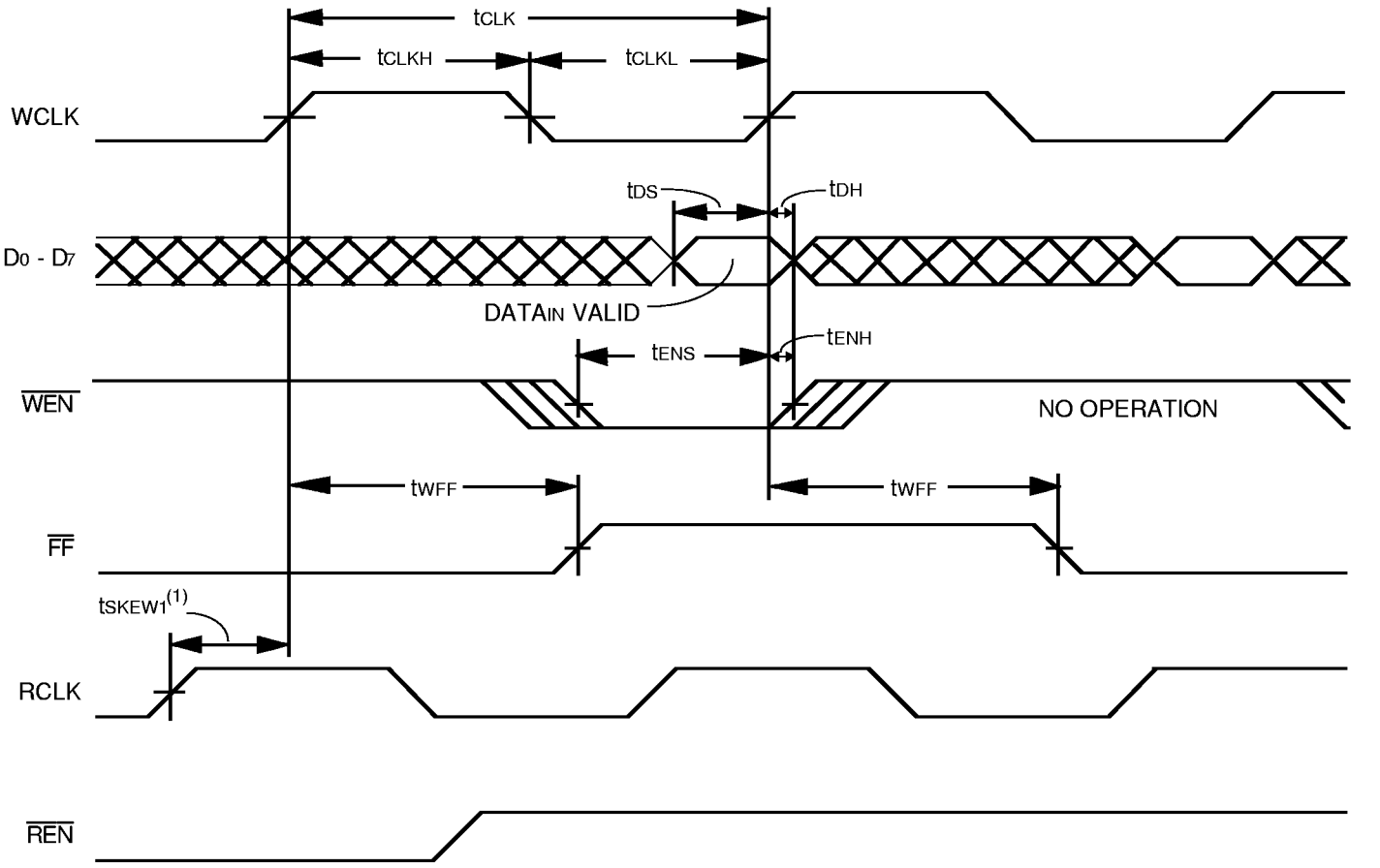
2680 tbl 10



2680 drw 04

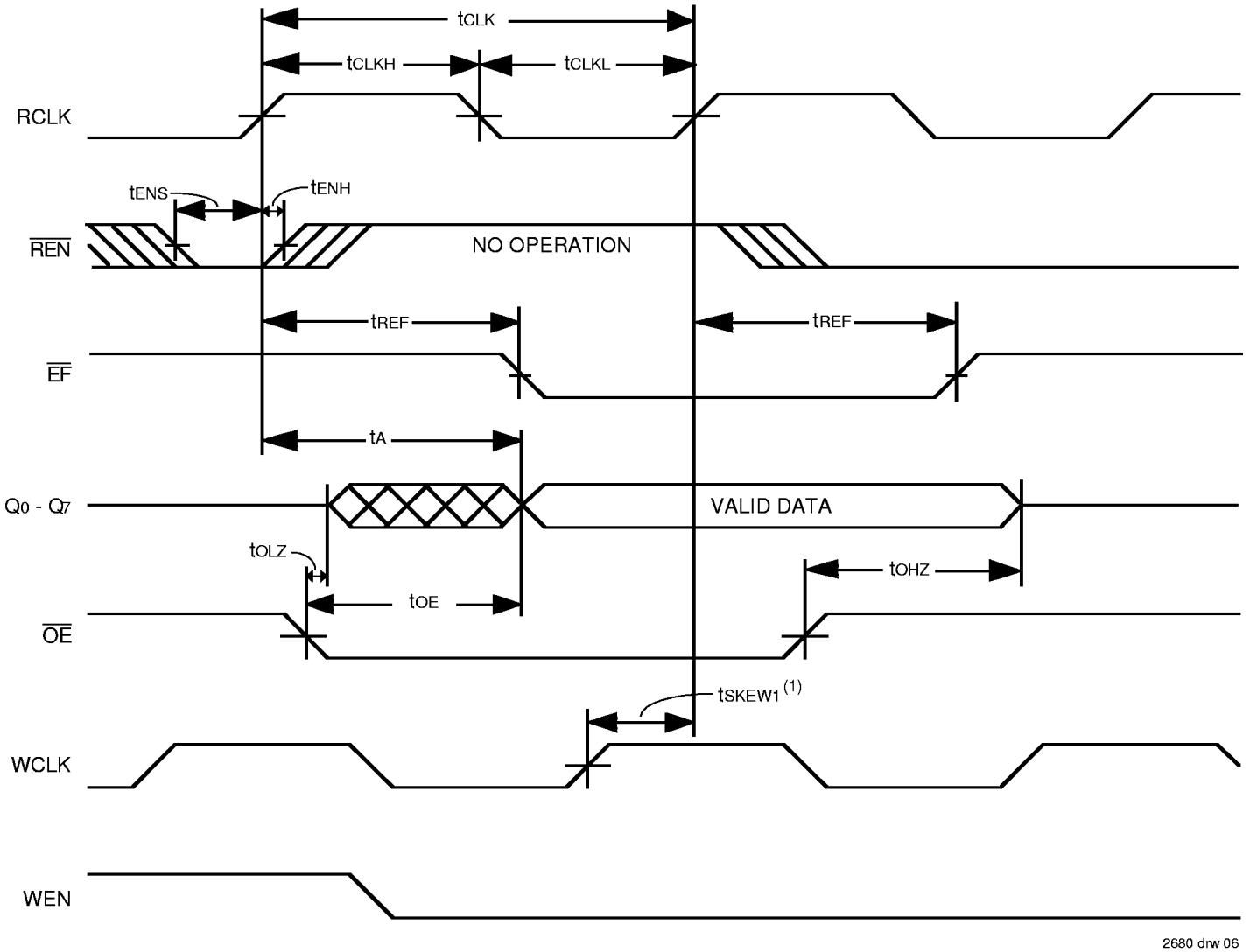
NOTE:
1. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and tri-state if $\overline{OE}$ = 1.
2. The clocks (RCLK, WCLK) can be free-running during reset.

Figure 2. Reset Timing



NOTES:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{FF}$ to change during the curent clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.

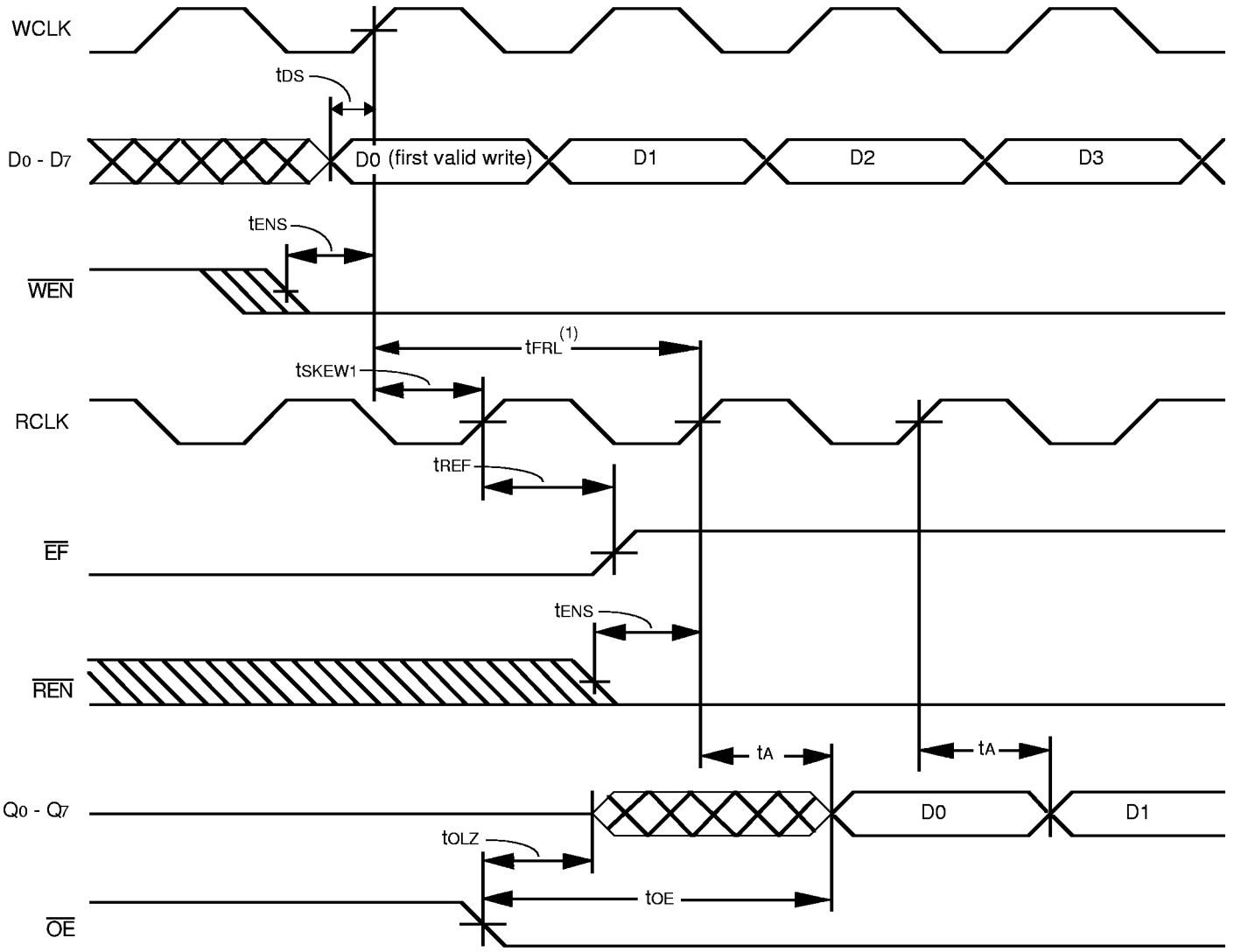
Figure 3. Write Cycle Timing



2680 drw 06

NOTE:
1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{EF}$ to change during the curent clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, then $\overline{EF}$ may not change state until the next RCLK edge.

Figure 4. Read Cycle Timing



2680 drw 07

NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} maximum = $t_{CLK} + t_{SKEW1}$
   t_{SKEW1} < minimum specification, t_{FRL} maximum = $2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timing apply only at the Empty Boundry ($\overline{EF}$ = LOW).

Figure 5. First Data Word Latency Timing

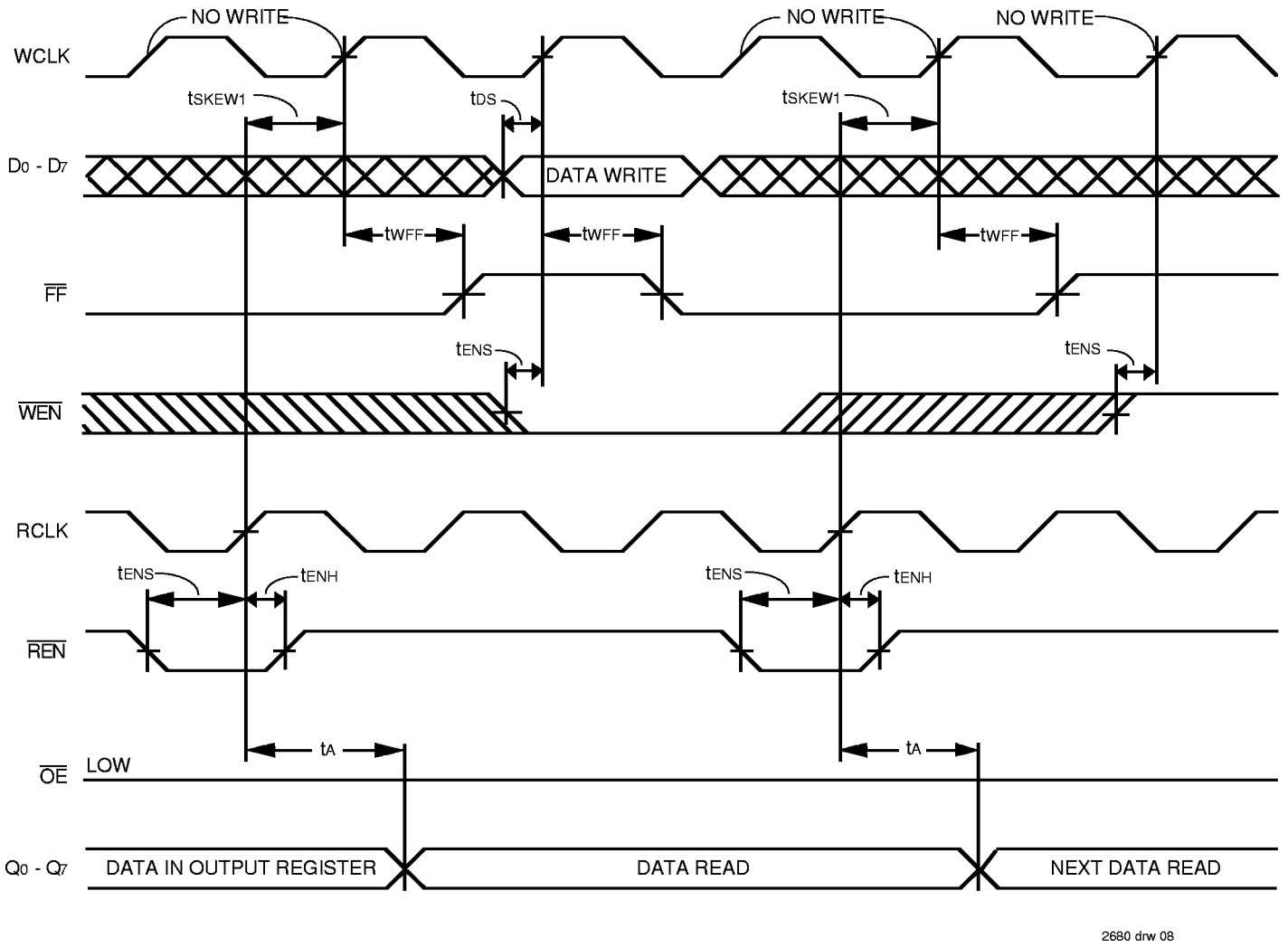
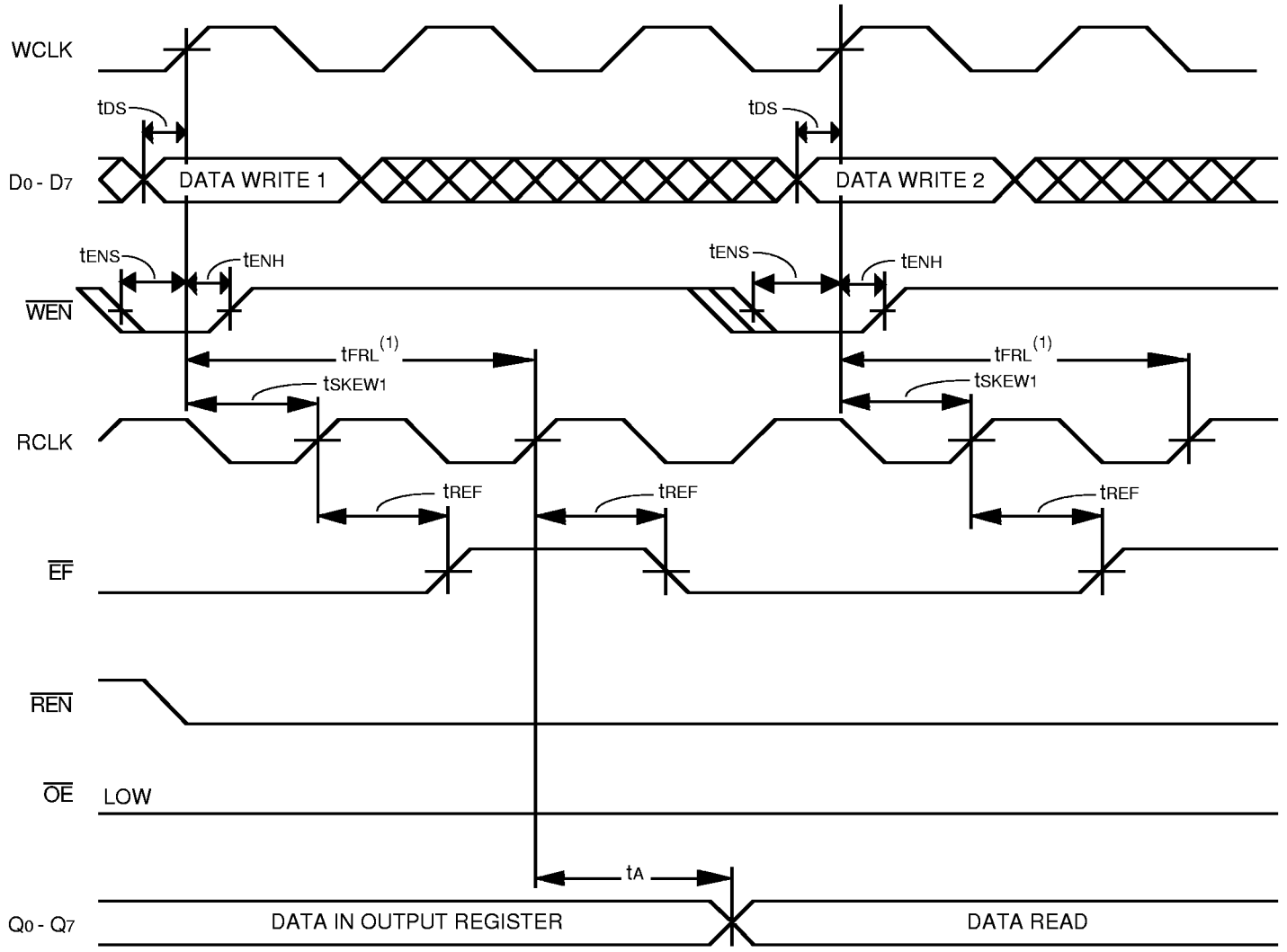


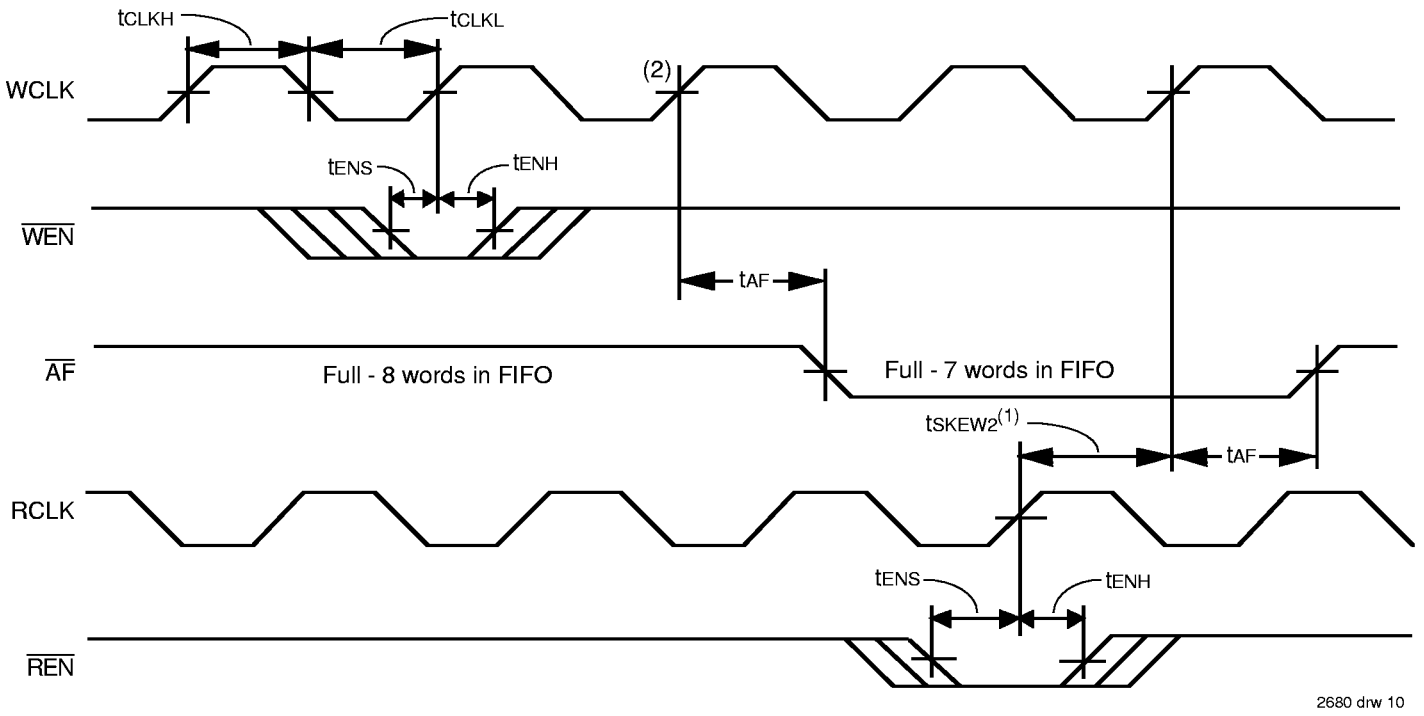
Figure 6. Full Flag Timing



2680 drw 09

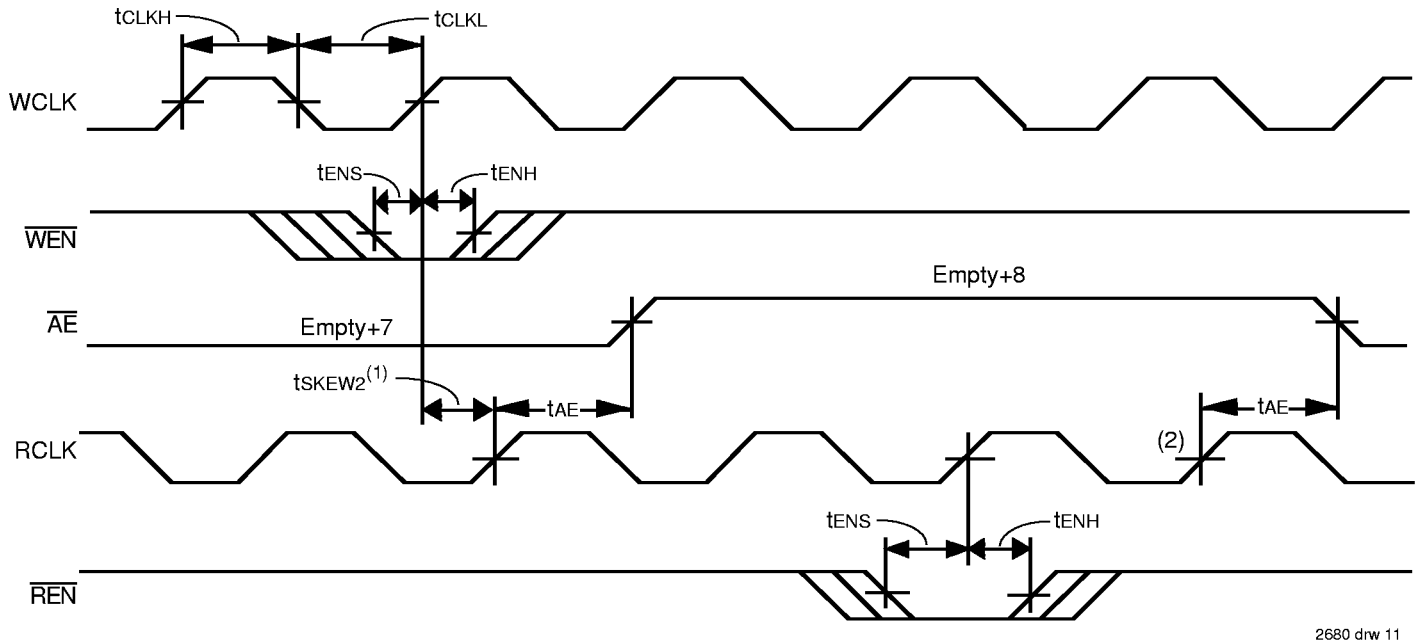
NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} maximum = $t_{CLK} + t_{SKEW1}$
   t_{SKEW1} < minimum specification, t_{FRL} maximum = $2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timing apply only at the Empty Boundry ($\overline{EF}$ = LOW).

Figure 7. Empty Flag Timing



NOTES:
1. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{AF}$ to change during the curent clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{AF}$ may not change state until the next WCLK edge.
2. If a write is performed on this rising edge of the write clock, there will be Full - 6 words in the FIFO when $\overline{AF}$ goes LOW.

Figure 8. Almost Full Flag Timing



NOTES:
1. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{AE}$ to change during the curent clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{AE}$ may not change state until the next RCLK edge.
2. If a read is performed on this rising edge of the read clock, there will be Empty - 6 words in the FIFO when $\overline{AE}$ goes LOW.

Figure 9. Almost Empty Flag Timing

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION - A single IDT72420/72200/72210/72220/72230/72240 may be used when the application requirements are for 64/256/512/1,024/2,048/4,096 words or less. See Figure 10.

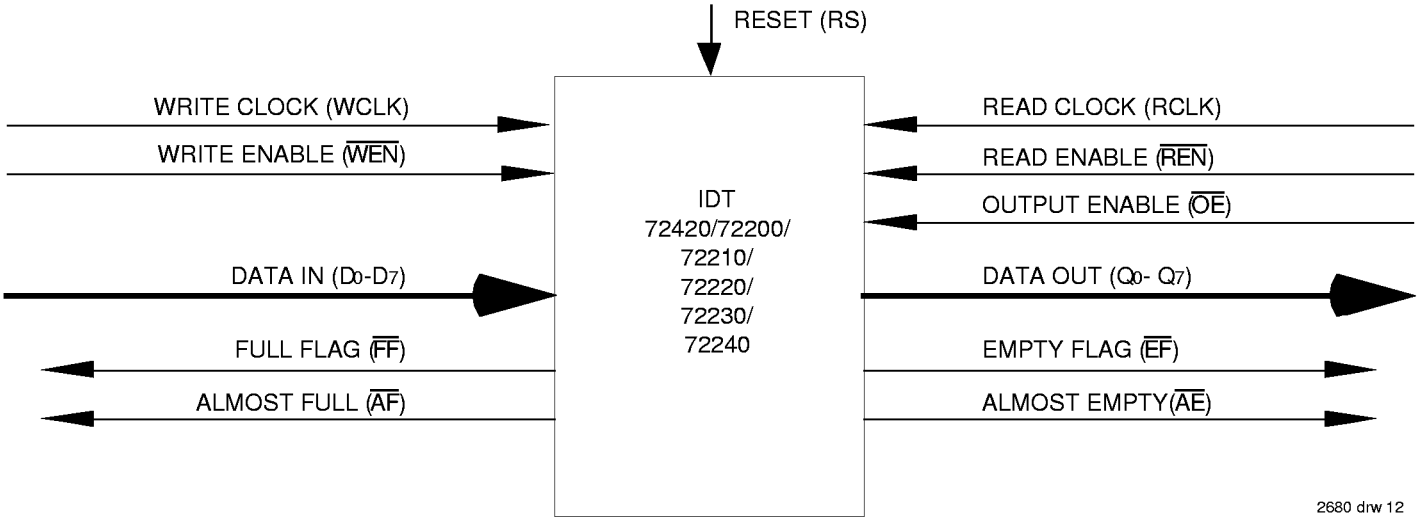


Figure 10. Block Diagram of Single 64 x 8, 256 x 8, 512 x 8, 1,024 x 8, 2,048 x 8, 4,096 x 8 Synchronous FIFO

WIDTH EXPANSION CONFIGURATION - Word width may be increased simply by connecting the corresponding input control signals of multiple devices. A composite flag should be created for each of the end-point status flags (EF and FF) The partial status flags (AE and AF) can be detected from any one device. Figure 11 demonstrates a 16-bit word width by using two IDT72420/72200/72210/72220/72230/72240s. Any word width can be attained by adding additional IDT72420/72200/72210/72220/72230/72240s.

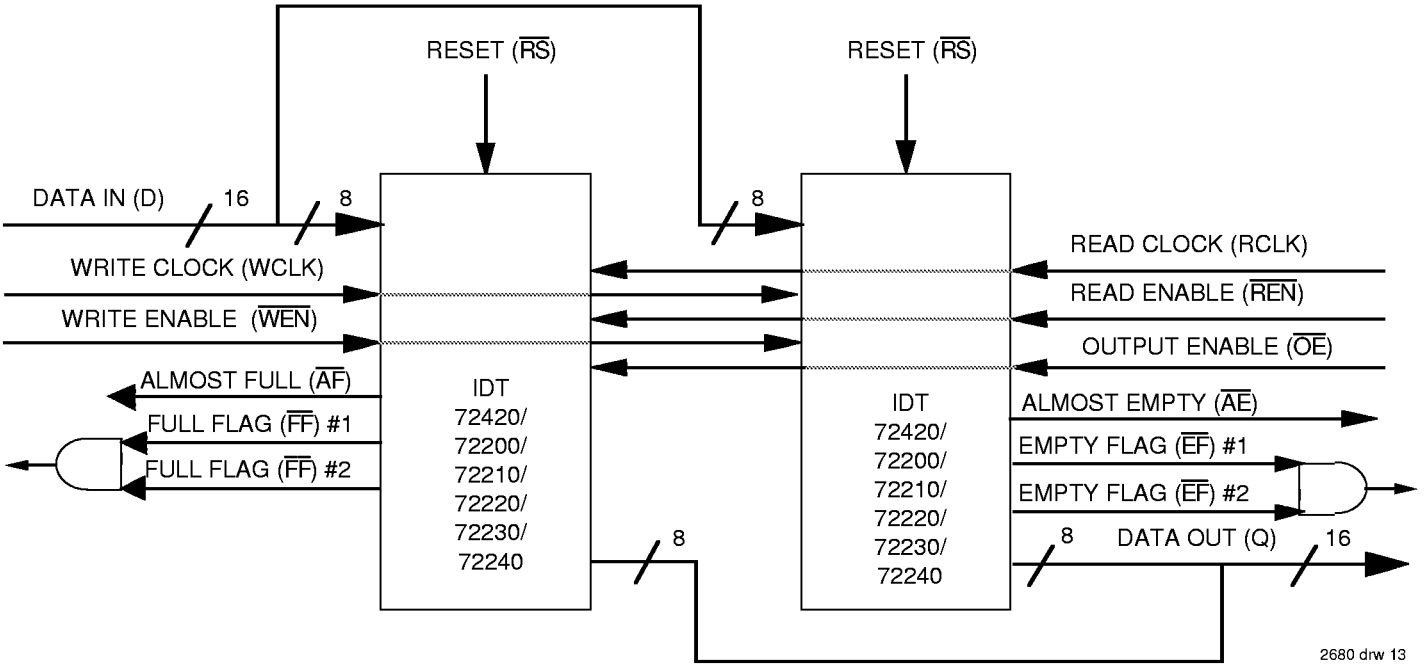
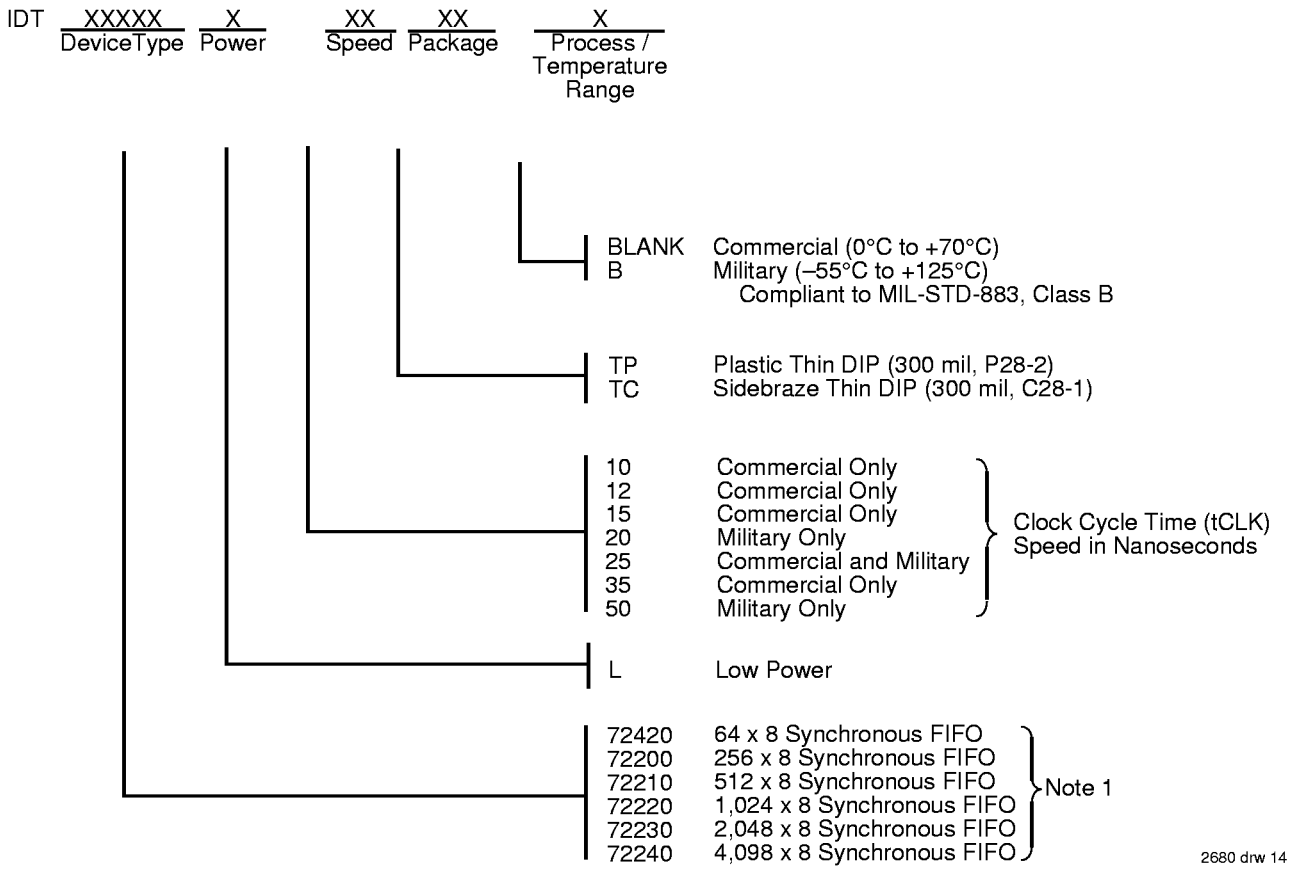


Figure 11. Block Diagram of 64 x 16, 256 x 16, 512 x 16, 1,024 x 16, 2,048 x 16, 4,096 x 16 Synchronous FIFO Used in a Width Expansion Configuration

DEPTH EXPANSION - The IDT72420/72200/72210/72220/72230/72240 can be adapted to applications when the requirements are for greater than 64/256/512/1,024/2,048/4,096 words. Depth expansion is possible by using expansion logic to direct the flow of data. A typical application would have the expansion logic alternate data accesses from one device to the next in a sequential manner.

Please see the Application Note "DEPTH EXPANSION IDT'S SYNCHRONOUS FIFOs USING RING COUNTER APPROACH" for details of this configuration.

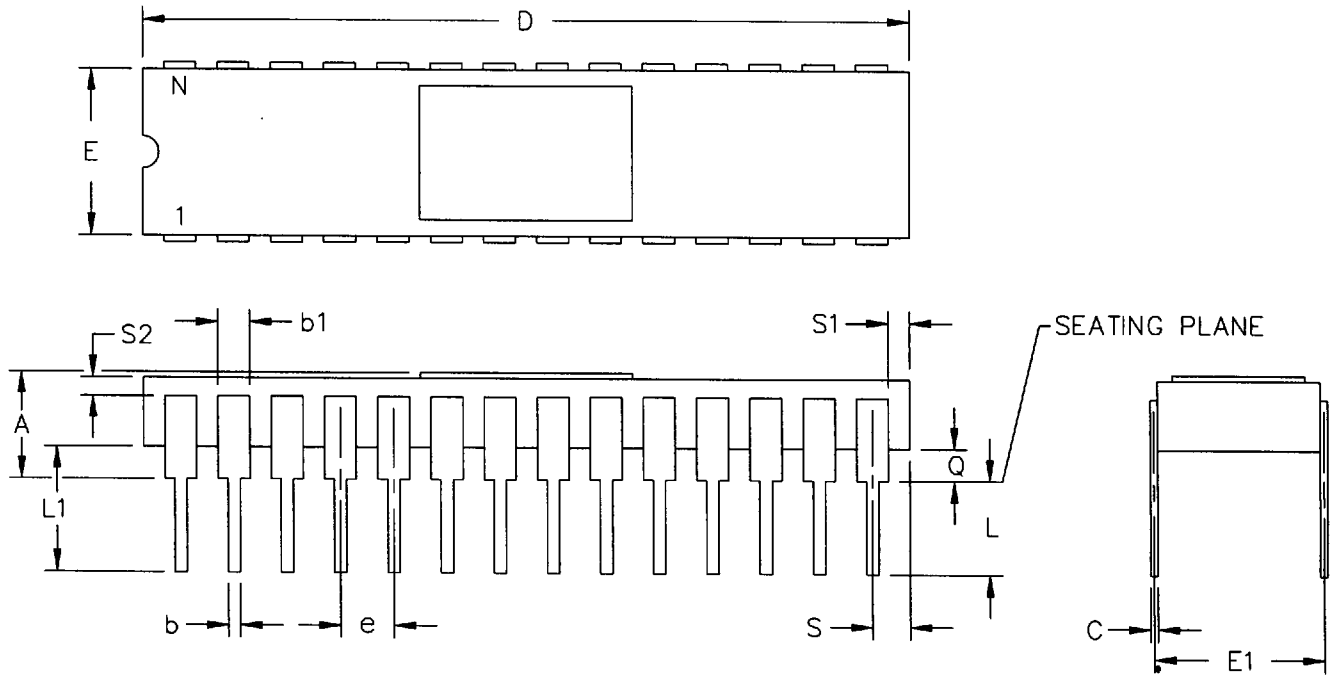
ORDERING INFORMATION



NOTES:
1. To order die revision "W" (improved Icc specs), please specify SCDS-W after the part number.
2. Industrial temperature range is available by special order.

SIDEBRAZE (Continued)

REV	DCN	DESCRIPTION	DATE	APPROVED
02	17564	UPDATED TO STANDARDIZE DWG	4-2-90	S. Thomas
03	19319	ADDED MIL-M-38510 REGISTRATION	10/30/90	D Guilhamet
04	22238	CHANGED b1 MIN DIMENSION		



NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "N" REPRESENTS THE NUMBER OF LEADS.

DWG #	C28-1	
SYMBOL	MIN	MAX
A	.090	.200
b	.014	.023
b1	.045	.060
C	.008	.015
D	1.380	1.420
E	.220	.310
E1	.290	.320
e	.100 BSC	
L	.125	.200
L1	.150	–
N	28	
Q	.015	.060
S	.030	.065
S1	.005	–
S2	.005	–

	CONFIGURATION	EXCEPTIONS
MIL-M-38510	D-15	
JEDEC	NOT REGISTERED	

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRAC DEC ANGLES
± – ± – ± –

APPROVALS	DATE
DRAWN AA	03/90
CHECKED	

Integrated Device Technology, Inc.
3236 Scott Blvd., Santa Clara, CA 95051
(408) 727-6116 FAX: (408) 727-2328

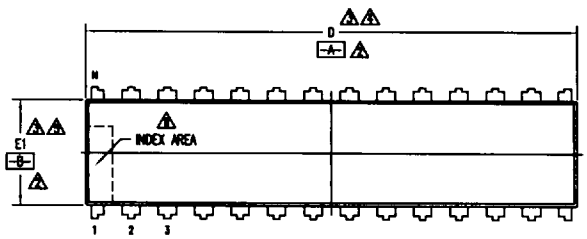
28 LD SIDE BRAZE
(300 MIL) MKT DWG

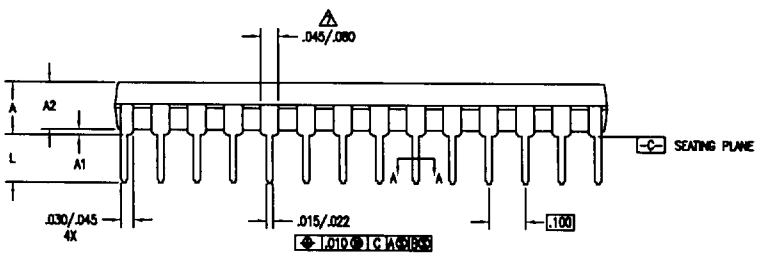
SCALE	SIZE	DRAWING NO.	REV
N/A	A	PSC-2042	04

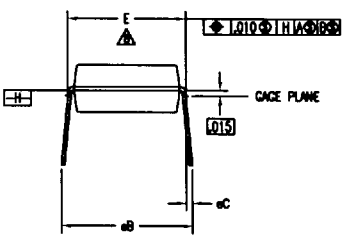
DO NOT SCALE DRAWING SHEET 36

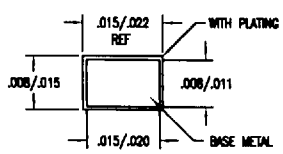
PLASTC DIP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27852	04	REDRAW TO JEDEC FORMAT	03/15/95	









SECTION A–A

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070
DECIMAL .XX± .XXX± .XXXX±	ANGULAR ±	
APPROVALS	DATE	TITLE PT 28 PACKAGE OUTLINE .300" BODY WIDTH PDIP .100" PITCH
DRAWN AA	07/15/88	
CHECKED		SIZE C DRAWING No. PSC-4018 REV 04
		DO NOT SCALE DRAWING

PLASTIC DIP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27652	04	REDRAW TO JEDEC FORMAT	03/15/96	

DWG #	P28-2			
SYMBOL	JEDEC VARIATION AH			NOTE
	MIN	NOM	MAX	
A	.145	-	.180	
A1	.015	-	.030	
A2	.120	.135	.150	
D	1.345	1.365	1.385	3,4
E	.300	.310	.325	6
E1	.275	.285	.295	3,5
eB	.310	-	.400	
eC	.000	-	.050	
L	.120	.135	.150	
N	28			

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .010 PER SIDE
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEEED .010 PER SIDE
6. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .010 MAXIMUM TOTAL PER LEAD
8. DIMENSION E IS MEASURED ON THE OUTSIDE SURFACE OF THE LEADS AT THE GAGE OF .015 BELOW DATUM PLANE -H-
9. ALL DIMENSIONS ARE IN INCHES
10. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-095, VARIATION AH

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070
DECIMAL XX± XXX± XXXX±	ANGULAR ±	
APPROVALS	DATE	TITLE PT 28 PACKAGE OUTLINE .300" BODY WIDTH PDIP .100" PITCH
DRAWN AA	07/15/96	
CHECKED		SIZE C DRAWING No. PSC-4018 REV 04
		DO NOT SCALE DRAWING