SONY

CXB1144Q/Q-Y

Dual 8 : 1 Multiplexer with Latch

T-68-11-51

Description

The CXB1144Q is an ultra high speed monolithic ECL IC, which contains two 8 : 1 multiplexers with transparent Latched outputs. The data select (S_0-S_2) inputs determine which data input is enabled. When both Latch enable (LEN1, LEN2) inputs are LOW, the Latch is transparent. The selected data is Latched on the positive transition of the Latch enable inputs. The Master Reset (MR) overrides all other control inputs and turns Q outputs to LOW.

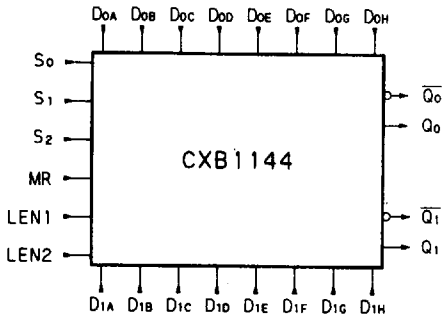
Features

- Typical propagation delay time: Tpd=1000 ps (D_{nA}-D_{nH} to Qn)
- Differential outputs
- Internal pull down resistors on input pins to maintain logic LOW level with the pins left open
- ECL 100K compatible I/O levels

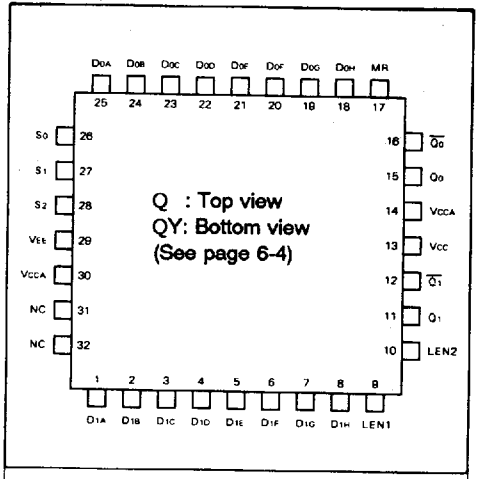
Pin Names

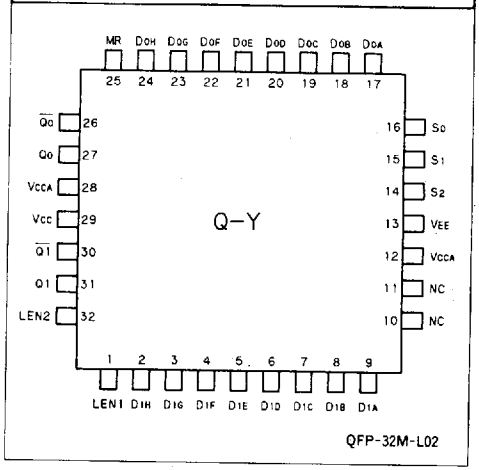
D_{nA}–D_{nH}	Data inputs
Qn, $\overline{Qn}$	Data outputs
Sn	Data select inputs
LENn	Latch enable inputs
MR	Direct Master Reset input
V_{CC}	Circuit ground
V_{CCA}	Circuit ground for outputs
V_{EE}	Negative power supply

Logic Symbol



Pin Assignment





DC Characteristics

$V_{EE}=-4.5V\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{EE}		−102	−75	−52	mA

Note: Other DC characteristics; See pages 3-3 and 3-4.

AC Characteristics

$V_{EE}=-4.5V\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$, $R_T=50\Omega$ to V_{TT}

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	T_{PLH}	D_{nA} to D_{nH}	Qn	LEN1=L LEN2=L	710	950	1240	ps
	T_{PHL}				750	1000	1300	
	T_{PLH}	Sn			900	1200	1560	
	T_{PHL}				920	1230	1600	
	T_{PLH}	LENn			600	810	1060	
	T_{PHL}				630	850	1110	
	T_{PLH}	MR			720	970	1260	
	T_{PHL}				740	990	1290	
Gate-to-Gate skew	T_{SG-G}	D		LENn=L		70	120	
Set up time	Ts	D, LENn			320			
		Sn, LENn			540			
Hold time	Th	LENn, D			−70			
		LENn, Sn			−290			
Release time	T_R	MR, LENn			330			
Min. Pulse width	T_{pw}	MR			550			
Rise time	T_{TLH}	D_{nA} to D_{nH}		20% to 80%		300	390	
Fall time	T_{THL}					250	330	

Note: AC test circuit; See pages 4-3, 4-4 and 4-5.

Truth Table

Select inputs			Outputs
S_0	S_1	S_2	Qn
L	L	L	D_{nA}
H	L	L	D_{nB}
L	H	L	D_{nC}
H	H	L	D_{nD}
L	L	H	D_{nE}
H	L	H	D_{nF}
L	H	H	D_{nG}
H	H	H	D_{nH}

Inputs		Operation
LEN1	LEN2	
L	L	Transparent
H	X	Latch
X	H	Latch

Note : H ; HIGH voltage Level
L ; LOW voltage Level
X ; Don't care

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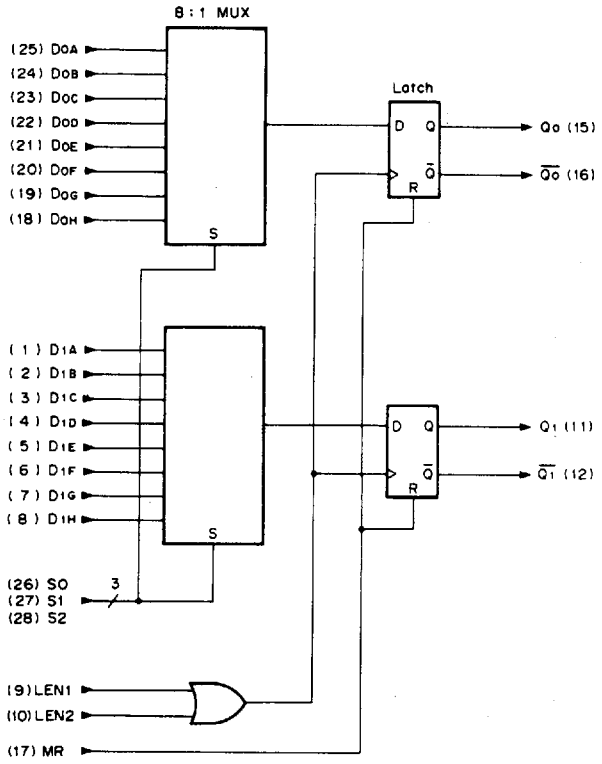
Block Diagram



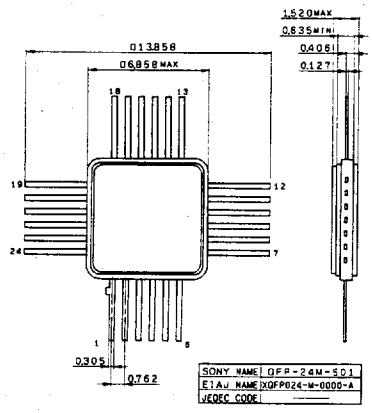
Package Data

T-90-20

Package Outline Uuit: mm

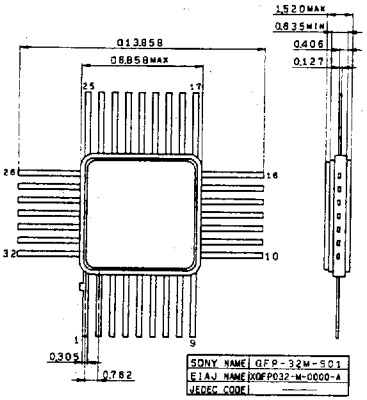
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



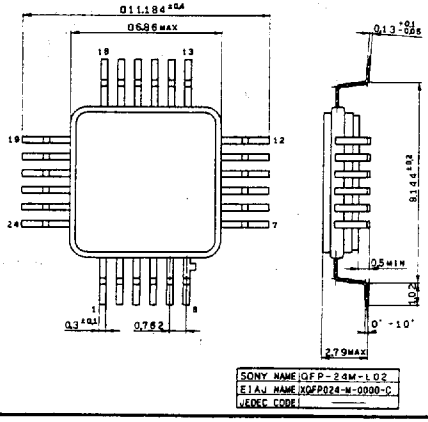
32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g



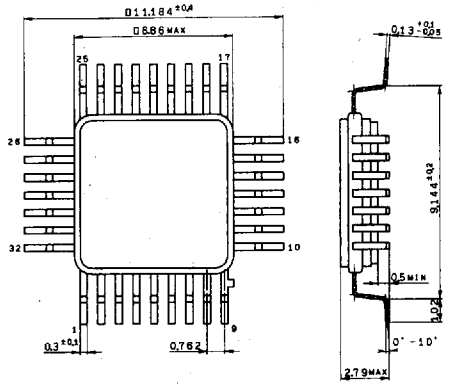
24pin QFP (QFP-24M-L02)

24pin QFP (Metal) 0.3g



32pin QFP (QFP-32M-L02)

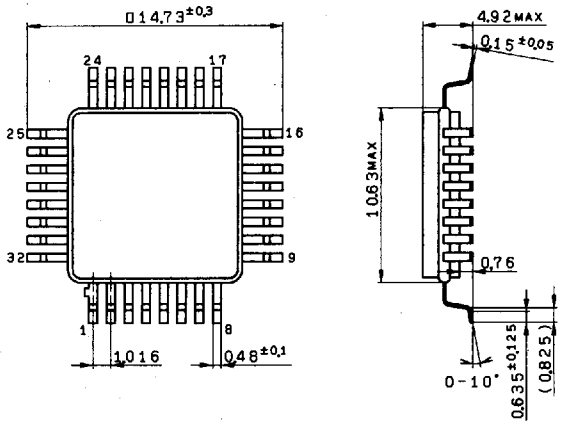
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	———

32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



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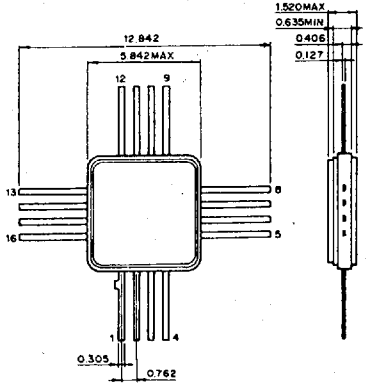
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	———

16pin QFP



Package Data

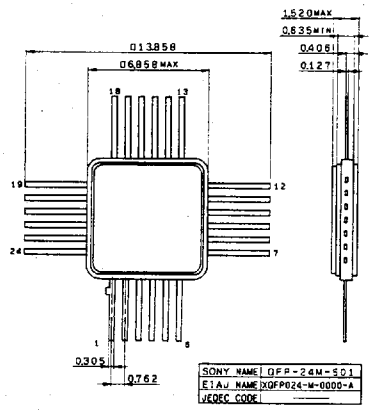
Package Data

T-90-20

Package Outline Uuit: mm

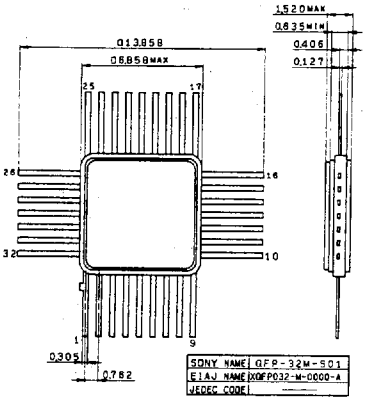
24pin QFP (QFP-24M-S01)

24pin QFP (Metal) 0.3g



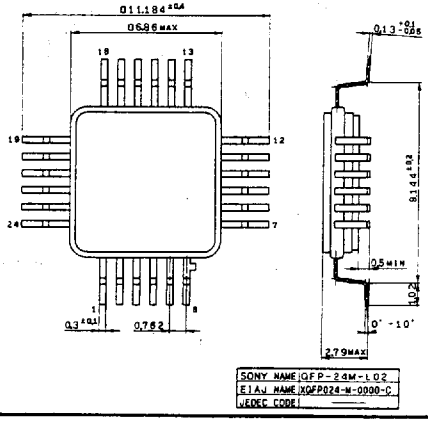
32pin QFP (QFP-32M-S01)

32pin QFP (Metal) 0.2g



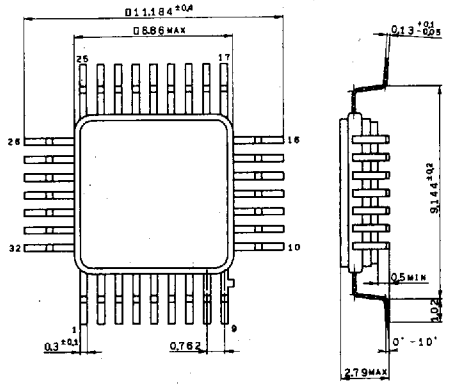
24pin QFP (QFP-24M-L02)

24pin QFP (Metal) 0.3g



32pin QFP (QFP-32M-L02)

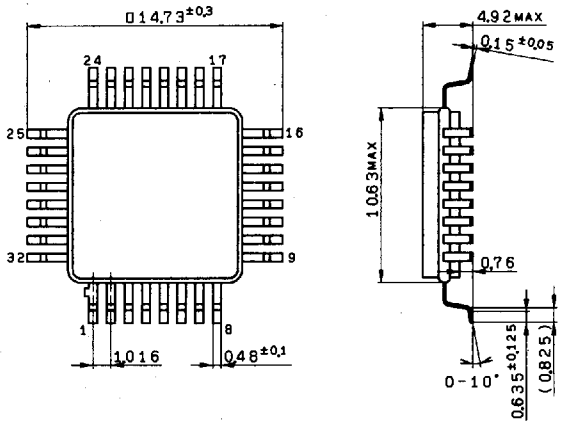
32pin QFP (Metal) 0.2g



SONY NAME	QFP-32M-L02
EIAJ NAME	XQFP032-M-0000-C
JEDEC CODE	———

32pin QFP (QFP-32C-L01)

32pin QFP (Ceramic)



SONY NAME	QFP-32C-L01
EIAJ NAME	XQFP032-G-0000-A
JEDEC CODE	———

16pin QFP