

CG31 Series 0.8-micron CMOS Gate Arrays

DESCRIPTION

The CG31 series of 0.8-µm CMOS gate arrays are currently available in three device types with from 120K to 200K gates. These arrays achieve the ultra fast speed of 0.37 ps per gate. Thanks to the channelless (sea-of-gates) structure of the CG31 gate array, CG31 basic cells can be used for logic cells, memory cells, or wiring area in order to implement the desired functions. The full utilization of the array surface and the three-layer metal interconnect technology produce a 65 percent maximum gate usability ratio.

The logic and I/O cells for the CG31 series are functionally compatible with Fujitsu's AU, UHB, CG10, and CG21 series of gate arrays to simplify upgrading. User-specifiable RAM and ROM configurations are also available. These gate arrays facilitate the implementation of large-scale devices such as computers and graphic processors on single chips.

FEATURES

- 0.8 micron CMOS sea-of-gates technology
 - 3 layer metal interconnect
- Ultra high speed
 - 0.37 ns/gate for 2-input NAND with F/O = 2
 - -0.55 ns/gate for power 2-input NAND with F/O = 2
- High basic cell usage
 - 65% maximum for logic with RAM/ROM
 - 55% maximum for logic only
- High sink current capability
 - sink current up to 12 mA, 24 mA planned
- Minimum delay clock buffer true option
- · High current clock drivers
 - Low-skew clock signal distribution

- Extensive unit cell library (logic cell, RAM, ROM, PLA, etc.)
 - Unit cells functionally compatible with Fujitsu's AU, UHB, CG10, and CG21 series gate arrays
- Automatic test pattern generation optional with Fujitsu scan testing
- On-chip pull-up/pull-down resistors
- High pin count ceramic packages
- High-density RAM and ROM compilers
 - up to 18K bit RAM block
 - up to 64K ROM block

PRODUCT FAMILY

Device	Available BCs (2-input gate +4 N-ch Tr)	Usable Logic Basic Cells (55% utilization)	Max Signal I/O
CG31134	129,540	71 K	300
CG31164	160,930	88 K	332
CG31204	210,188	115 K	332*

Note: * Package constrained

AVAILABLE PACKAGES¹

Package	CG31134	CG31164	CG31204	Type
PGA-135	•	•	0	Cavity up
PGA-155	0	0	0	Cavity down
PGA-179	•	•	0	Cavity up
PGA-208	•	•	0	Cavity up
PGA-223	0	0	0	Cavity down
PGA-256	•	•	0	Cavity up
PGA-299	0	0	0	Cavity down ²
PGA-321	0	0	0	Cavity down ²
PGA-361	0	0	0	Cavity down ²
PGA-401	_	0	0	Cavity down ²

Notes: ¹All packages are ceramic pin grid arrays (PGAs).

²These packages feature 70-mil interstitial pin
arrangement and metal heatspreader with optional
heatsink

= available

o = under development

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