REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R003-98.	97-10-31	Monica L. Poelking
B	Changes in accordance with NOR 5962-R042-98.	98-02-26	Monica L. Poelking
B	Add radiation features in section 1.4. In table IA: Change test conditions of V_{IN} for I_{IL} and I_{LI} tests; add I_{IL} and I_{LI} tests for XTAL1 input; add footnote 7/ to t_{CHCX}, t_{CLCX}, t_{CLCH}, and t_{CHCL}; change footnote 6/. Add pin connections for case outline Y in figure 5. Editorial changes throughout. - TVN	99-07-26	Monica L. Poelking
D	Update the boilerplate in accordance with the requirements of MIL-PRF-38535. – TVN	01-04-11	Thomas M. Hess

REV																				
SHEET																				
REV	C	C	C	C	D	C	C	D	C	C	C	D	C	C	C					
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29					

REV STATUS OF SHEETS																	
REV	D	C	D	C	D	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY Thomas M. Hess	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Thomas M. Hess APPROVED BY Monica L. Poelking DRAWING APPROVAL DATE 95-12-13 REVISION LEVEL **D**	MICROCIRCUIT, DIGITAL, RADIATION HARDENED, 8-BIT MICROCONTROLLER, MONOLITHIC SILICON SIZE **A** / CAGE CODE **67268** / **5962-95638** SHEET 1 OF 29

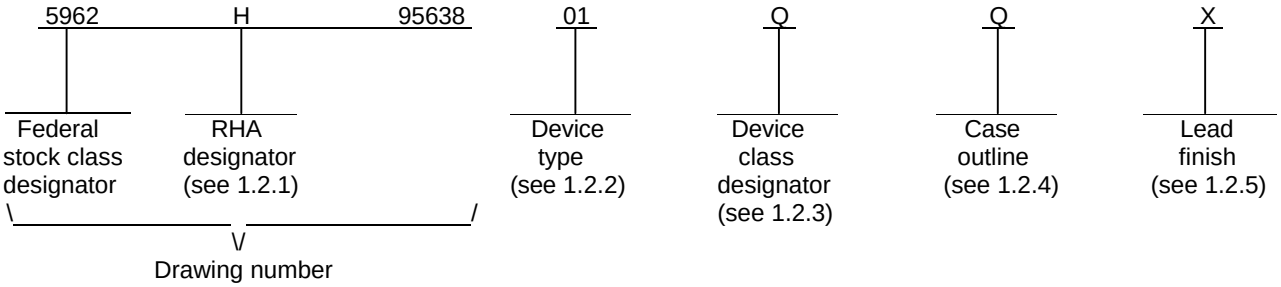
DSCC FORM 2233
APR 97

5962-E367-01

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	69RH051	Radiation hardened 8-bit microcontroller

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line package
Y	See figure 1	44	Quad flatpack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Input voltage, V_{DD} to V_{SS}	-0.5 V dc to +7.0 V dc
Voltage on any pin to V_{SS}	-0.5 V dc to V_{CC} + 0.3 V dc
I_{OL} per output pin	15 mA
Maximum power dissipation (P_D)	750 mW
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Maximum junction temperature (T_J)	175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	+4.5 V dc to +5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Radiation features:	
Total dose (50 rads(Si)/s ≤ dose rate ≤ 300 rads(Si)/s)	≥ 1 x 10^6 rads(Si)
Single event phenomenon (SEP) effective	
LET, no upsets	≤ 14 MeV/(mg/cm^2)
LET, no latchup	≤ 126 MeV/(mg/cm^2)
Dose rate upset (20 ns pulse)	2/
Dose rate latchup	2/
Dose rate survivability	2/
Neutron irradiated	2/

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	94.92 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ When characterized as a result of the procuring activities request, the condition will be specified.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational sevices.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figures 4.

3.2.5 Radiation exposure connections. The radiation exposure connecttions shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Low level input voltage, (except $\overline{EA}$ input)	V_{IL1}		All	1, 2, 3		0.8	V
Low level input voltage, $\overline{EA}$ input only	V_{IL2}		All	1, 2, 3		0.8	
High level input voltage (except XTAL, RST)	V_{IH1}		All	1, 2, 3	2.0		
High level intput voltage, XTAL, RST	V_{IH2}		All	1, 2, 3	3.85		
Low level output voltage (ports 1, 2 and 3) 2/ 3/	V_{OL1}	V_{DD} = 4.5 V, I_{OL} = 100 µA	All	1, 2, 3		0.3	
		V_{DD} = 4.5 V, I_{OL} = 1.6 mA				0.45	
		V_{DD} = 4.5 V, I_{OL} = 3.5 mA				1.0	
Low level output voltage (port 0, ALE/$\overline{PROG}$, $\overline{PSEN}$) 2/ 3/	V_{OL2}	V_{DD} = 4.5 V, I_{OL} = 200 µA	All	1, 2, 3		0.3	
		V_{DD} = 4.5 V, I_{OL} = 3.2 mA				0.45	
		V_{DD} = 4.5 V, I_{OL} = 7.0 mA				1.0	
High level output voltage (ports 1, 2, 3, ALE/$\overline{PROG}$, $\overline{PSEN}$) 2/ 4/	V_{OH1}	V_{DD} = 4.5 V, I_{OH} = -10 µA	All	1, 2, 3	4.2		
		V_{DD} = 4.5 V, I_{OH} = -30 µA			3.8		
		V_{DD} = 4.5 V, I_{OH} = -60 µA			3.0		
High level output voltage (port 0 in external bus mode)	V_{OH2}	V_{DD} = 4.5 V, I_{OH} = -200 µA	All	1, 2, 3	4.2		
		V_{DD} = 4.5 V, I_{OH} = -3.2 mA			3.8		
		V_{DD} = 4.5 V, I_{OH} = -7.0 mA			3.0		
Logic 0 input current (ports 1, 2, and 3)	I_{IL1}	V_{DD} = 5.5 V V_{IN} = 0.0 V	All	1, 2, 3		-50	µA
Logic 0 input current (XTAL1)	I_{IL2}	V_{DD} = 5.5 V V_{IN} = 0.0 V	All	1, 2, 3		-65	µA
Input leakage current (port 0)	I_{LI1}	V_{DD} = 5.5 V V_{IN} = 0.0 V or V_{DD}	All	1, 2, 3		±25	µA
Input leakage current (XTAL1)	I_{LI2}	V_{DD} = 5.5 V V_{IN} = 0.0 V or V_{DD}	All	1, 2, 3		±65	µA
RST pulldown resistor (except $\overline{EA}$) 5/	R_{RST}		All	1, 2, 3	10	225	kΩ
Power supply current 6/	I_{DD}	f = 16 MHz	All	4, 5, 6		95	mA
		f = 20 MHz				120	
Pin capacitance	C_{IO}	f = 1 MHz, T_A = 25°C See 4.4.1c	All	4		15	pF
Functional tests		See 4.4.1b	All	7, 8			

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Clock period	t_{CLCL}	V_{DD} = 4.5 V See figure 4	All	9, 10, 11	50		ns
Oscillator frequency	$1/t_{CLCL}$		All	9, 10, 11		20	
ALE pulse width	t_{LHLL}		All	9, 10, 11	$2t_{CLCL}$-40		
Address valid to ALE low	t_{AVLL}		All	9, 10, 11	t_{CLCL}-40		
Address hold after ALE low 7/	t_{LLAX}		All	9, 10, 11	t_{CLCL}-30		
ALE low to valid instruction in	t_{TLLIV}		All	9, 10, 11		$4t_{CLCL}$-100	
ALE low to $\overline{PSEN}$ low	t_{LLPL}		All	9, 10, 11	t_{CLCL}-30		
$\overline{PSEN}$ pulse width	t_{PLPH}		All	9, 10, 11	$3t_{CLCL}$-45		
$\overline{PSEN}$ low to valid instruction low	t_{PLIV}		All	9, 10, 11		$3t_{CLCL}$-105	
Input instruction hold after $\overline{PSEN}$ 7/	t_{PXIX}		All	9, 10, 11	0		
Input instruction float after $\overline{PSEN}$ 7/	t_{PXIZ}		All	9, 10, 11		t_{CLCL}-25	
Address to valid instruction in	t_{AVIV}		All	9, 10, 11		$5t_{CLCL}$-105	
$\overline{PSEN}$ low address float 7/	t_{PLAZ}		All	9, 10, 11		10	
$\overline{RD}$ pulse width	t_{RLRH}		All	9, 10, 11	$6t_{CLCL}$-100		
$\overline{WR}$ pulse width	t_{WLWH}		All	9, 10, 11	$6t_{CLCL}$-100		
$\overline{RD}$ low to valid data in	t_{RLDV}		All	9, 10, 11		$5t_{CLCL}$-165	
Data hold after $\overline{RD}$ 7/	t_{RHDX}		All	9, 10, 11	0		
Data float after $\overline{RD}$ 7/	t_{RHDZ}		All	9, 10, 11		$2t_{CLCL}$-60	
ALE low to valid data in	t_{LLDV}		All	9, 10, 11		$8t_{CLCL}$-150	
Address to valid data in	t_{AVDV}		All	9, 10, 11		$9t_{CLCL}$-165	
ALE low to $\overline{RD}$ or $\overline{WR}$ low	t_{LLWL}		All	9, 10, 11	$3t_{CLCL}$-50	$3t_{CLCL}$+50	
Address valid to $\overline{WR}$ low	t_{AVWL}		All	9, 10, 11	$4t_{CLCL}$-130		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{DD} \le 5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Data valid before $\overline{WR}$	t_{QVWX}	V_{DD} = 4.5 V See figure 4	All	9, 10, 11	t_{CLCL}-33		ns
Data hold after $\overline{WR}$	t_{WHQX}		All	9, 10, 11	t_{CLCL}-33		
Data valid to $\overline{WR}$ high	t_{QVWH}		All	9, 10, 11	$7t_{CLCL}$-150		
$\overline{RD}$ low to address float 7/	t_{RLAZ}		All	9, 10, 11		0	
$\overline{RD}$ or $\overline{WR}$ high to ALE high	t_{WHLH}		All	9, 10, 11	t_{CLCL}-40	t_{CLCL}+40	
Serial port clock period 7/	t_{XLXL}		All	9, 10, 11	$12t_{CLCL}$-10	$12t_{CLCL}$+10	
Output data setup to clock rising edge	t_{QVXH}		All	9, 10, 11	$10t_{CLCL}$-133		
Output data hold after clock rising edge	t_{XHQX}		All	9, 10, 11	$2t_{CLCL}$-70		
Input data hold after clock rising edge 7/	t_{XHDX}		All	9, 10, 11	0		
Clock rising edge to input data valid	t_{XHDV}		All	9, 10, 11		$10t_{CLCL}$-133	
High time 7/	t_{CHCX}		All	9, 10, 11	16		
Low time 7/	t_{CLCX}		All	9, 10, 11	16		
Rise time 7/	t_{CLCH}		All	9, 10, 11		20	
Fall time 7/	t_{CHCL}		All	9, 10, 11		20	

1/ Devices supplied to this drawing have been characterized through all levels M, D, L, R, F, G and H of irradiation. However, this device is only tested at the 'H' level. Pre and Post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C ±5°C. All parameters are tested to worst case conditions unless otherwise specified.

2/ Under steady state (nontransient) conditions, I_{OL} must be limited extrnally as follows:

Maximum I_{OL} per port pin:	10 mA
Maximum I_{OL} per 8-bit port:	
Port 0:	26 mA
Ports 1,2, and 3:	15 mA
Maximum total I_{OL} for all output pins:	71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

3/ Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1 to 0 transitions during bus operations. In applications where capacitance loading exceeds 100 pF, the noise pulse on the ALE may exceed 0.8 V. In these cases, it may be desirable to qualify ALE with a schmitt trigger or use an address latch with a schmitt trigger strobe input.

TABLE IA. Electrical performance characteristics - Continued.

4/ Capacitive loading on ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the V_{DD} - 0.3 V specification when the address lines are stabilizing.

5/ R_{RST}(typical) = 50 kΩ.

6/ I_{DD} is measured with all output pins disconnected and only only at points where electrical parameters and read and record in accordance with MIL-STD-883, method 5004, table I, footnote 7. XTAL1 is driven with $t_{CLCH} = t_{CHCL} \leq 5$ ns, $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$ measured with $\overline{EA}$ and RST connected to V_{DD}.

7/ Guaranteed but not 100% tested.

TABLE IB. SEP test limits. 1/ 2/

Device type	T_A = Temperature ±10°C 3/	V_{DD} = 4.5 V		Bias for latch-up test V_{DD} = 5.5 V no latch-up LET = 3/
		Effective LET no upsets [MeV/(mg/cm^2)]	Maximum device cross section (μm$^{2)}$ (LET = 126)	
All	+25°C	14	1.0×10^{-4}	126

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verfication supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Test at worst case temperature T_A = +100°C.

Case Y

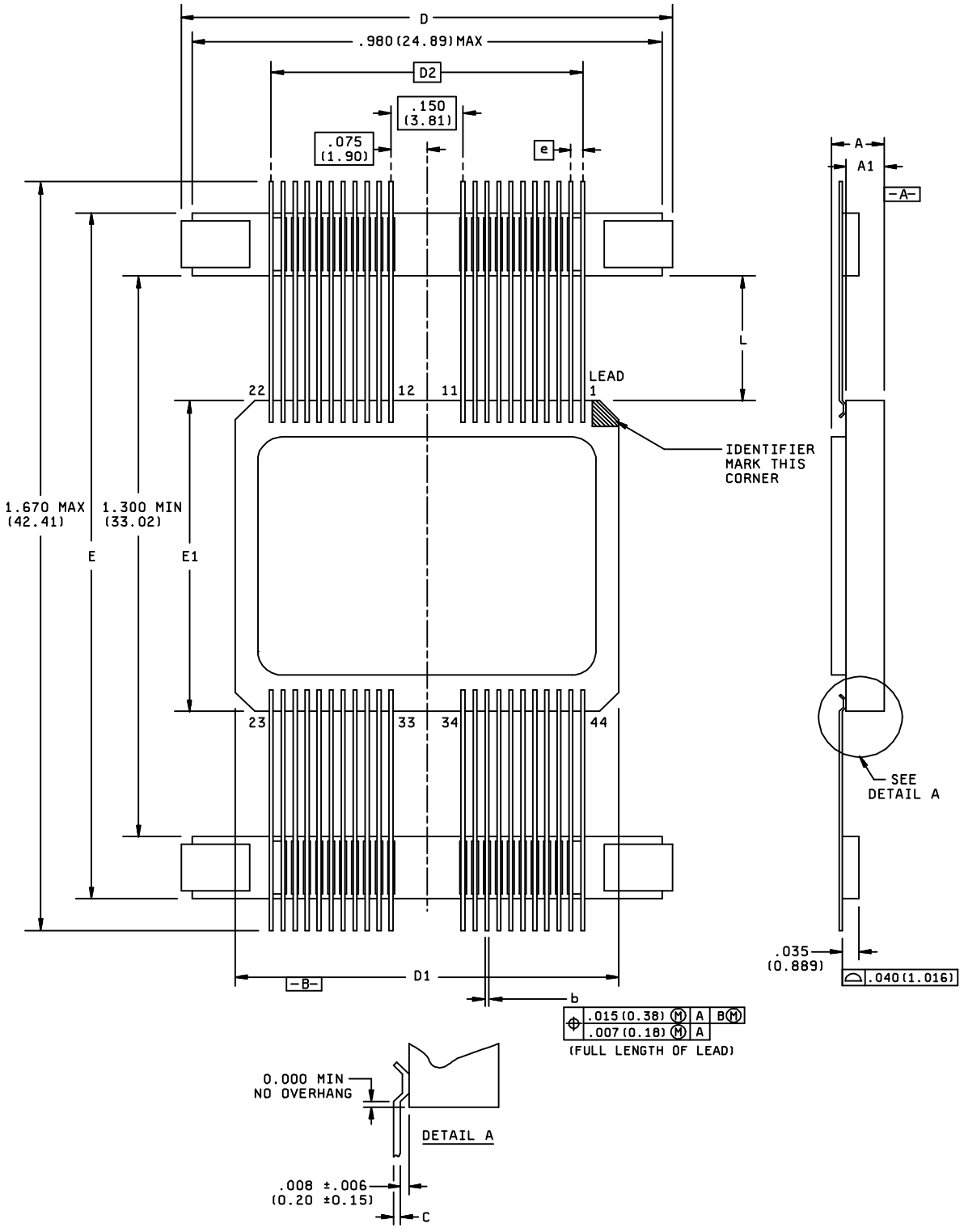


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE **A**		**5962-95638**
		REVISION LEVEL C	SHEET 10

Case Y				
Dimension	Millimeters		Inches	
	Min	Max	Min	Max
A		2.794		.110
A1	1.829	2.235	.072	.088
b	0.152	0.254	.006	.010
C	0.102	0.203	.004	.008
D	25.400	27.432	1.000	1.080
D1	20.117	20.523	.792	.808
D2	16.51 BSC		.650 BSC	
E		40.64		1.600
E1	16.84	17.196	.663	.677
L	6.858		.270	
e	0.635 BSC		.025 BSC	

NOTE: The US government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outline - Continued.

Device type	All		
Case outline	Q		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	P1.0 (T2)	21	P2.0 (A8)
2	P1.1 (T2EX)	22	P2.1 (A9)
3	P1.2 (ECI)	23	P2.2 (A10)
4	P1.3 (CEX0)	24	P2.3 (A11)
5	P1.4 (CEX1)	25	P2.4 (A12)
6	P1.5 (CEX2)	26	P2.5 (A13)
7	P1.6 (CEX3)	27	P2.6 (A14)
8	P1.7 (CEX4)	28	P2.7 (A15)
9	RST	29	$\overline{\text{PSEN}}$
10	P3.0 (RXD)	30	ALE
11	P3.1 (TXD)	31	$\overline{\text{EA}}$
12	P3.2 ($\overline{\text{INT0}}$)	32	P0.7 (AD7)
13	P3.3 ($\overline{\text{INT1}}$)	33	P0.6 (AD6)
14	P3.4 (T0)	34	P0.5 (AD5)
15	P3.5 (T1)	35	P0.4 (AD4)
16	P3.6 ($\overline{\text{WR}}$)	36	P0.3 (AD3)
17	P3.7 ($\overline{\text{RD}}$)	37	P0.2 (AD2)
18	XTAL2	38	P0.1 (AD1)
19	XTAL1	39	P0.0 (AD0)
20	V_{SS}	40	V_{DD}

FIGURE 2. Terminal connections.

Device type	All		
Case outline	Y		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{SS}	23	V_{DD}
2	P1.0 (T2)	24	NC
3	P1.1 (T2EX)	25	P2.0 (A8)
4	NC	26	P2.1 (A9)
5	P1.2 (ECI)	27	P2.2 (A10)
6	P1.3 (CEX0)	28	P2.3 (A11)
7	P1.4 (CEX1)	29	P2.4 (A12)
8	P1.5 (CEX2)	30	P2.5 (A13)
9	P1.6 (CEX3)	31	P2.6 (A14)
10	P1.7 (CEX4)	32	P2.7 (A15)
11	RST	33	$\overline{\text{PSEN}}$
12	P3.0 (RXD)	34	ALE
13	P3.1 (TXD)	35	$\overline{\text{EA}}$
14	P3.2 ($\overline{\text{INT0}}$)	36	P0.7 (AD7)
15	P3.3 ($\overline{\text{INT1}}$)	37	P0.6 (AD6)
16	P3.4 (T0)	38	P0.5 (AD5)
17	P3.5 (T1)	39	P0.4 (AD4)
18	P3.6 ($\overline{\text{WR}}$)	40	P0.3 (AD3)
19	P3.7 ($\overline{\text{RD}}$)	41	P0.2 (AD2)
20	XTAL2	42	P0.1 (AD1)
21	XTAL1	43	P0.0 (AD0)
22	V_{SS}	44	V_{DD}

NC = No connection

FIGURE 2. Terminal connections - Continued.

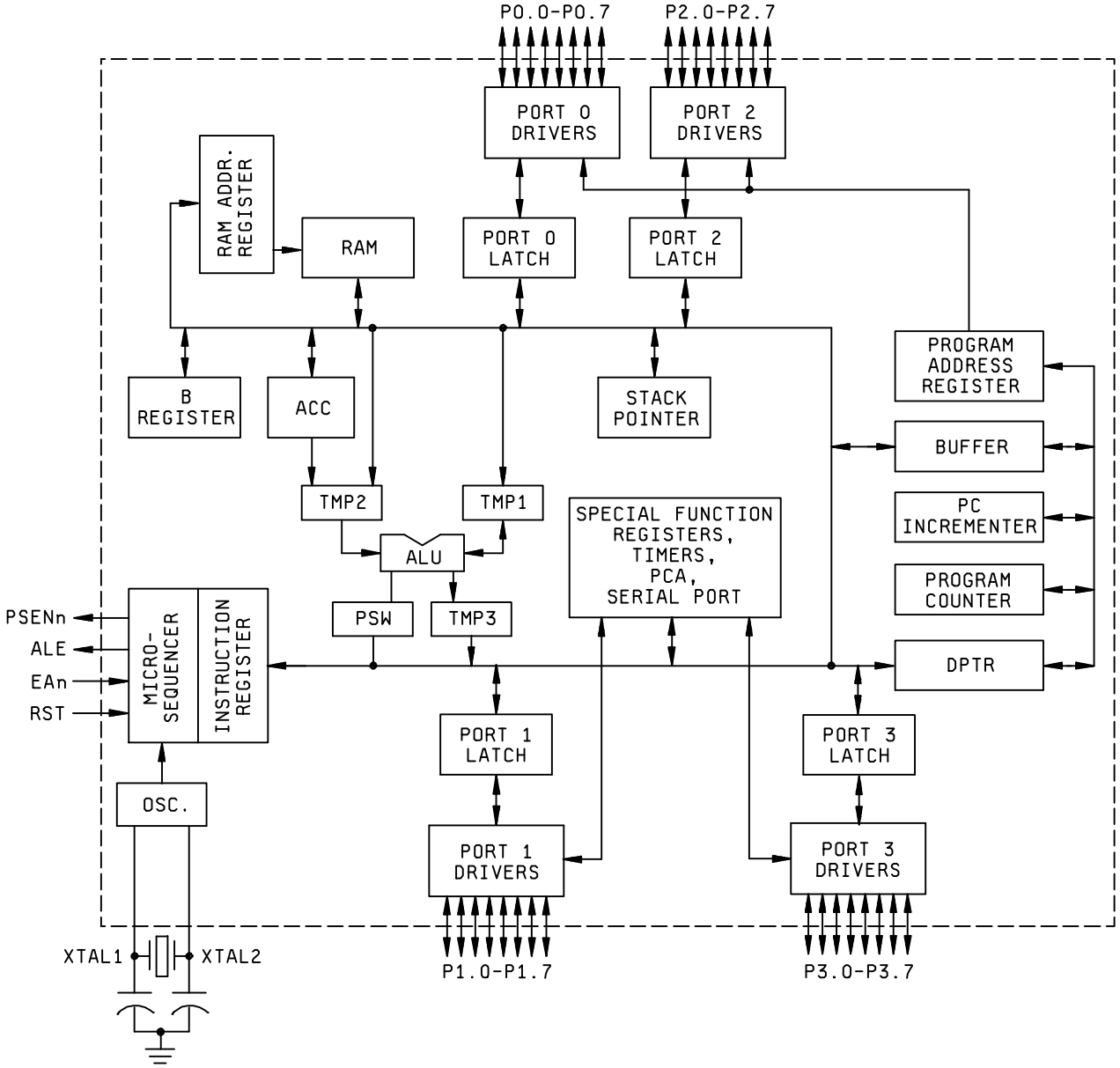
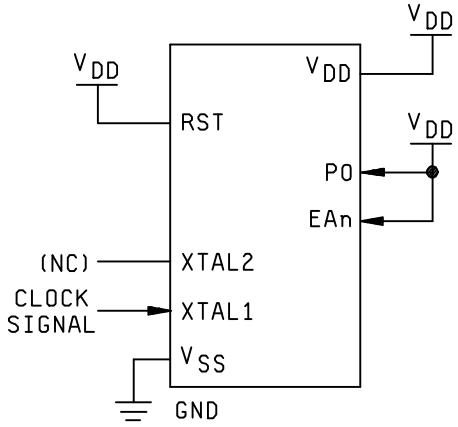
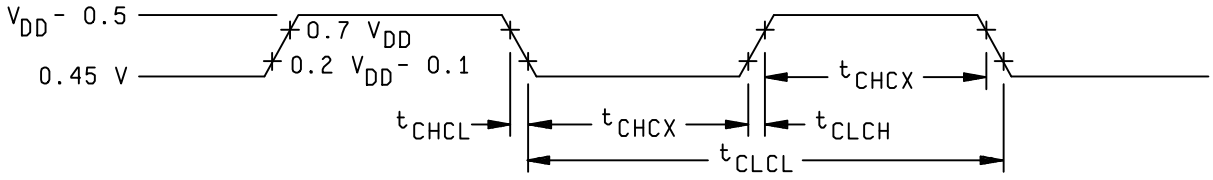


FIGURE 3. Block diagram.



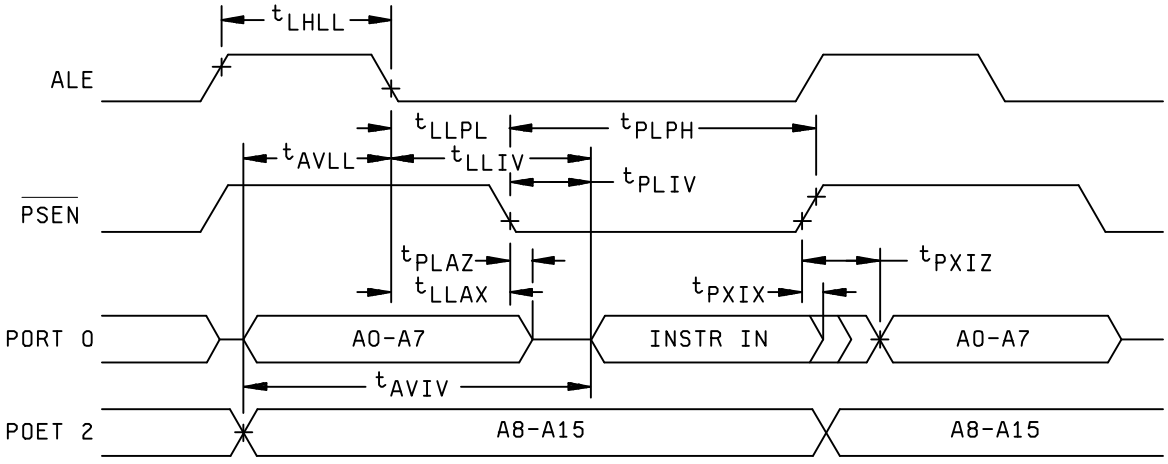
ALL OTHER PINS DISCONNECTED

$t_{CLCH} = t_{CHCL} = 5$ ns

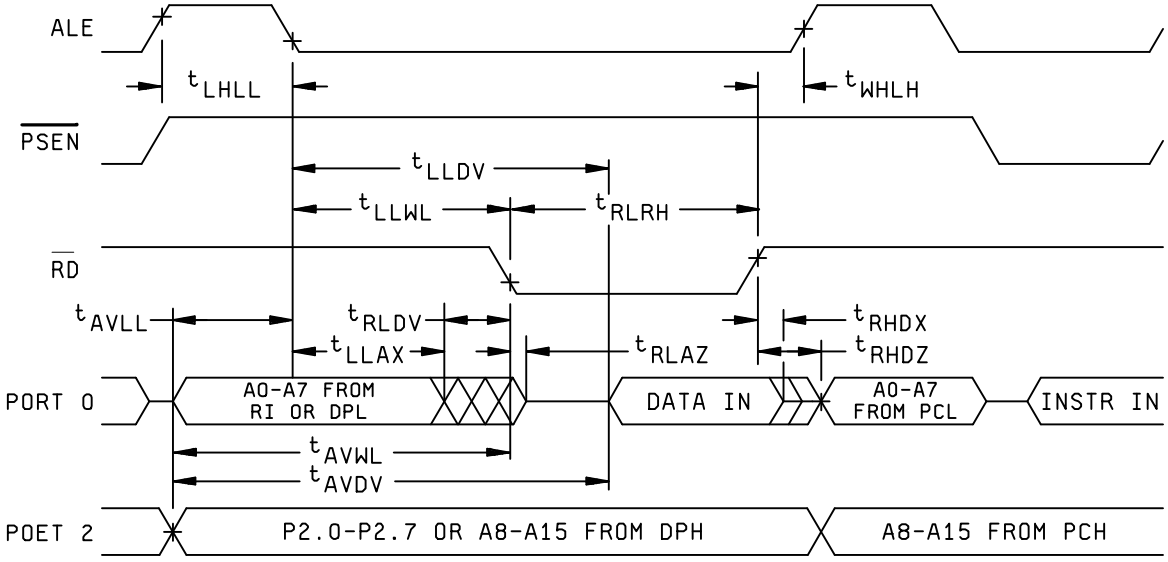


EXTERNAL CLOCK DRIVE

FIGURE 4. Test circuit and timing waveforms.

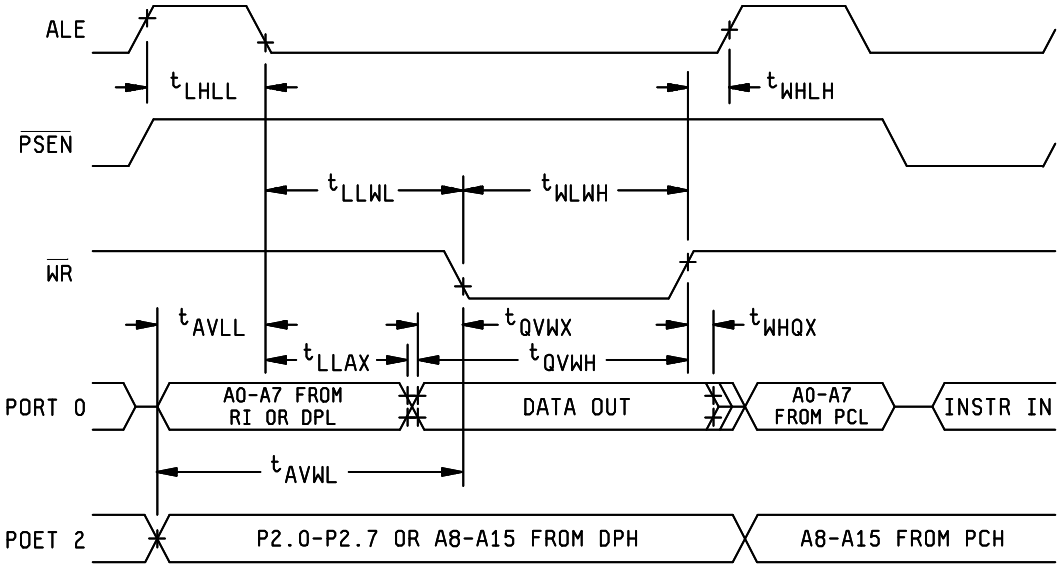


EXTERNAL PROGRAM MEMORY READ

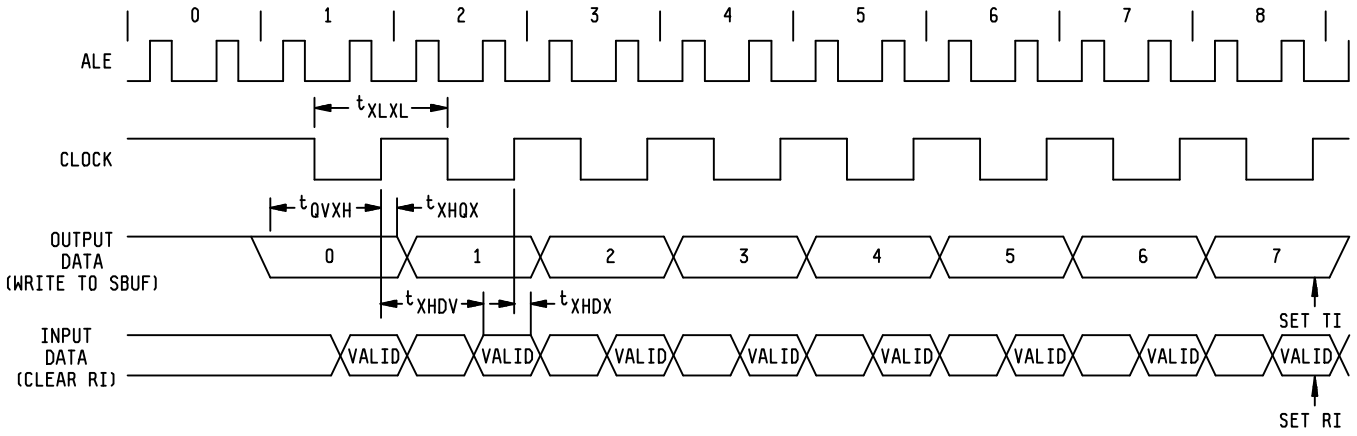


EXTERNAL DATA MEMORY READ CYCLE

FIGURE 4. Test circuit and timing waveforms - Continued.



EXTERNAL DATA MEMORY WRITE CYCLE



SERIAL PORT TIMING WAVEFORMS

FIGURE 4. Test circuit and timing waveforms - Continued.

Case outline	Open	V_{DD} = 5 V ± 0.5 V	Ground
Q		1, 2, 3, 4, 5, 6, 7, 8, 10, 11, 12, 13, 14, 15, 16, 17, 18, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 32, 33, 34, 35, 36, 37, 38, 39, 40	9, 19, 20, 31
Y	4, 24	2, 3, 5, 6, 7, 8, 9, 10, 12, 13, 14, 15, 16, 17, 18, 19, 20, 23, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 36, 37, 38, 39, 40, 41, 42, 43, 44	1, 11, 21, 22, 35

NOTE: Each pin except 20 and 40 for case outline Q and 1, 4, 22, 23, 24, and 44 for case outline Y will have a resistor of 2.49 kΩ ± 5% for irradiation testing.

FIGURE 5. Radiation exposure connections.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IO} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample of 5 devices with zero failures shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 1/	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 1/	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein (see 1.4).

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (see 1.4). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein (see 1.4).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices (see 1.4). SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^6$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be V_{DD} = 4.5 V dc for the upset measurements and V_{DD} = 5.5 V dc for the latchup measurements.

g. For SEP test limits, see table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

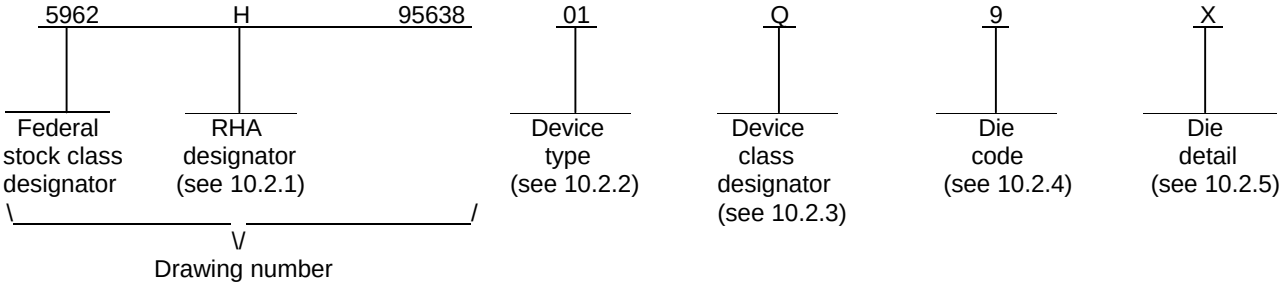
e. Occurrence of latchup (SEP).

APPENDIX A FORMS A PART OF SMD 5962-95638

10. SCOPE

10.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

10.2 PIN. The PIN is as shown in the following example:



10.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

10.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	69RH051	Radiation hardened 8-bit microcontroller

10.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

10.2.4 Die code. The die code designator shall be a number 9 for all devices supplied as die only with no case outline.

10.2.5. Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

10.2.5.1 Die physical dimensions.

Die type	Figure number
01	A-1

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10.2.5.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1

10.2.5.3 Interface materials.

Die type	Figure number
01	A-1

10.2.5.4 Assembly related information.

Die type	Figure number
01	A-1

10.3. Absolute maximum ratings.

See paragraph 1.3 within the body of this drawing for details.

10.4 Recommended operating conditions.

See paragraph 1.4 within the body of this drawing for details.

20. APPLICABLE DOCUMENTS.

20.1 Government specifications, standards, bulletin, and handbooks. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity).

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20.2. Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

30. REQUIREMENTS

30.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit or function as described herein.

30.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

30.2.1 Die physical dimensions. The die physical dimensions shall be as specified in 10.2.5.1 and on figure A-1.

30.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in 10.2.5.2 and on figure A-1.

30.2.3 Interface materials. The interface materials for the die shall be as specified in 10.2.5.3 and on figure A-1.

30.2.4 Assembly related information. The assembly related information shall be as specified in 10.2.5.4 and figure A-1.

30.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

30.4 Electrical test requirements. The test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

30.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in 10.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

30.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

30.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

40. QUALITY ASSURANCE PROVISIONS

40.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit or function as described herein.

40.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for class V product using the criteria defined within MIL-STD-883 test method 5007.

b) 100% wafer probe (see paragraph 30.4).

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c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 test method 2010 or the alternate procedures allowed within MIL-STD-883 test method 5004.

40.3 Conformance inspection

40.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see 30.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table II herein.

50. Die carrier

50.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical, and electrostatic protection.

60. NOTES

60.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

60.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614) 692-0547.

60.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535 and MIL-STD-1331.

60.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see 30.6 herein) to DSCC-VA and have agreed to this drawing.

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 370 mils x 506 mils.
Die thickness: 17.5 ±1 mils.

Interface materials.
Top metallization: Si Al Cu 9 kA-12.5 kA
Backside metallization: None: Backgrind

Glassivation.
Type: PSG
Thickness: 9 kA ±2 kA

Substrate: EPI on single crystal silicon
Substrate potential: Tied to V_{DD}
Special assembly instructions: None

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Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME
1	-0.0004	0.2462	P1.0 (T2)
2	-0.0164	0.2462	P1.1 (T2EX)
3	-0.0324	0.2462	P1.2 (ECI)
4	-0.0484	0.2462	P1.3 (CEX0)
5	-0.0644	0.2462	V_{SS}
6	-0.0804	0.2462	V_{DD}
7	-0.0964	0.2462	P1.4 (CEX1)
8	-0.1124	0.2462	P1.5 (CEX2)
9	-0.1284	0.2462	P1.6 (CEX3)
10	-0.1444	0.2462	P1.7 (CEX4)
11	-0.1526	0.2462	RST
12	-0.1589	0.2462	P3.0 (RXD)
13	-0.1652	0.2462	V_{SS}
14	-0.1715	0.2462	V_{DD}
15	-0.1715	-0.2462	V_{DD}
16	-0.1652	-0.2462	V_{SS}
17	-0.1589	-0.2462	P3.1 (TXD)
18	-0.1526	-0.2462	P3.2 ($\overline{\text{INT0}}$)
19	-0.1444	-0.2462	P3.3 ($\overline{\text{INT1}}$)
20	-0.1284	-0.2462	P3.4 (T0)
21	-0.1124	-0.2462	P3.5 (T1)
22	-0.0964	-0.2462	P3.6 ($\overline{\text{WR}}$)
23	-0.0804	-0.2462	V_{DD}
24	-0.0644	-0.2462	V_{SS}
25	-0.0484	-0.2462	P3.7 ($\overline{\text{RD}}$)
26	-0.0324	-0.2462	XTAL2
27	-0.0164	-0.2462	XTAL1

NOTE: The die center is the coordinate origin (0,0).

FIGURE A-1

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Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME
28	-0.0004	-0.2462	P2.0 (A8)
29	0.0155	-0.2462	P2.1 (A9)
30	0.0315	-0.2462	P2.2 (A10)
31	0.0475	-0.2462	P2.3 (A11)
32	0.0635	-0.2462	V_{SS}
33	0.0795	-0.2462	V_{DD}
34	0.0955	-0.2462	P2.4 (A12)
35	0.1115	-0.2462	P2.5 (A13)
36	0.1275	-0.2462	P2.6 (A14)
37	0.1435	-0.2462	P2.7 (A15)
38	0.1517	-0.2462	$\overline{PSEN}$
39	0.1580	-0.2462	ALE
40	0.1643	-0.2462	V_{SS}
41	0.1706	-0.2462	V_{DD}
42	0.1706	0.2462	V_{DD}
43	0.1643	0.2462	V_{SS}
44	0.1580	0.2462	$\overline{EA}$
45	0.1517	0.2462	P0.7 (AD7)
46	0.1435	0.2462	P0.6 (AD6)
47	0.1275	0.2462	P0.5 (AD5)
48	0.1115	0.2462	P0.4 (AD4)
49	0.0955	0.2462	P0.3 (AD3)
50	0.0795	0.2462	V_{DD}
51	0.0635	0.2462	V_{SS}
52	0.0475	0.2462	P0.2 (AD2)
53	0.0315	0.2462	P0.1 (AD1)
54	0.0155	0.2462	P0.0 (AD0)

NOTE: The die center is the coordinate origin (0,0).

FIGURE A-1

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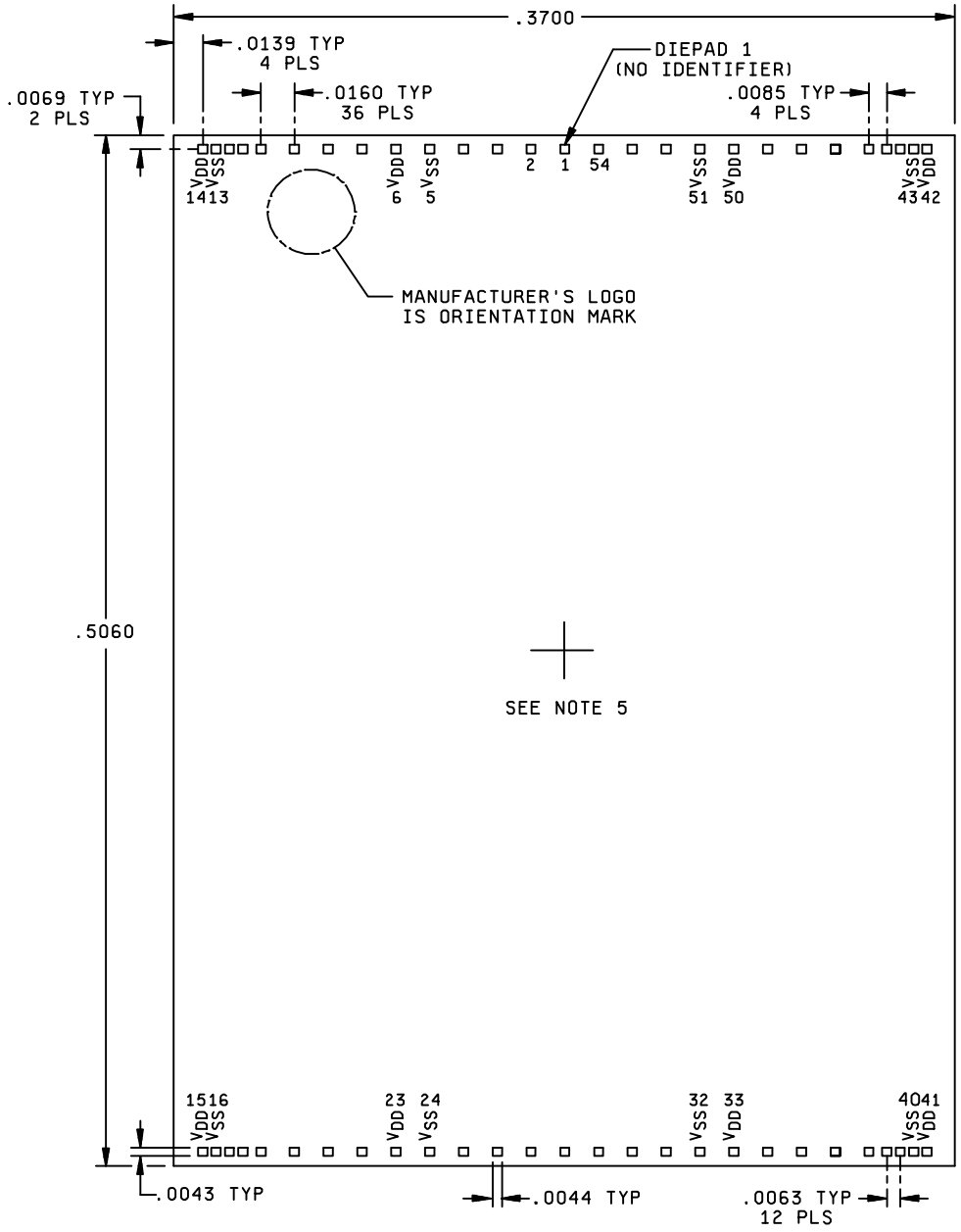

NOTES:
1. All dimensions are in inches and are basic.
2. Backside bias is V_{DD}.
3. Die thickness is 0.0175 ±0.001.
4. Die backside is lapped.
5. The die center is the coordinate origin (0,0).

FIGURE A-1

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-04-11

Approved sources of supply for SMD 5962-95638 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H9563801QQA	65342	UT69RH051PCA
5962H9563801QQC	65342	UT69RH051PCC
5962H9563801QYA	65342	UT69RH051WCA
5962H9563801QYC	65342	UT69RH051WCC
5962H9563801VQA	65342	UT69RH051PCA
5962H9563801VQC	65342	UT69RH051PCC
5962H9563801VYA	65342	UT69RH051WCA
5962H9563801VYC	65342	UT69RH051WCC
5962H9563801Q9A	65342	UT69RH051-Q DIE
5962H9563801V9A	65342	UT69RH051-V DIE

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	UTMC Microelectronics System Inc. 4350 Centennial Boulevard Colorado Springs, Colorado 80907-3486