Selectable Timeout Watchdog & V_{CC} Supervisory Circuit w/Serial E^2PROM

FEATURES

- **Selectable Timeout Watchdog Timer**
- **Low Vcc Detection and Reset Assertion**
  - **—Reset Signal Valid to Vcc=1V**
- **Save Critical Data With IDLock™ Memory**
  - **—IDLock First or Last Page, any 1/4 or Lower 1/2 of E^2PROM Array**
- **Long Battery Life With Low Power Consumption**
  - **—<50µA Max Standby Current, Watchdog On**
  - **—<1µA Max Standby Current, Watchdog Off**
  - **—<3mA Max Active Current during Write**
  - **—<400µA Max Active Current during Read**
- **1.8V to 3.6V, 2.7V to 5.5V and 4.5V to 5.5V Power Supply Versions**
- **5MHz Clock Rate**
- **Minimize Programming Time**
  - **—16 Byte Page Write Mode**
  - **—Self-Timed Write Cycle**
  - **—5ms Write Cycle Time (Typical)**
- **SPI Modes (0,0 & 1,1)**
- **Built-in Inadvertent Write Protection**
  - **—Power-Up/Power-Down Protection Circuitry**
  - **—Write Enable Latch**
  - **—Write Protect Pin**
- **High Reliability**
- **Available Packages**
  - **—8-Lead TSSOP**
  - **—8-Lead SOIC**

DESCRIPTION

These devices combine three popular functions, Watchdog Timer, Supply Voltage Supervision, and Serial E^2PROM Memory in one package. This combination lowers system cost, reduces board space requirements, and increases reliability.

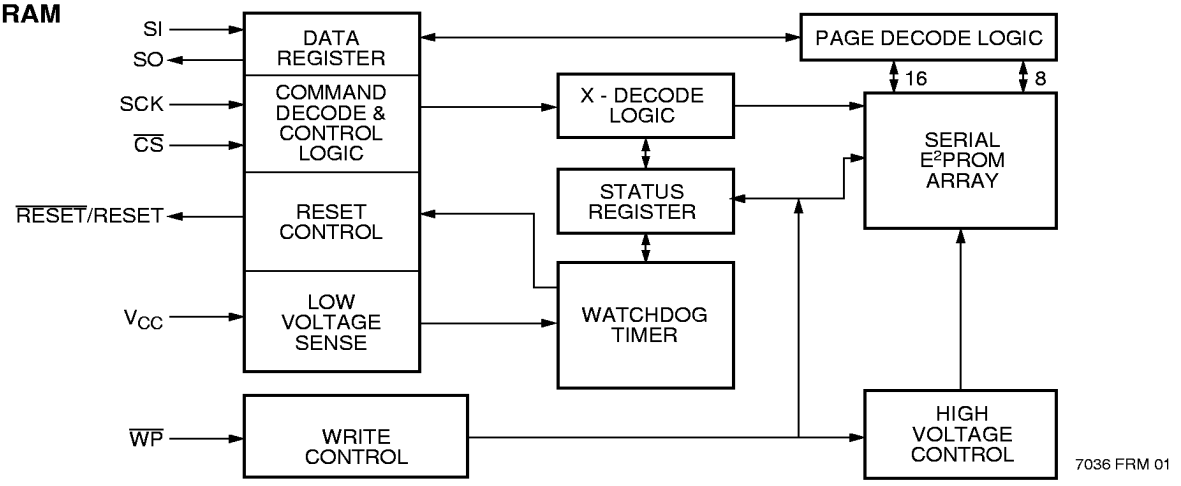
The Watchdog Timer provides an independent protection mechanism for microcontrollers. During a system failure, the device will respond with a $\overline{\text{RESET}}$/RESET signal after a selectable time-out interval. The user selects the interval from three preset values. Once selected, the interval does not change, even after cycling the power.

The user's system is protected from low voltage conditions by the device's low Vcc detection circuitry. When Vcc falls below the minimum Vcc trip point, the system is reset. $\overline{\text{RESET}}$/RESET is asserted until Vcc returns to proper operating levels and stabilizes.

The memory portion of the device is a CMOS Serial E^2PROM array with Xicor's IDLock Memory. The array is internally organized as x 8. The device features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple four-wire bus.

The device utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles per sector and a minimum data retention of 100 years.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is a serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the device is deselected and the SO output pin is at high impedance and unless a nonvolatile write cycle is underway, the device will be in the standby power mode. $\overline{CS}$ LOW enables the device, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

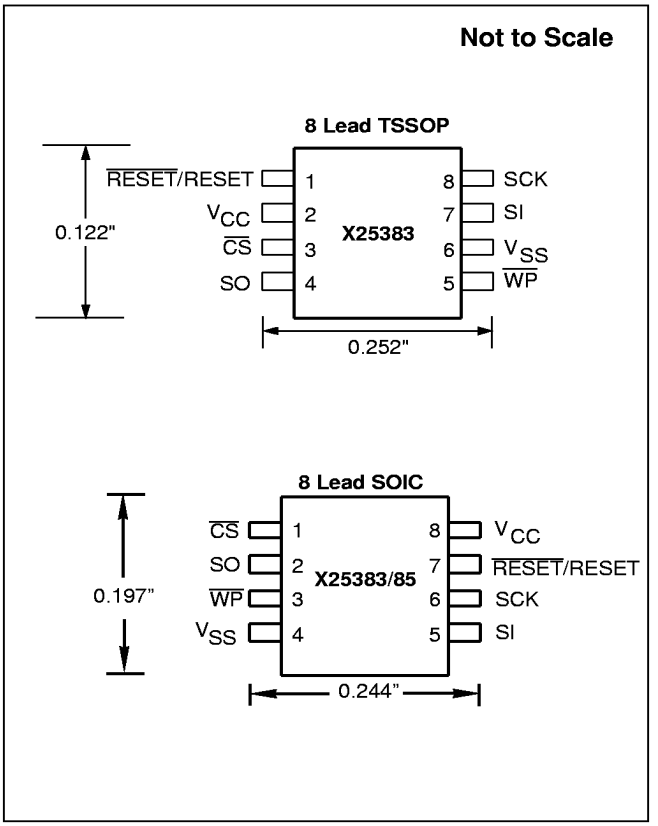
Write Protect ($\overline{WP}$)

When $\overline{WP}$ is LOW, nonvolatile writes to the device are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held HIGH, all functions, including nonvolatile writes operate normally. $\overline{WP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a write to the device. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no affect on this write.

Reset ($\overline{RESET}$/RESET)

$\overline{RESET}$/RESET is an active LOW/HIGH, open drain output which goes active whenever Vcc falls below the minimum Vcc sense level V_{trip}. It will remain active until Vcc rises above the minimum Vcc sense level for 200ms. $\overline{RESET}$/RESET will also go active if the Watchdog Timer is enabled and $\overline{CS}$ remains either HIGH or LOW longer than the selectable Watchdog time-out period. A falling edge of $\overline{CS}$ will reset the Watchdog Timer.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{RESET}$/RESET	Reset Output

PRINCIPLES OF OPERATION

The device is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of many popular microcontroller families.

The device monitors the bus and asserts $\overline{\text{RESET}}$/RESET output if there is no bus activity within user selctable time-out period or the supply voltage falls below a preset minimum V_{trip}. The device contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising edge of SCK. $\overline{\text{CS}}$ must be LOW during the entire operation.

All instructions (Table 1), addresses and data are transferred MSB first. Data input on the SI line is latched on the first rising edge of SCK after $\overline{\text{CS}}$ goes LOW. Data is output on the SO line by the falling edge of SCK. SCK is static, allowing the user to stop the clock and then start it again to resume operations where left off.

Write Enable Latch

The device contains a Write Enable Latch. This latch must be SET before a Write Operation is initiated. The WREN instruction will set the latch and the WRDI instruction will reset the latch (Figure 3). This latch is automatically reset upon a power-up condition and after the completion of a valid Write Cycle.

Status Register

The RDSR instruction provides access to the Status Register. The Status Register may be read at any time, even during a Write Cycle. The Status Register is formatted as follows:

Status Register/IDLock/WDT Byte

7	6	5	4	3	2	1	0
0	0	0	WD1	WD0	IDL2	IDL1	IDL0

IDLock Memory

Xicor's IDLock Memory provides a flexible mechanism to store and lock system ID and parametric information. There are seven distinct IDLock Memory areas within the array which vary in size from one page to as much as half of the entire array. These areas and associated address ranges are IDLocked by writing the appropriate two byte IDLock instruction to the device as described in Table 1 and Figure 7. Once an IDLock instruction has been completed, that IDLock setup is held in the nonvolatile Status Register until the next IDLock instruction is issued. The sections of the memory array that are IDLocked can be read but not written until IDLock Protection is removed or changed.

Watchdog Timer

The Watchdog Timer bits, WD0 and WD1, select the Watchdog Time-out Period. These nonvolatile bits are programmed with the WRSR instruction.

Status Register Bits		Watchdog Time-out (Typical)
WD1	WD0	
0	0	1.4 Seconds
0	1	600 Milliseconds
1	0	200 Milliseconds
1	1	Disabled

Read Sequence

When reading from the E^2PROM memory array, $\overline{\text{CS}}$ is first pulled low to select the device. The 8-bit READ instruction is transmitted to the device, followed by the 16-bit address. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to address $0000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{\text{CS}}$ high. Refer to the Read E^2PROM Array Sequence (Figure 1).

To read the Status Register, the $\overline{\text{CS}}$ line is first pulled low to select the device followed by the 8-bit RDSR instruction. After the RDSR opcode is sent, the contents of the Status Register are shifted out on the SO line. Refer to the Read Status Register Sequence (Figure 2).

Write Sequence

Prior to any attempt to write data into the device, the "Write Enable" Latch (WEL) must first be set by issuing the WREN instruction (Figure 3). $\overline{\text{CS}}$ is first taken LOW, then the WREN instruction is clocked into the device. After all eight bits of the instruction are transmitted, $\overline{\text{CS}}$ must then be taken HIGH. If the user continues the Write Operation without taking $\overline{\text{CS}}$ HIGH after issuing the WREN instruction, the Write Operation will be ignored.

To write data to the E^2PROM memory array, the user then issues the WRITE instruction followed by the 16 bit address and then the data to be written. Any unused address bits are specified to be "0's". The WRITE operation minimally takes 32 clocks. $\overline{\text{CS}}$ must go low and remain low for the duration of the operation. If the address counter reaches the end of a page and the clock contin-

ues, the counter will roll back to the first address of the same page and overwrite any data that may have been previously written.

For a Write Operation (byte or page write) to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of the last data byte to be written is clocked in. If it is brought HIGH at any other time, the write operation will not be completed (Figure 4).

To write to the Status Register, the WRSR instruction is followed by the data to be written (Figure 5). Data bits 5, 6 and 7 must be "0".

End of Write Detect

To speed the writing of the memory array an early end of write detection is provided. To detect the end of a nonvolatile write operation, simply read the status register. If the status register returns '0' in the first bit location, the write is complete. If the first status bit is a '1', then the write is still in progress. If the first bit read is a '1', the remaining bits are undefined. An alternative method of reading the end of write operation is to send the read status command, then monitor the SO line without toggling SCK. When SO goes from HIGH to LOW, the nonvolatile write has ended. To read the status bits requires that a new read status command be issued.

Read Status Operation

If there is no nonvolatile write in progress, the Read Status instruction returns the watchdog timer bits and the ID Lock bits from the Status Register. The watchdog timer bits specify the time-out period for the watchdog timer. The ID Lock bits define the ID Lock condition (Figure 1/ Table1). The other bits are reserved. See Figure 3.

$\overline{RESET}$/RESET Operation

The $\overline{RESET}$ (X25383) output is designed to go LOW whenever V_{CC} has dropped below the minimum trip point and/or the Watchdog timer has reached its programmable time-out limit.

The RESET (X25385) output is designed to go HIGH whenever V_{CC} has dropped below the minimum trip point and/or the watchdog timer has reached its programmable time-out limit.

The $\overline{RESET}$/RESET output is an open drain output and requires an external pull up resistor.

Operational Notes

The device powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The Write Enable Latch is reset.
- Reset Signal is active for t_{PURST}.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- A WREN instruction must be issued to set the Write Enable Latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a nonvolatile write cycle.

Table 1. Instruction Set and IDLock Protection Byte Definition

Instruction Format*	Instruction Name and Operation
0000 0110	WREN: Set the Write Enable Latch (Write Enable Operation)
0000 0100	WRDI: Reset the Write Enable Latch (Write Disable Operation)
0000 0001 **Note:** W1=WD1Bit W0=WD0Bit	**Write Status Instruction—followed by:** **IDLock/WDT Byte: (See Figure 1)** 000W_1 $W_2$000 --->NO IDLock: 00h-00h - - - - - - - >None of the Array 000W_1 $W_2$001 --->IDLock Q1: 0000h-00FFh - - - - >Lower Quadrant (Q1) 000W_1 $W_2$010 --->IDLock Q2: 0100h-01FFh - - - - >Q2 000W_1 $W_2$011 --->IDLock Q3: 0200h-02FFh - - - - >Q3 000W_1 $W_2$100 --->IDLock Q4: 0300h-03FFh - - - - >Upper Quadrant (Q4) 000W_1 $W_2$101 --->IDLock H1: 0000h-01FFh - - - - >Lower Half of the Array (H1) 000W_1 $W_2$110 --->IDLock P0: 0000h-000Fh - - - - >Lower Page (P0) 000W_1 $W_2$111 --->IDLock Pn: 03F0h-03FFh - - - - >Upper Page (Pn)
0000 0101	READ STATUS: Reads Status Register & provides write in progress status on SO Pin
0000 0010	WRITE: Write operation followed by address and data
0000 0011	READ: Read operation followed by address

*Instructions are shown with MSB in leftmost position. Instructions are transferred MSB first.

Figure 2. Read Operation Sequence

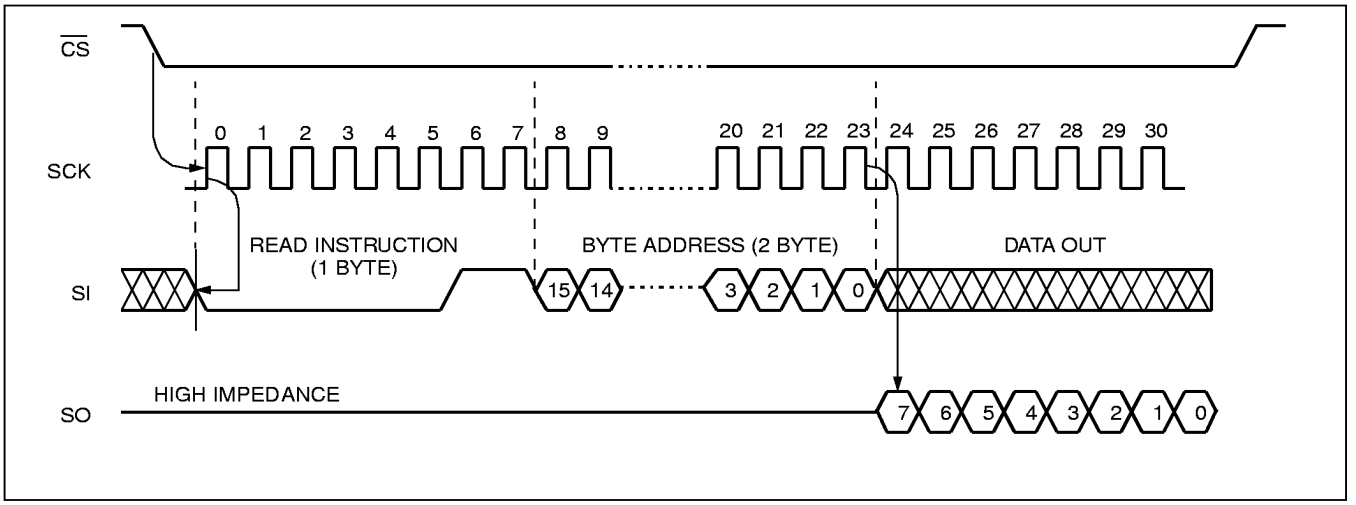


Figure 3. Read Status Register Operation Sequence

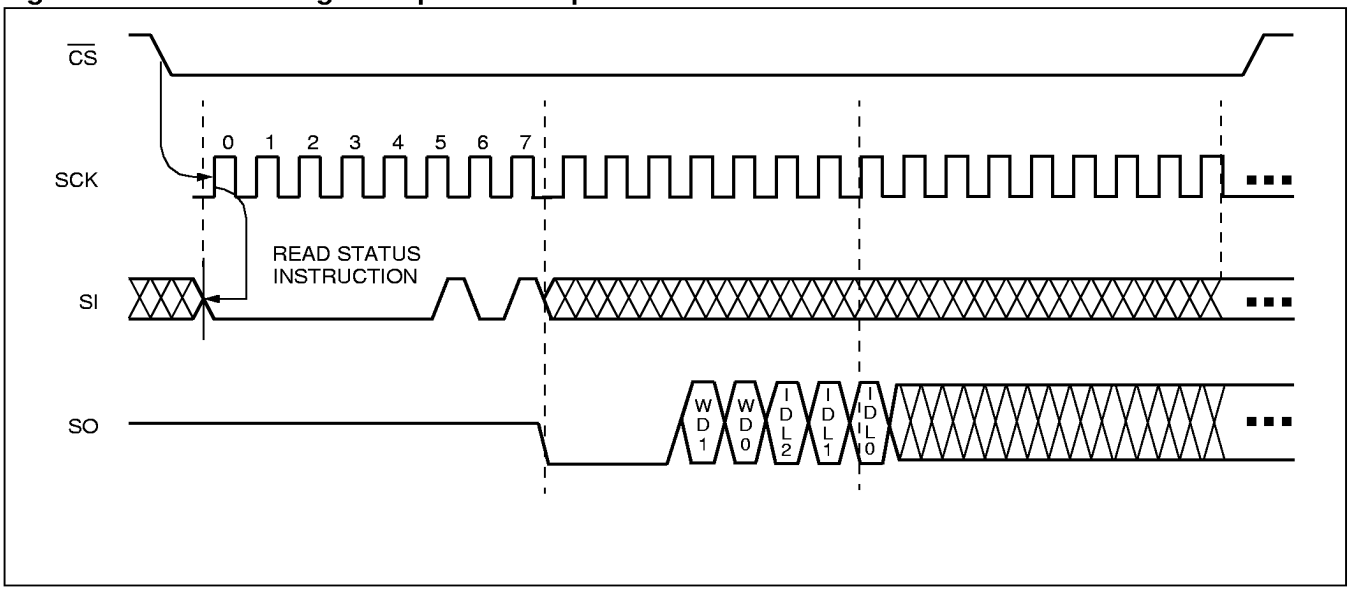


Figure 4. WREN/WRDI Sequence

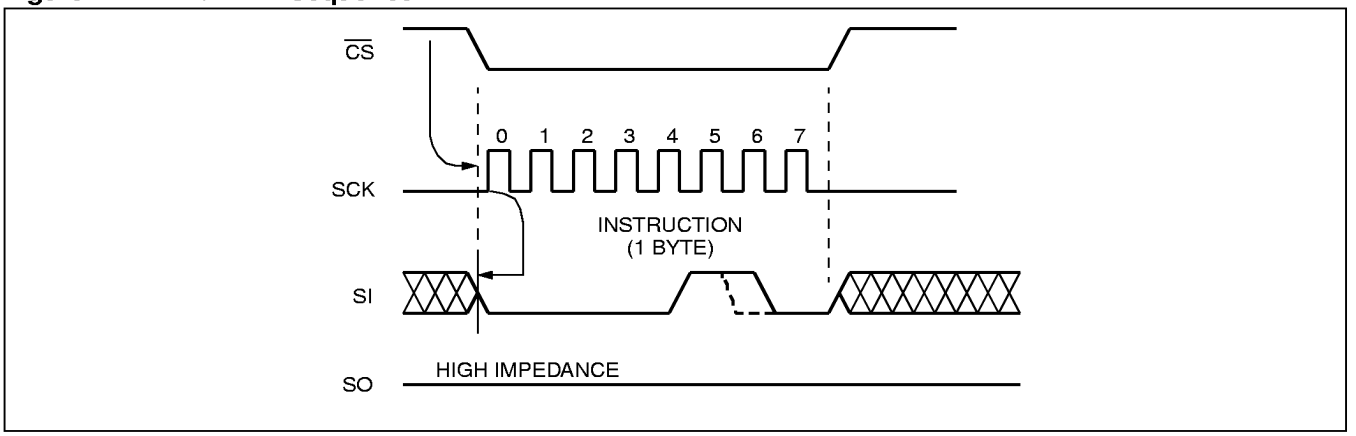


Figure 4. Write Sequence

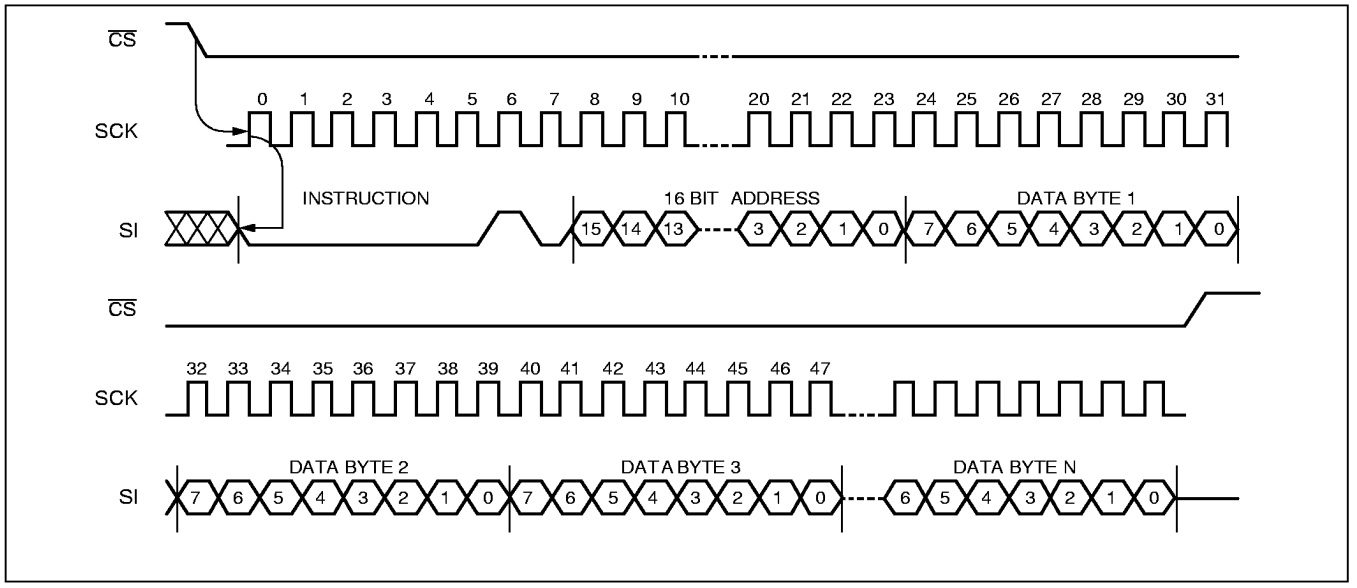


Figure 5. Status Register Write Sequence

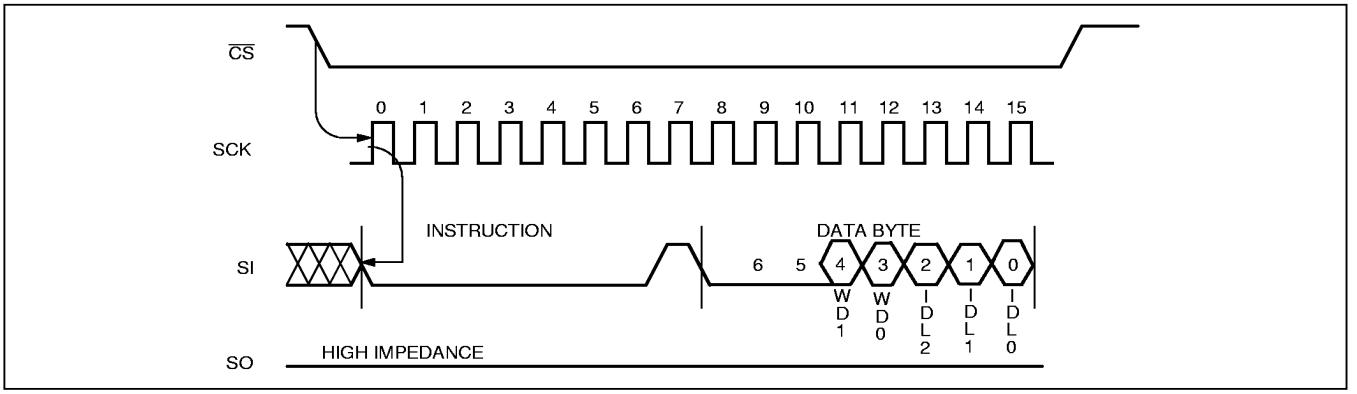


Figure 6. Read Nonvolatile Status (Option 1) (Used to determine end of Watchdog Timer store operation)

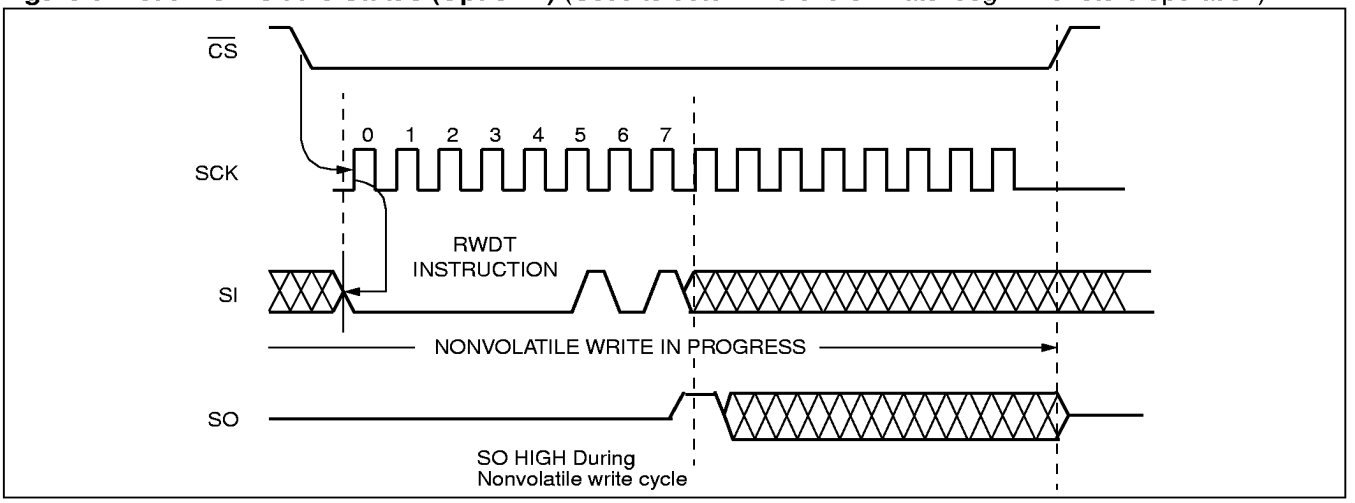
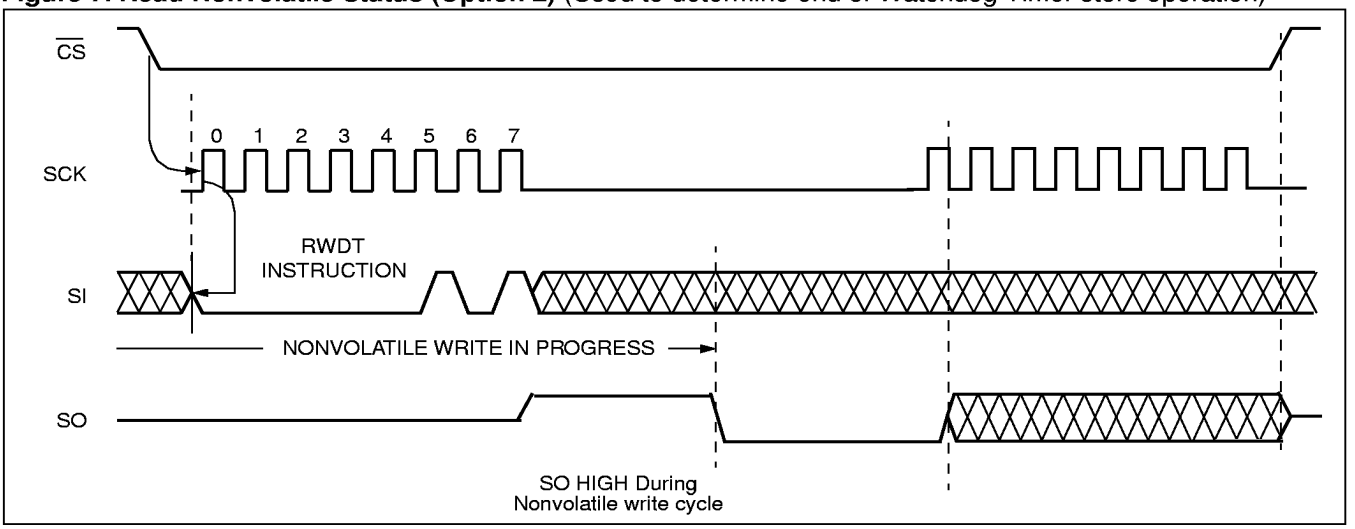


Figure 7. Read Nonvolatile Status (Option 2) (Used to determine end of Watchdog Timer store operation)



Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias .....–65°C to +135°C
Storage Temperature .....–65°C to +150°C
Voltage on any Pin with Respect to V_{SS}.....–1.0V to +7V
D.C. Output Current 5mA
Lead Temperature (Soldering, 10 seconds).....300°C

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C

7036 FRM T07

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Supply Voltage	Limits
X25383/85–1.8	1.8V-3.6V
X25383/85–2.7	2.7V to 5.5V
X25383/85	4.5V-5.5V

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC1}	V_{CC} Write Current (Active)			5	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 5MHz, SO = Open
I_{CC2}	V_{CC} Read Current (Active)			0.4	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 5MHz, SO = Open
I_{SB1}	V_{CC} Standby Current WDT=OFF			1	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5V
I_{SB2}	V_{CC} Standby Current WDT=ON			50	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5V
I_{SB3}	V_{CC} Standby Current WDT=ON			20	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} =3.6V
I_{LI}	Input Leakage Current		0.1	10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		0.1	10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–0.5		V_{CC}x0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC}x0.7		V_{CC}+0.5	V	
V_{OL1}	Output LOW Voltage			0.4	V	V_{CC} > 3.3V, I_{OL} = 2.1mA
V_{OL2}	Output LOW Voltage			0.4	V	2V < V_{CC} ≤ 3.3V, I_{OL} = 1mA
V_{OL3}	Output LOW Voltage			0.4	V	V_{CC} ≤ 2V, I_{OL} = 0.5mA
V_{OH1}	Output HIGH Voltage	V_{CC}–0.8			V	V_{CC} > 3.3V, I_{OH} = –1.0mA
V_{OH2}	Output HIGH Voltage	V_{CC}–0.4			V	2V < V_{CC} ≤ 3.3V, I_{OH} = –0.4mA
V_{OH3}	Output HIGH Voltage	V_{CC}–0.2			V	V_{CC} ≤ 2V, I_{OH} = –0.25mA
V_{OLRS}	Reset Output LOW Voltage			0.4	V	I_{OL} = 1mA

POWER-UP TIMING

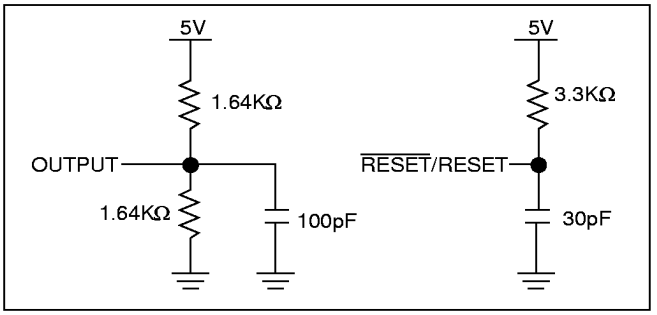
Symbol	Parameter	Min.	Max.	Units
t_{PUR}(2)	Power-up to Read Operation		1	ms
t_{PUW}(2)	Power-up to Write Operation		5	ms

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
C_{OUT}(2)	Output Capacitance (SO, $\overline{RESET}$, RESET)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$)	6	pF	V_{IN} = 0V

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT AT 5V V_{CC}



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x0.5

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

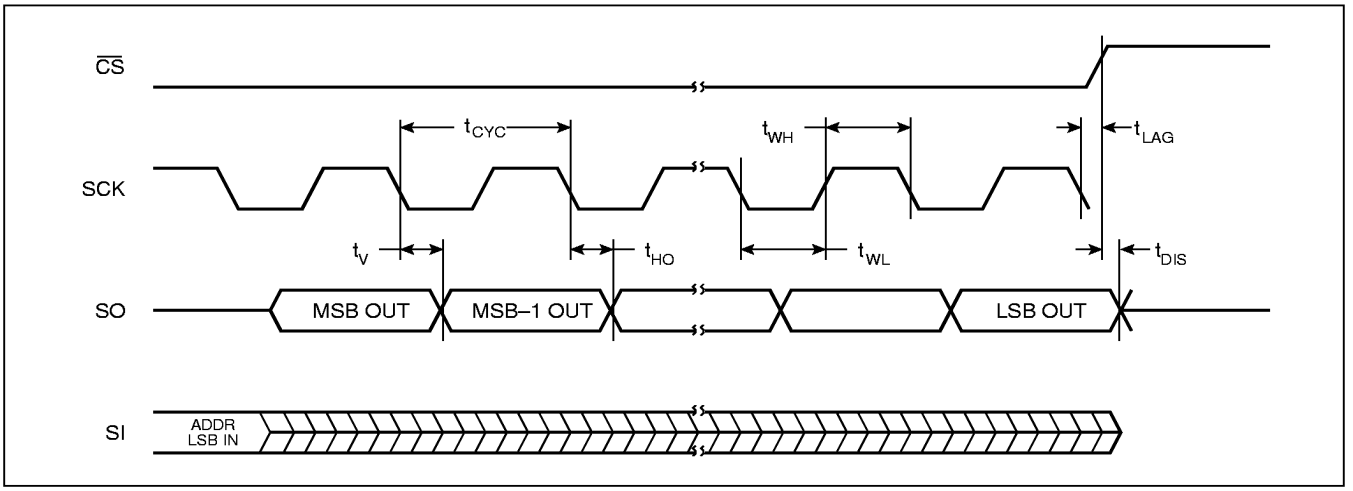
		1.8V–3.6V		2.7V–5.5V		4.5V–5.5V		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
f_{SCK}	Clock Frequency	0	2.0	0	3.3	0	5	MHz
t_{CYC}	Cycle Time	500		300		200		ns
t_{LEAD}	$\overline{CS}$ Lead Time	250		150		100		ns
t_{LAG}	$\overline{CS}$ Lag Time	250		150		100		ns
t_{WH}	Clock HIGH Time	230		130		80		ns
t_{WL}	Clock LOW Time	230		130		80		ns
t_{SU}	Data Setup Time	20		20		20		ns
t_H	Data Hold Time	20		20		20		ns
t_{RI}(3)	Input Rise Time		2		2		2	µs
t_{FI}(3)	Input Fall Time		2		2		2	µs
t_{CS}	$\overline{CS}$ Deselect Time	100		100		100		ns
t_{WC}(4)	Write Cycle Time		10		10		10	ms

Data Output Timing

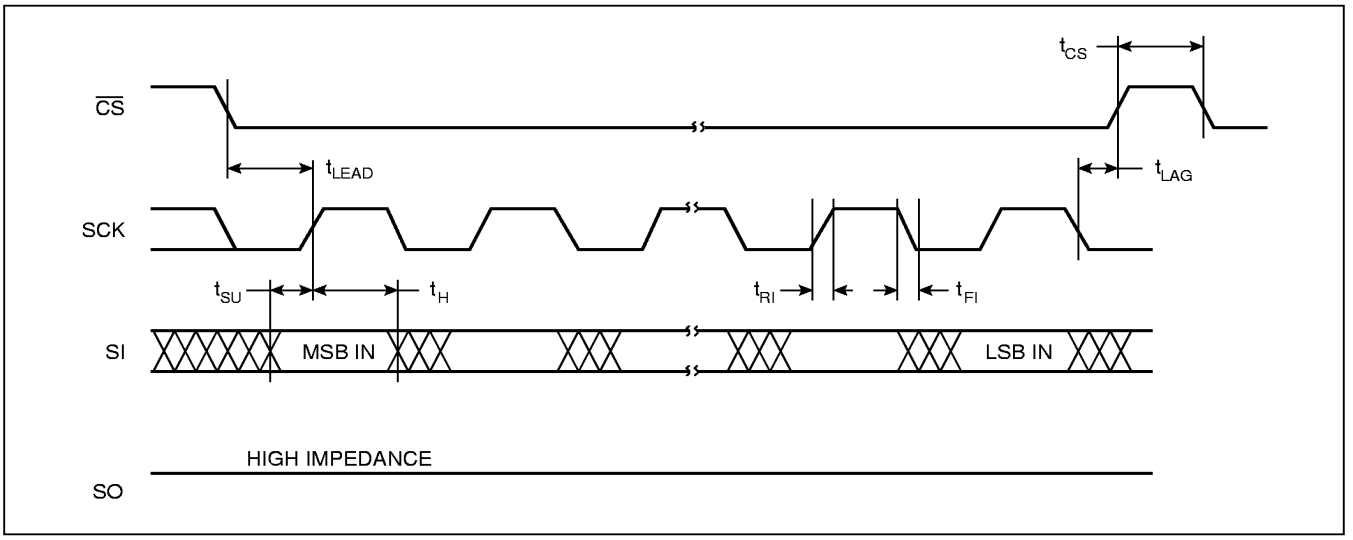
		1.8V–3.6V		2.7V–5.5V		4.5V–5.5V		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
f_{SCK}	Clock Frequency	0	2.0	0	3.3	0	5	MHz
t_{DIS}	Output Disable Time		250		150		100	ns
t_V	Output Valid from Clock Low		230		130		80	ns
t_{HO}	Output Hold Time	0		0		0		ns
t_{RO}(3)	Output Rise Time		50		50		50	ns
t_{FO}(3)	Output Fall Time		50		50		50	ns

Notes: (3) This parameter is periodically sampled and not 100% tested.
(4) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

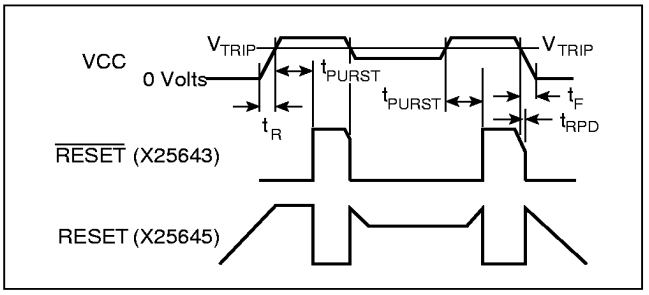
Serial Output Timing



Serial Input Timing



Power-Up and Power-Down Timing

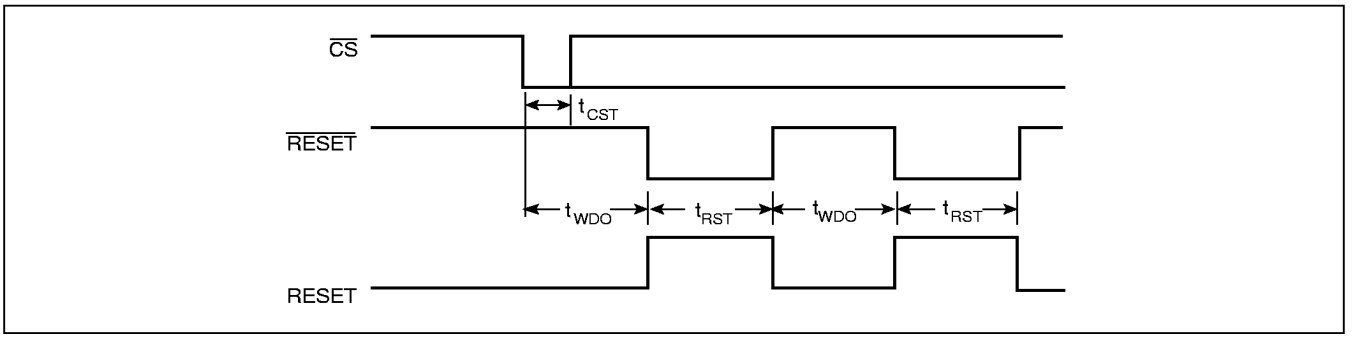


RESET Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{TRIP}	Reset Trip Point Voltage, 5V Device Reset Trip Point Voltage, 2.7V Device Reset Trip Point Voltage, 1.8V Device	4.25 2.55 1.7		4.5 2.7 1.8	V V V
t_{PURST}	Power-up Reset Timeout	100	200	300	ms
t_{RPD}(5)	V_{CC} Detect to Reset/Output			500	ns
t_F(5)	V_{CC} Fall Time	0.1			ns
t_R(5)	V_{CC} Rise Time	0.1			ns
V_{RVALID}	Reset Valid V_{CC}	1			V

Notes: (5) This parameter is periodically sampled and not 100% tested.

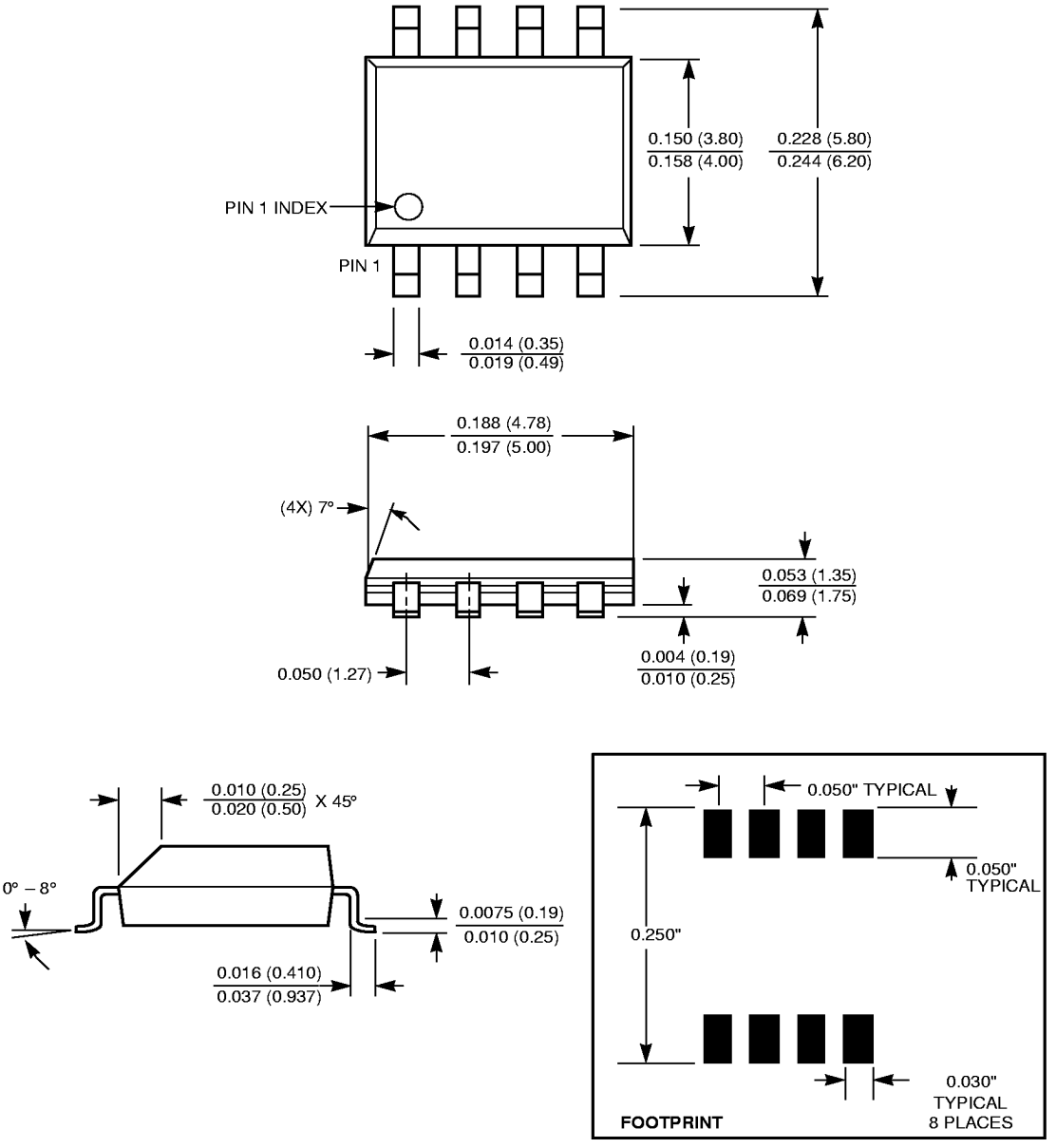
CS vs. RESET/RESET Timing



RESET/RESET Output Timing

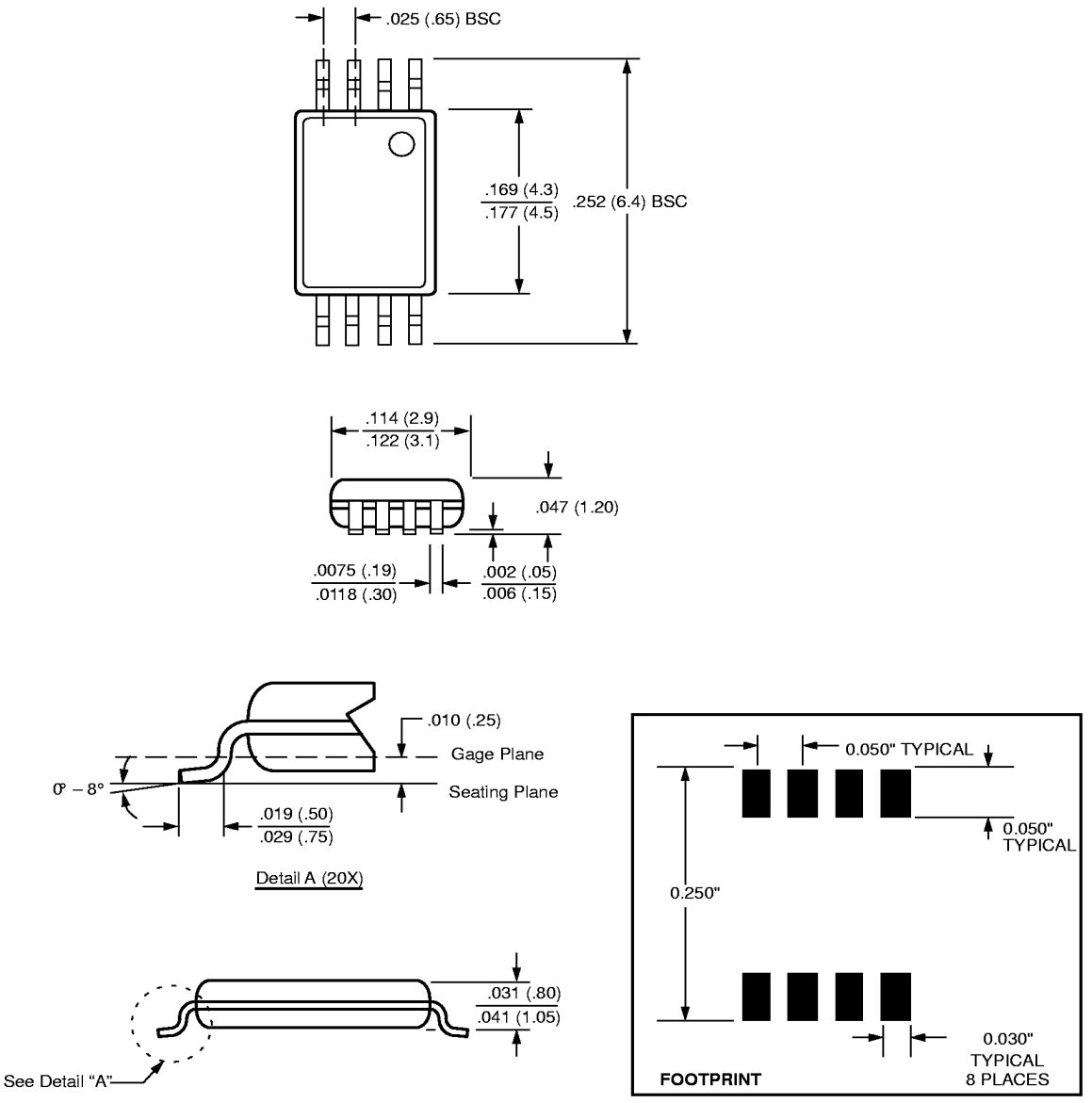
Symbol	Parameter	Min.	Typ.	Max.	Units
t_{WDO}	Watchdog Timeout Period, WD1 = 1, WD0 = 0 WD1 = 0, WD0 = 1 WD1 = 0, WD0 = 0	 100 450 1	 200 600 1.4	 300 800 2	 ms ms sec
t_{CST}	CS Pulse Width to Reset the Watchdog	400			ns
t_{RST}	Reset Timeout	100	200	300	ms

8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



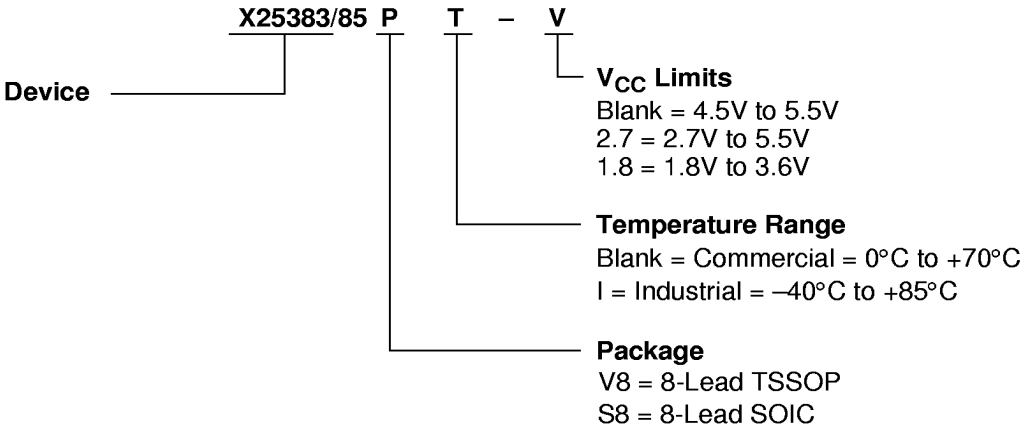
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

8-LEAD PLASTIC, TSSOP, PACKAGE TYPE V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

ORDERING INFORMATION



Part Mark Convention

8-Lead TSSOP

EYWW
5383/85XX

AG = 1.8 to 3.6V, 0 to +70°C
AH = 1.8 to 3.6V, -40 to +85°C
F = 2.7 to 5.5V, 0 to +70°C
G = 2.7 to 5.5V, -40 to +85°C
Blank = 4.5 to 5.5V, 0 to +70°C
I = 4.5 to 5.5V, -40 to +85°C

8-Lead SOIC

X25383/85 X — Blank = 8-Lead SOIC
XX

AG = 1.8 to 3.6V, 0 to +70°C
AH = 1.8 to 3.6V, -40 to +85°C
F = 2.7 to 5.5V, 0 to +70°C
G = 2.7 to 5.5V, -40 to +85°C
Blank = 4.5 to 5.5V, 0 to +70°C
I = 4.5 to 5.5V, -40 to +85°C