QUALITY SEMICONDUCTOR, INC.

High Speed 3.3V 16-Bit Bidirectional Transceivers

QS74FCT163245

FEATURES/BENEFITS

- Pin and function compatible with T.I. Widebus™ and IDT Double-Density™ families
- CMOS power levels: <1µW typical standby
- SSOP (PV) and TSSOP (PA) packages
- Low output skew: 0.5ns $t_{SK(O)}$
- Flow-through pinout for easy layout
- Extended commercial temperature: –40°C to +85°C
- Extended 3.3V supply range 2.7V to 3.6V
- JEDEC compatible LVTTL output levels for 3.3V
- Input hysteresis for noise immunity
- Multiple power and ground pins for low noise
- A and C speed grades: 4.1ns t_{PD} for C
- 5V tolerant inputs for 5V to 3.3V translation

DESCRIPTION

The FCT163245 16-bit transceiver is ideal for bidirectional data buffering between two buses. This device can be used as either two independent 8-bit transceivers or one 16-bit transceiver determined by the Direction and Output Enable controls. Easy board layout is facilitated by the use of flow-through pinouts. All outputs have ground bounce suppression circuitry (see QSI Application Note AN-01). Multiple power and ground pins result in low ground and V_{CC} bounce. This JEDEC LVTTL compliant 3.3V device is useful for 5V to 3.3V buffering applications, since all inputs will support 5V signals.

Figure 1. Functional Block Diagram

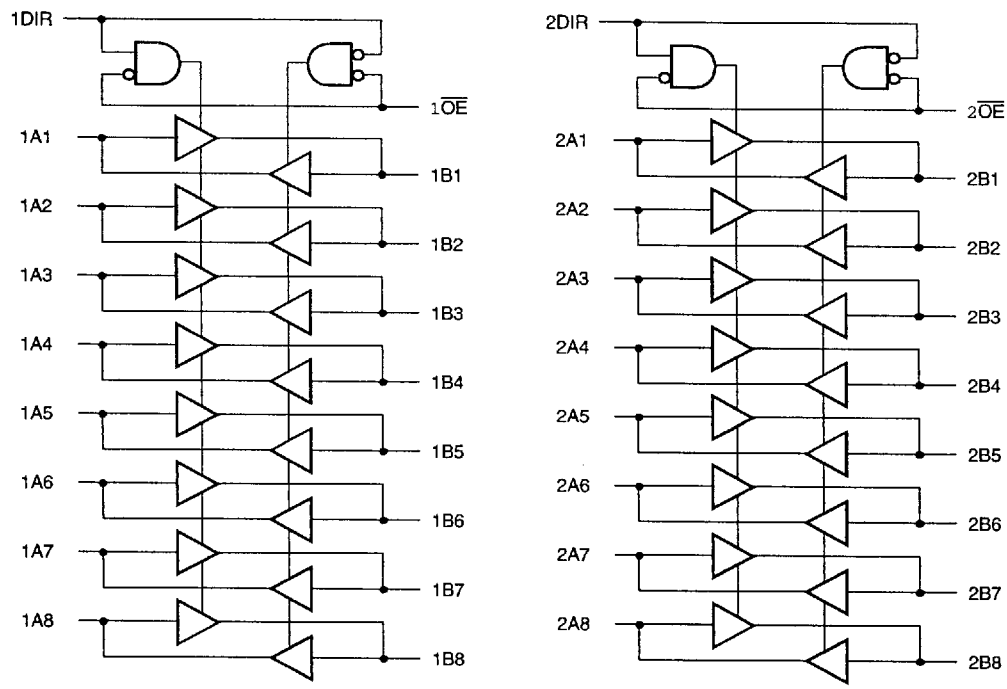


Figure 2. Pin Configuration (All Pins Top View)

SSOP, TSSOP

1DIR	1	48	$1\overline{OE}$
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
V_{CC}	7	42	V_{CC}
1B5	8	41	1A5
1B6	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
GND	15	34	GND
2B3	16	33	2A3
2B4	17	32	2A4
V_{CC}	18	31	V_{CC}
2B5	19	30	2A5
2B6	20	29	2A6
GND	21	28	GND
2B7	22	27	2A7
2B8	23	26	2A8
2DIR	24	25	$2\overline{OE}$

Table 1. Pin Description

Name	Description
xDIR	Transmit/Receive Input
$x\overline{OE}$	Output Enable Inputs
xAx	Bus A
xBx	Bus B

Table 2. Function Table

Inputs		
$x\overline{OE}$	xDIR	Outputs
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Hi-Z

Table 3. Capacitance

$T_A = 25°C$, f = 1MHz, $V_{IN} = 0V$, $V_{OUT} = 0V$

Symbol	Parameter	Typ	Unit
C_{IN}	Input Capacitance	7.0	pF
C_{OUT}	Output Capacitance	8.0	pF

Note: Capacitance is characterized but not production tested.

Table 4. Absolute Maximum Ratings

Supply Voltage to Ground	−0.5V to +4.6V
DC Output Voltage V_{OUT}	−0.5V to V_{CC} +0.5V
DC Input Voltage V_{IN}	−0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	−3.0V
DC Input Diode Current with $V_{IN} < 0$	−20mA
DC Output Diode Current with $V_{OUT} < 0$	−50mA
DC Output Current Max. Sink Current/Pin	120mA
T_{STG} Storage Temperature	−65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

Table 5. Recommended Operating Conditions

Symbol		Min	Max	Unit
V_{CC}	Supply Voltage	2.7	3.6	V
V_{IN}	Input Voltage	−0.5	5.5	V
V_{OUT}	Voltage Applied to Output or I/O	0	V_{CC}	V
$\Delta t/\Delta v$	Input Transition Slew Rate	—	10	ns/V
T_A	Operating Free Air Temperature	−40	+85	°C

Table 6. DC Electrical Characteristics Over Operating Range

Recommended Operating Ranges apply unless otherwise noted.

Symbol	Parameter	Test Conditions[1]		Min	Typ[2]	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs		2.0	—	5.5	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs		–0.5	—	0.8	V
ΔV_T	Input Hysteresis[4]	$V_{TLH} - V_{THL}$ for All Inputs		—	150	—	mV
$\lvert I_{IH} \rvert$ $\lvert I_{IL} \rvert$	Input Current Input HIGH or LOW	V_{CC} = Max., $0 \le V_{IN} < 5.5V$		—	—	1	µA
$\lvert I_{OZ} \rvert$	Off-State Output Current (Hi-Z)	V_{CC} = Max., $0 \le V_{OUT} \le V_{CC}$		—	—	1	µA
I_{OS}	Short Circuit Current[3,4]	V_{CC} = Max., V_{OUT} = GND		–60	–140	–240	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 2.7V $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = –0.1mA I_{OH} = –3.0mA	V_{CC} –0.2 2.4	— —	— —	V
		V_{CC} = 3.0V $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = –8mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	V_{CC} = 2.7V $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 0.1mA I_{OL} = 16mA I_{OL} = 24mA	— — —	— — —	0.2 0.4 0.55	V
		V_{CC} = 3.0V $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 24mA	—	—	0.5	V
V_{IK}	Input Clamp Voltage[4]	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V

Notes:

1. For conditions shown as Max. or Min. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values indicate V_{CC} = 3.3V and T_A = 25°C.
3. Not more than one output should be shorted at one time. Duration of test should not exceed one second.
4. These parameters are guaranteed by design but not production tested.

Table 7. Power Supply Characteristics

Symbol	Parameter	Test Conditions[1]		Typ [2]	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., Freq = 0 V_{IN} = GND or V_{CC}		1	10	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH[3]	V_{CC} = Max., V_{IN} = V_{CC} –0.6V		2.0	30	µA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open One Bit Toggling @ 50% Duty Cycle $x\overline{OE}$ = GND		50	75	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open One Bit Toggling @ 50% Duty Cycle $x\overline{OE}$ = GND, f_i = 10MHz	V_{IN} = V_{CC} –0.6V V_{IN} = GND	0.5[5]	0.8[5]	mA
		V_{CC} = Max., Outputs Open Sixteen Bits Toggling @ 50% Duty Cycle $x\overline{OE}$ = GND, f_i = 2.5MHz	V_{IN} = V_{CC} –0.6V V_{IN} = GND	2.0[5]	3.3[5]	mA

Notes:

1. For conditions shown as Min. or Max., use the appropriate values specified under Recommended Operating Conditions for applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input. All Other Inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed by design but not tested.
6. I_C = Iquiescent + Iinputs = Idynamic.
   $I_C = I_{CCQ} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$.
   I_{CCQ} = Quiescent Current (I_{CCL}, I_{CCH}, and I_{CCZ}).
   ΔI_{CC} = Power Supply Current for a TTL-High Input (V_{IN} = V_{CC} –0.6V).
   D_H = Duty Cycle for TTL High Inputs.
   N_T = Number of TTL High Inputs.
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL).
   f_{CP} = Clock Frequency for Register devices (Zero for Non-Register Devices).
   N_{CP} = Number of Clock Inputs at f_{CP}.
   f_i = Input Frequency.
   N_i = Number of Inputs at f_i.

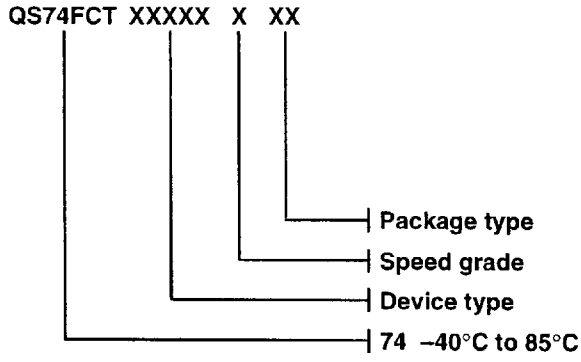
Table 8. Switching Characteristics Over Operating Range

Recommended Operating Ranges apply unless otherwise specified.
C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

		FCT163245A		FCT163245C		
Symbol	**Description**[1,2]	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PHL} t_{PLH}	Propagation Delay A to B, B to A	1.5	4.6	1.5	4.1	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to A or B	1.5	6.2	1.5	5.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] x$\overline{OE}$ to A or B	1.5	5.0	1.5	4.8	ns
t_{PZH} t_{PZL}	Output Enable Time[3] xDIR to A or B	1.5	6.2	1.5	5.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] xDIR to A or B	1.5	5.0	1.5	4.8	ns
$t_{SK(O)}$	Output Skew[4]	—	0.5	—	0.5	ns

Notes:
1. Minimums guaranteed but not tested. See Test Circuit and Waveforms.
2. Switching Characteristics are with V_{CC} = 3.3V ± 0.3V
   For 2.7V V_{CC} operation, parameters should be degraded by 20%.
3. Guaranteed by design, but not production tested.
4. Skew between any two outputs of the same package switching in the same direction.
   This parameter is guaranteed by design but not tested.

ORDERING INFORMATION



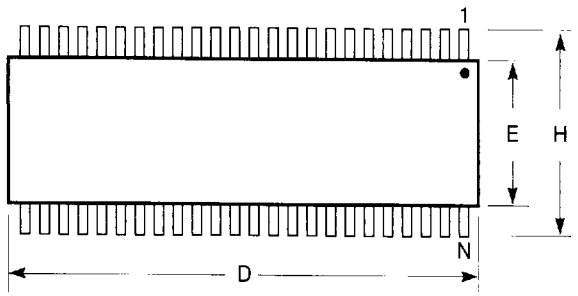
Device Type:
163245

Speed Grades:
A
C

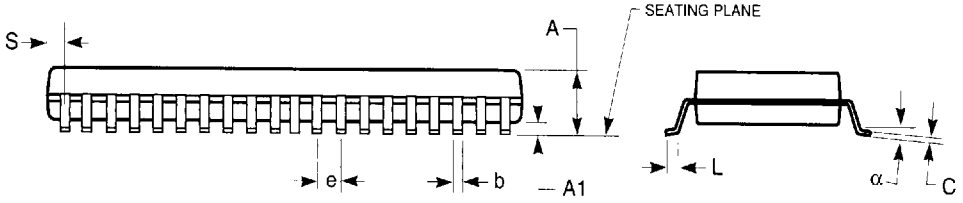
Package Type:
PV – SSOP, 300 mil
PA – TSSOP, 240 mil

300-MIL SSOP - Package Code PV

Shrink Small Outline Package
Plastic Small Outline Gull-Wing



Notes:
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 in. per side.
5. Lead coplanarity is 0.004 in. maximum.



JEDEC#	MO-118AA			MO-118AB		
DWG#	PSS-48B			PSS-56B		
Symbol	Min	Nom	Max	Min	Nom	Max
A	0.095	0.102	0.110	0.095	0.102	0.110
A1	0.008	0.012	0.016	0.008	0.012	0.016
b	0.008	0.010	0.0135	0.008	0.010	0.0135
C	0.005	0.008	0.010	0.005	0.008	0.010
D	0.620	0.625	0.630	0.720	0.725	0.730
E	0.291	0.295	0.299	0.291	0.295	0.299
e	0.025 BSC			0.025 BSC		
H	0.395	0.410	0.420	0.395	0.410	0.420
L	0.020	0.030	0.040	0.020	0.030	0.040
N	48			56		
α	0°	5°	8°	0°	5°	8°
S	0.022	0.025	0.028	0.022	0.025	0.028