MX26C1000

1M-BIT (128K x 8) CMOS MULTIPLE-TIME-PROGRAMMABLE ROM

FEATURES

- 128K x 8 organization
- +5V operating power supply
- +12.5V program/erase voltage
- Electric erase instead of UV light erase
- Fast access time: 70/90/100/120/150 ns
- Totally static operation
- Completely TTL compatible
- Operating current: 30mA
- Standby current: 100μA
- 100 minimum erase/program cycles
- Package type:
  - 32 pin PDIP
  - 32 pin SOP
  - 32 pin PLCC
 - 32 pin TSOP(I)

PATENTED TECHNOLOGY

GENERAL DESCRIPTION

The MX26C1000 is a 12V/5V, 1M-bit MTP ROM™ (Multiple Time Programmable Read Only Memory). It is organized as 128K words by 8 bits per word, operates from a +5 volt supply, has a static standby mode, and features fast address location programming. It is designed to be reprogrammed and erased by an EPROM programmer or on-board. All programming/erasing signals are TTL levels, requiring a single pulse. The MX26C1000 supports an intelligent quick pulse programming algorithm which can result in a programming time of less than 30 seconds.

This MTP ROM™ is packaged in industry standard 32 pin dual-in-line packages, 32 pinPLCC packages or 32 pin TSOP packages and 32 pin SOP packages.

PIN CONFIGURATIONS

PDIP/SOP
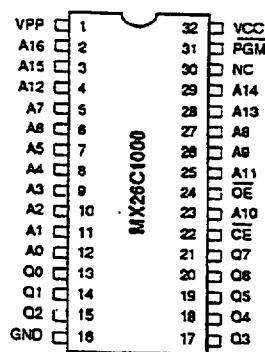
PLCC
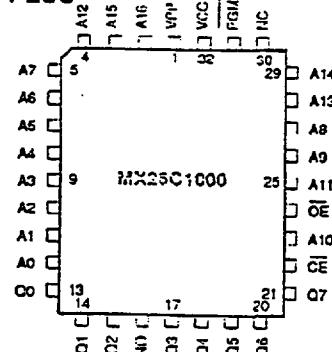
TSOP
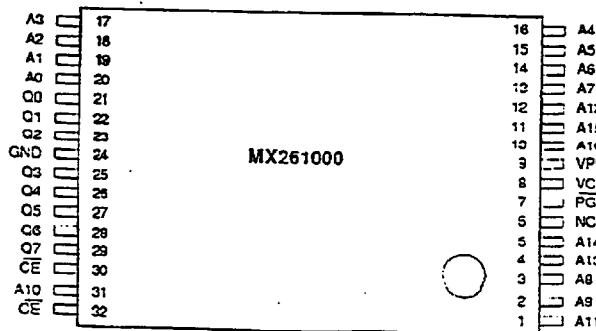
BLOCK DIAGRAM
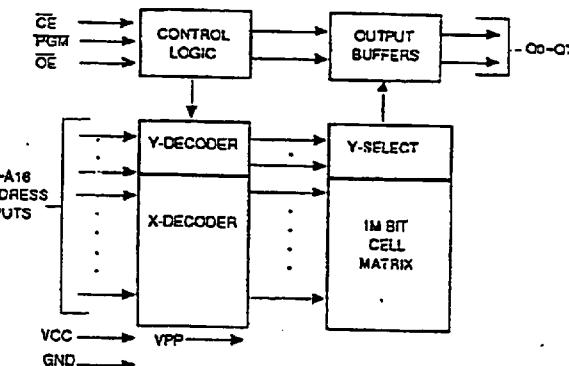
PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A16	Address Input
Q0~Q7	Data Input/Output
CE	Chip Enable Input
OE	Output Enable Input
PGM	Program Enable Input
VPP	Program Supply Voltage
NC	No Internal Connection
VCC	Power Supply Pin (+5V)
GND	Ground Pin

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FUNCTIONAL DESCRIPTION

When the MX26C1000 is delivered, or it is erased, the chip has all 1000K bits in the "ONE", or HIGH state. "ZEROs" are loaded into the MX26C1000 through the procedure of programming.

PROGRAMMING MODE
ON-BOARD PROGRAMMING ALGORITHM

The MX26C1000 is programmed by an EPROM programmer or on-board. The device is set up in the programming mode when the programming voltage VPP = 12.5V is applied, with VCC = 5 V and $\overline{PGM}$ = VIH (Algorithm shown in Figure 1). Programming is achieved by applying a single TTL low level 100μs pulse to the $\overline{PGM}$ input after addresses and data lines are stable. If the data is not verified, additional pulses are applied for a maximum of 20 pulses. After the data is verified, one 100us pulse is applied to overprogram the byte so that program margin is assured. This process is repeated while sequencing through each address of the device. When programming is completed, the data at all the address is verified at VCC = VPP = 5V ± 10%.

The VCC supply of the MXIC On-Board Programming Algorithm is designed to be 5V ± 10% particularly to facilate the programming operation under the on-board application environment. But it can also be implemented in an industrial-standard EPROM programmer.

COMPATIBILITY WITH MX27C1000 FAST PROGRAMMING ALGORITHM

Besides the On-Board Programming Algorithm, the Fast Programming Algorithm of MX27C1000 also applies to MX26C1000. MXIC Fast Algorithm is the conventional EPROM programming algorithm and is available in industrial-standard EPROM programmers. A user of industrial-standard EPROM programmer can choose either of the algorithms base on his preference.

The device is set up in the fast programming mode when the programming voltage VPP = 12.75V is applied, with VCC = 6.25V and $\overline{PGM}$ = VIL(or $\overline{OE}$ = VIH)(Algorithm is shown in Figure 2). The programming is achieved by applying a single TTL low level 100μs pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the device. When the programming mode is completed, the data in all address is verified at VCC = VPP = 5V ± 10%.

ERASE MODE

The MX26C1000 is erased by an EPROM programmer or in-system. The device is set up in erase mode when the A9 = 12.5V and VPP = 12.5V are applied, with VCC = 5V and PGM = VIL.(Algorithm shown in Figure 3). Erase time is around 1sec. If the erase is not verified, an additional erase processes will be repeated for a maximum of 60 times.

PROGRAM INHIBIT MODE

Programming of multiple MX26C1000s in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for CE and OE, all like inputs of the parallel MX26C1000 may be common. A TTL low-level program pulse applied to an MX26C1000 $\overline{CE}$ input with VPP = 12.5 ± 0.5 V and $\overline{PGM}$ LOW will program that MX26C1000. A high-level $\overline{CE}$ input inhibits the other MX26C1000 from being programmed.

PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determine that they were correctly programmed. Verification should be performed with $\overline{OE}$ and $\overline{CE}$, at VIL, PGM at VIH, and VPP at its programming voltage.

ERASE VERIFY MODE

Verification should be performed on the erased chip to determine that the whole chip(all bits) was correctly erased. Verification should be performed with OE and $\overline{CE}$ at VIL, PGM at VIH, and VCC = 5V, VPP = 12.5V

AUTO IDENTIFY MODE

The auto identify mode allows the reading out of a binary code from an MTP that will identify its manufacturer and device type. This mode is intended for use by the programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the MX26C1000.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A9 of the device. Two

identifier bytes may then be sequenced from the device outputs by toggling address line A0 from VIL to VIH. All other address lines must be held at VIL during auto identify mode.

Byte 0 (A0 = VIL) represents the manufacturer code, and byte 1 (A0 = VIH), the device identifier code. For the MX26C1000, these two identifier bytes are given in the Mode Select Table. All identifiers for the manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

READ MODE

The MX26C1000 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable (CE) is the power control and should be used for device selection. Output Enable (OE) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from CE to output (tCE). Data is available at the outputs tOE after the falling edge of OE, assuming that CE has been LOW and addresses have been stable for at least tACC - tOE.

STANDBY MODE

The MX26C1000 has a CMOS standby mode which reduces the maximum VCC current to 100 μA. It is placed in CMOS standby when CE is at VCC ± 0.3 V. The MX26C1000 also has a TTL-standby mode which reduces the maximum VCC current to 1.5 mA. It is placed in TTL-standby when CE is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the OE input.

TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that CE be decoded and used as the primary device-selecting function, while OE be made a common connection to all devices in the array and connected to the READ line from the system control bus.

This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between VCC and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 μF bulk electrolytic capacitor should be used between VCC and GND for each of the eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

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MODE SELECT TABLE

MODE	$\overline{CE}$	$\overline{CE}$	$\overline{PGM}$	A0	A9	VPP	OUTPUTS
						PINS	
Read	VIL	VIL	X	X	X	VCC	DOUT
Output Disable	VIL	VIH	X	X	X	VCC	High Z
Standby (TTL)	VIH	X	X	X	X	VCC	High Z
Standby (CMOS)	VCC	X	X	X	X	VCC	High Z
Program	VIL	VIH	VIL	X	X	VPP	DIN
Program Verify	VIL	VIL	VIH	X	X	VPP	DOUT
Erase	VIL	VIH	VIL	X	VH	VPP	HIGH Z
Erase Verify	VIL	VIL	VIH	X	X	VPP	DOUT
Program Inhibit	VIH	X	X	X	X	VPP	High Z
Manufacturer Code	VIL	VIL	X	VIL	VH	VCC	C2H
Device Code(26C1000)	VIL	VIL	X	VIH	VH	VCC	D2H

NOTES: 1. VH = 12.0 V ± 0.5 V
2. X = Either VIH or VIL(For auto select)
3. A1 - A8 = A10 - A16 = VIL(For auto select)
4. See DC Programming Characteristics for VPP voltage during programming.

FIGURE 1. ON-BOARD PROGRAMMING FLOW CHART

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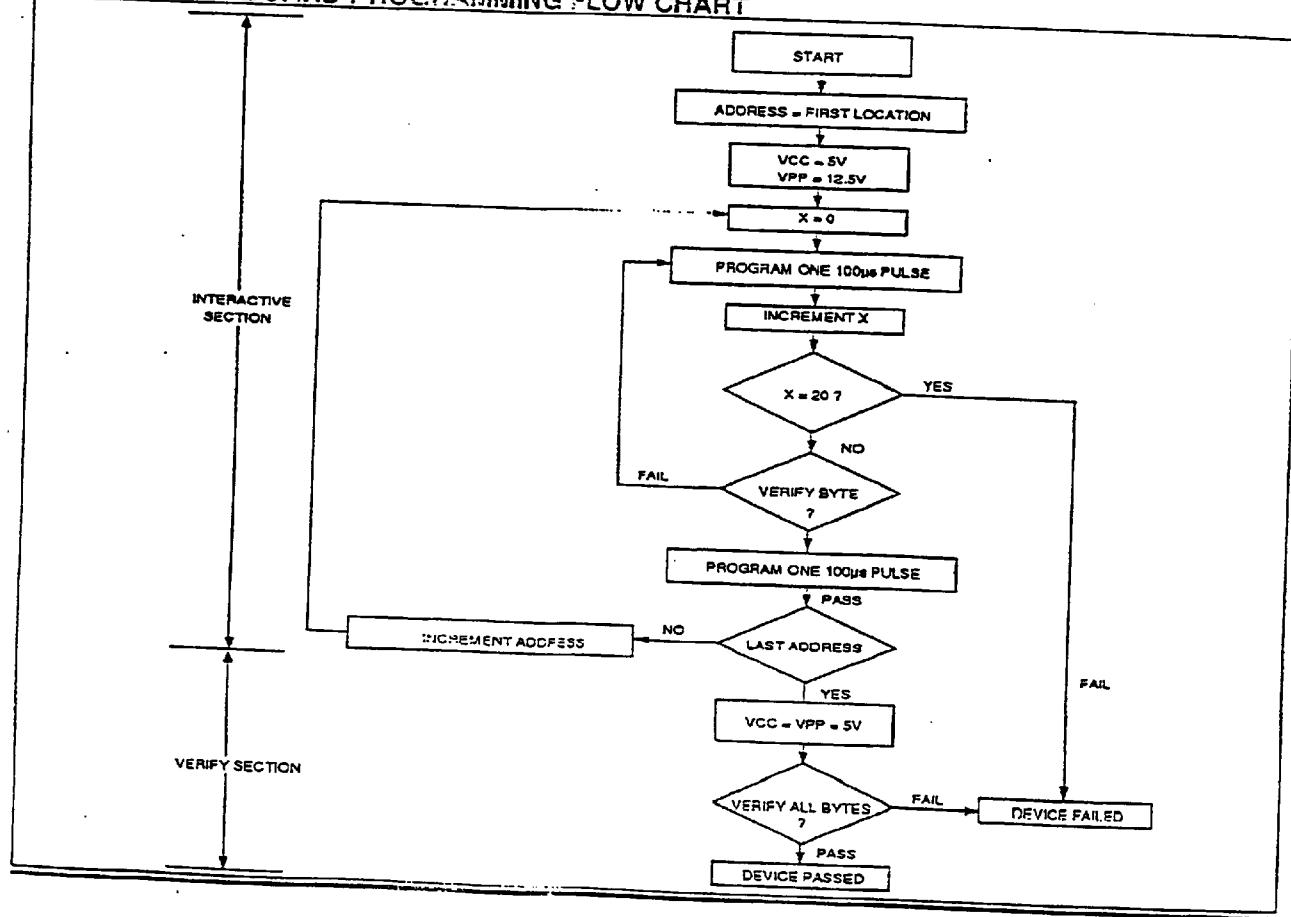
FIGURE 2. COMPATIBILITY WITH MX27C1000 FAST PROGRAMMING FLOW CHART
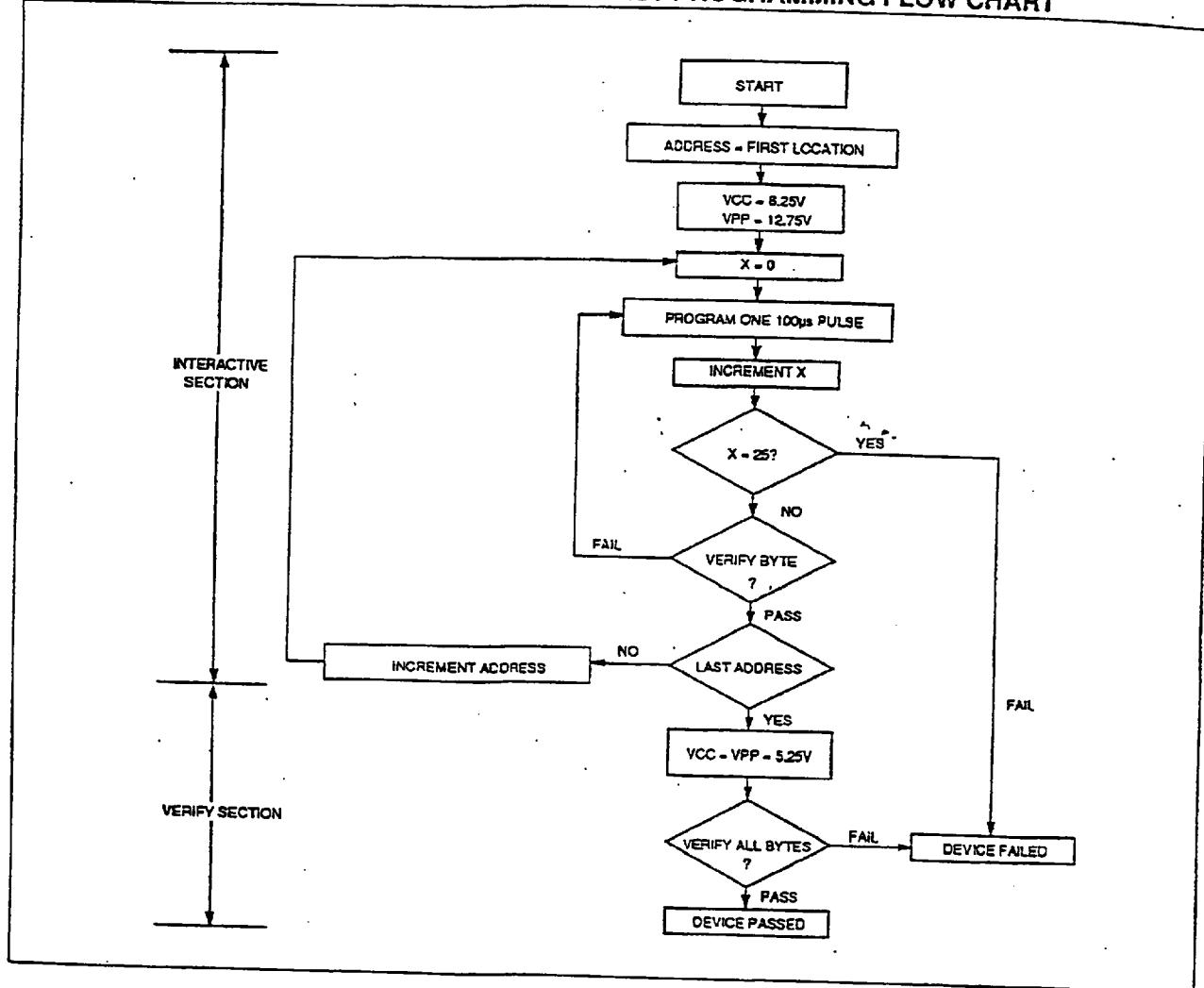
FIGURE 3. ERASING MODE FLOW CHART

```
                    START
                      |
                    X = 0
                      |
              PROGRAM ALL "0"
                      |
               A9 = 12.5V
               VCC = 5V
               VPP = 12.5V   <-----------------+
                      |                         |
               CHIP ERASE (1s)                  |
                      |                         |
               A9 = VIL or VIH                  |
               VCC = 5V                         |
               VPP = 12.5V                      |
                      |                         |
              All Bits Verify              NO   |
                      |                         |
            < ERASE VERIFY ? >--FAIL-->INCREMENT X -->< X = 60 ? >
                      |                                     |
                    PASS                                  YES
                      |                                     |
              DEVICE PASSED                         DEVICE FAILED
```
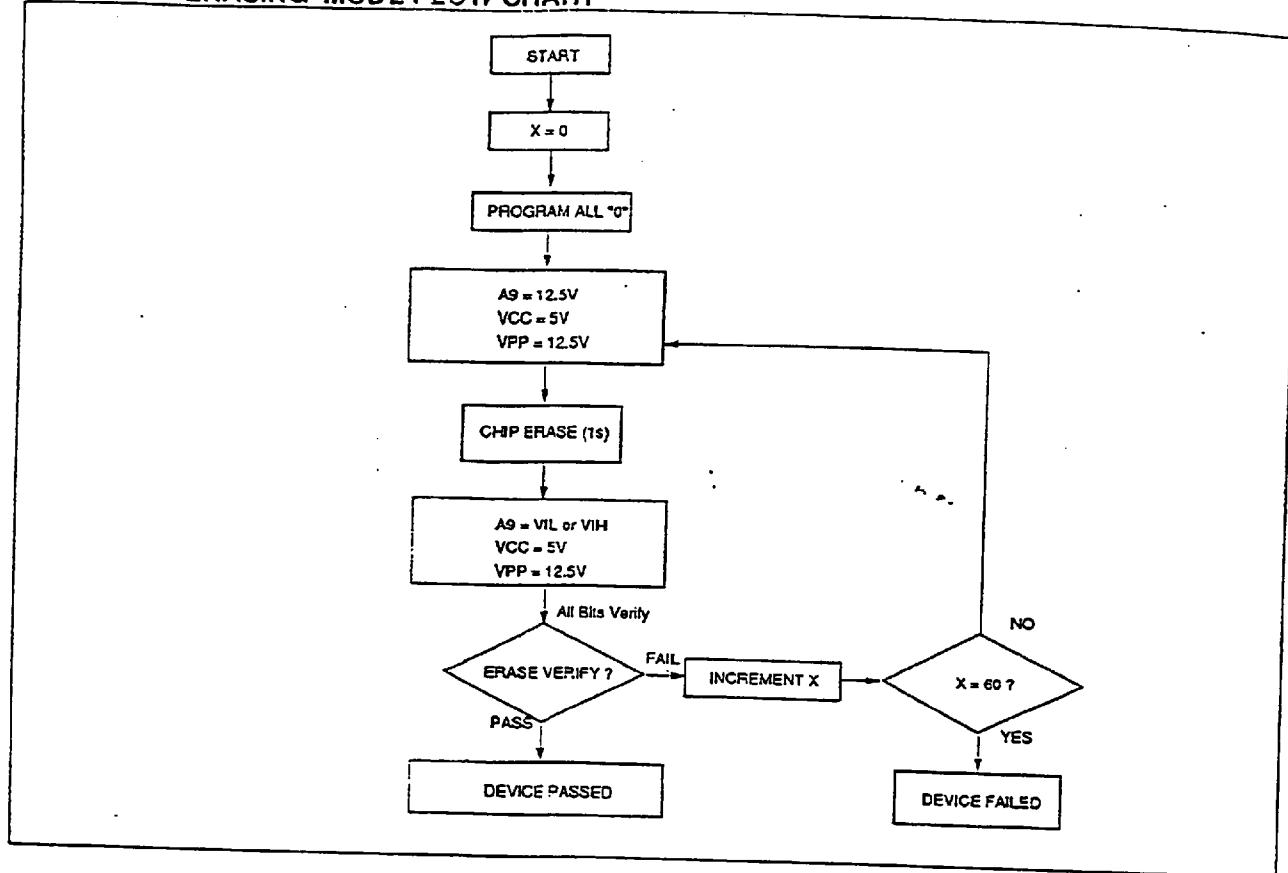
SWITCHING TEST CIRCUITS

```
DEVICE
UNDER          ┤◄┤         1.8KΩ
TEST                      ──/\/\──○ +5V

        ─┴─ CL    ┌─┐ 6.2KΩ      ▽
         ─         │             ▽      DIODES = IN3064
                   └─┘           ▽      OR EQUIVALENT
         ▽         ▽             ▽
```
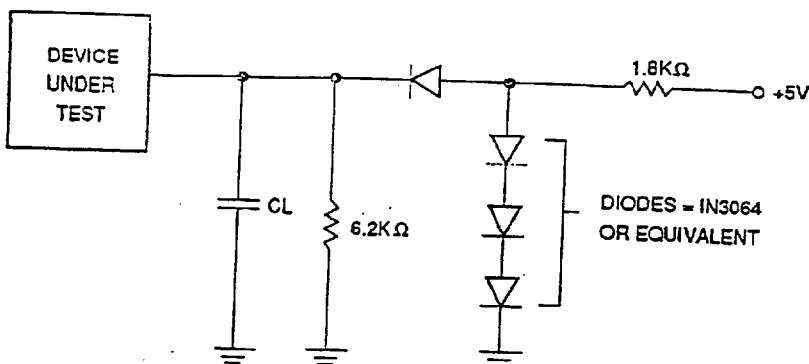
CL = 100 pF including jig capacitance(30pF for 70 ns parts)

SWITCHING TEST WAVEFORMS

```
2.4V ───\      /─── 2.0V                    2.0V \      /───
         \    /                                   \    /
          \  /          TEST POINTS                \  /
           \/                                       \/
           /\                                       /\
          /  \         2.0V              2.0V      /  \
0.4V ────/    \─── 0.8V                       0.8V /    \────
         INPUT                                    OUTPUT
```
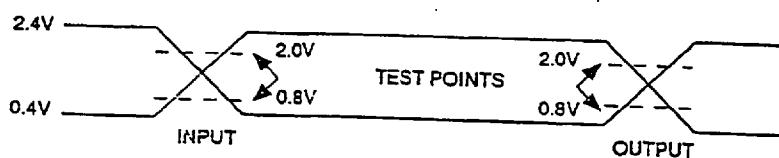
AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.4V for a logic "0".
input pulse rise and fall times are ≤10ns.

```
3.0V ───\      /───
         \    /
1.5V ─ ─ \─ ─/ ─       TEST POINTS
          \  /                               ─ ─\─ ─ ─ 1.5V
           \/                                    \  /
0V  ──────/ \──────                        ──────/  \──────
         INPUT                                   OUTPUT
```
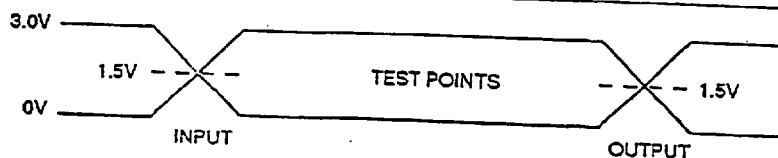
AC TESTING: (1) Inputs are driven at 3.0V for a logic "1" and 0V for a logic "0".
Input pulse rise and fall times are ≤10ns.
(2) For MX27M1000-70

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ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to VCC + 0.5V
VCC to Ground Potential	-0.5V to 7.0V
A9 & Vpp	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
NOTICE:
Specifications contained within the following tables are subject to change.

DC CHARACTERISTICS   TA = 0°C to 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	ICH = -0.4mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	μA	VIN = 0 to 5.5V
ILO	Output Leakage Current	-10	10	μA	VOUT = 0 to 5.5V
ICC3	VCC Power-Down Current		100	μA	$\overline{CE}$ = VCC ± 0.3V
ICC2	VCC Standby Current		1.5	mA	$\overline{CE}$ = VIH
ICC1	VCC Active Current		30	mA	CE = VIL, f=5MHz, Iout = 0mA
IPP	VPP Supply Current Read		100	μA	$\overline{CE}$ = $\overline{OE}$ = VIL, VPP = 5.5V

CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance	8	8	pF	VIN = 0V
COUT	Output Capacitance	8	12	pF	VOUT = 0V
CVPP	VPP Capacitance	18	25	pF	VPP = 0V

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AC CHARACTERISTICS   TA = 0°C to 70°C, VCC = 5V± 10%

| SYMBOL	PARAMETER	26C1000 -70		26C1000 -90		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.		
tACC	Address to Output Delay		70		90	ns	$\overline{CE} = \overline{OE} = VIL$
tCE	Chip Enable to Output Delay		70		90	ns	$\overline{OE} = VIL$
tOE	Output Enable to Output Delay		35		40	ns	$\overline{CE} = VIL$
tDF	OE High to Output Float, or CE High to Output Float	0	20	0	25	ns	
tOH	Output Hold from Address, CE or OE which ever occurred firs	0		0		ns	

SYMBOL	PARAMETER	26C1000 -10		26C1000 -12		26C1000 -15		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
tACC	Address to Output Delay		100		120		150	ns	$\overline{CE} = \overline{OE} = VIL$
tCE	Chip Enable to Output Delay		100		120		150	ns	$\overline{OE} = VIL$
tOE	Output Enable to Output Delay		45		50		65	ns	$\overline{CE} = VIL$
tDF	OE High to Output Float, or CE High to Output Float	0	30	0	35	0	50	ns	
tOH	Output Hold from Address, CE or OE which ever occurred first	0		0		0		ns	

DC PROGRAMMING CHARACTERISTICS   TA = 25°C ± 5°C

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.40mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	µA	VIN = 0 to 5.5V
VH	A9 Auto Select Voltage	11.5	12.5	V	
ICC3	VCC Supply Current (Program/Erase & Verify)		50	mA	
IPP2	VPP Supply Current(Program)/Erase		50	mA	$\overline{CE} = PGM = VIL$, $\overline{OE} = VIH$
VCC2	Fast Programming Supply Voltage	6.00	6.50	V	
VPP2	Fast Programming Voltage	12.5	13.0	V	
IPP A9	A9 Auto Select Current /Erase		1	mA	$\overline{CE} = PGM = VIL$, $\overline{OE} = VIH$

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AC PROGRAMMING CHARACTERISTICS   TA = 25°C ± 5°C

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
tAS	Address Setup Time	2.0		μS	
tOES	$\overline{OE}$ Setup Time	2.0		μS	
tDS	Data Setup Time	2.0		μS	
tAH	Address Hold Time	0		μS	
tDH	Data Hold Time	2.0		μS	
tDFP	$\overline{CE}$ to Output Float Delay	0	130	nS	
tVPS	VPP Setup Time	2.0		μS	
tPW	Program Pulse Width	95	105	μS	
tVCS	VCC Setup Time	2.0		μS	
tDV	Data Valid from $\overline{CE}$		250	nS	
tCES	CE Setup Time	2.0		μS	
tOE	Data valid from $\overline{OE}$		150	nS	
tER	Erase Recovery Time	0.5		S	
tEW	Erase Pulse Width	1		S	
tEV	Erase Verify Time		200	nS	
tA9S	A9 Setup Time	2.0		μS	

WAVEFORMS
READ CYCLE
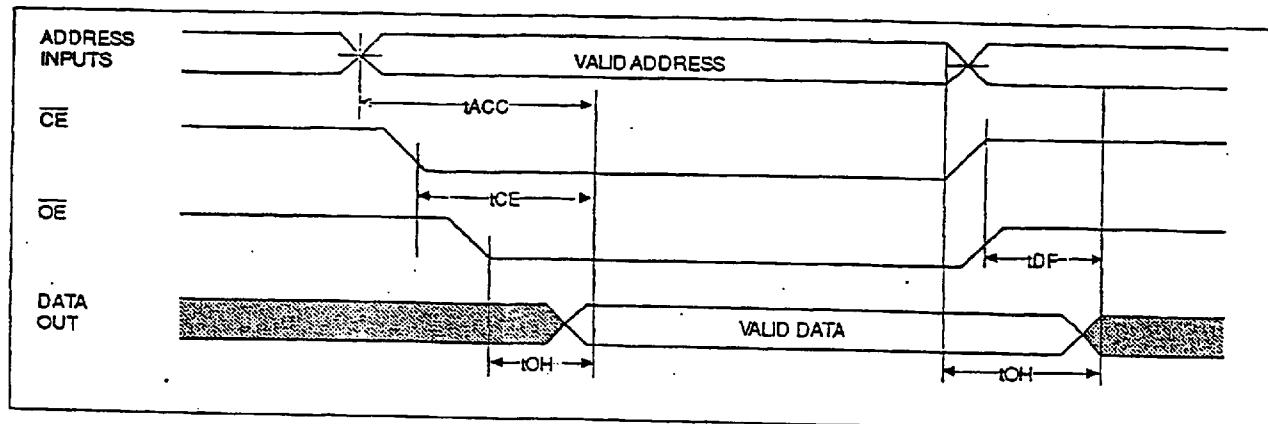
PROGRAMMING WAVEFORMS

ERASE WAVEFORMS

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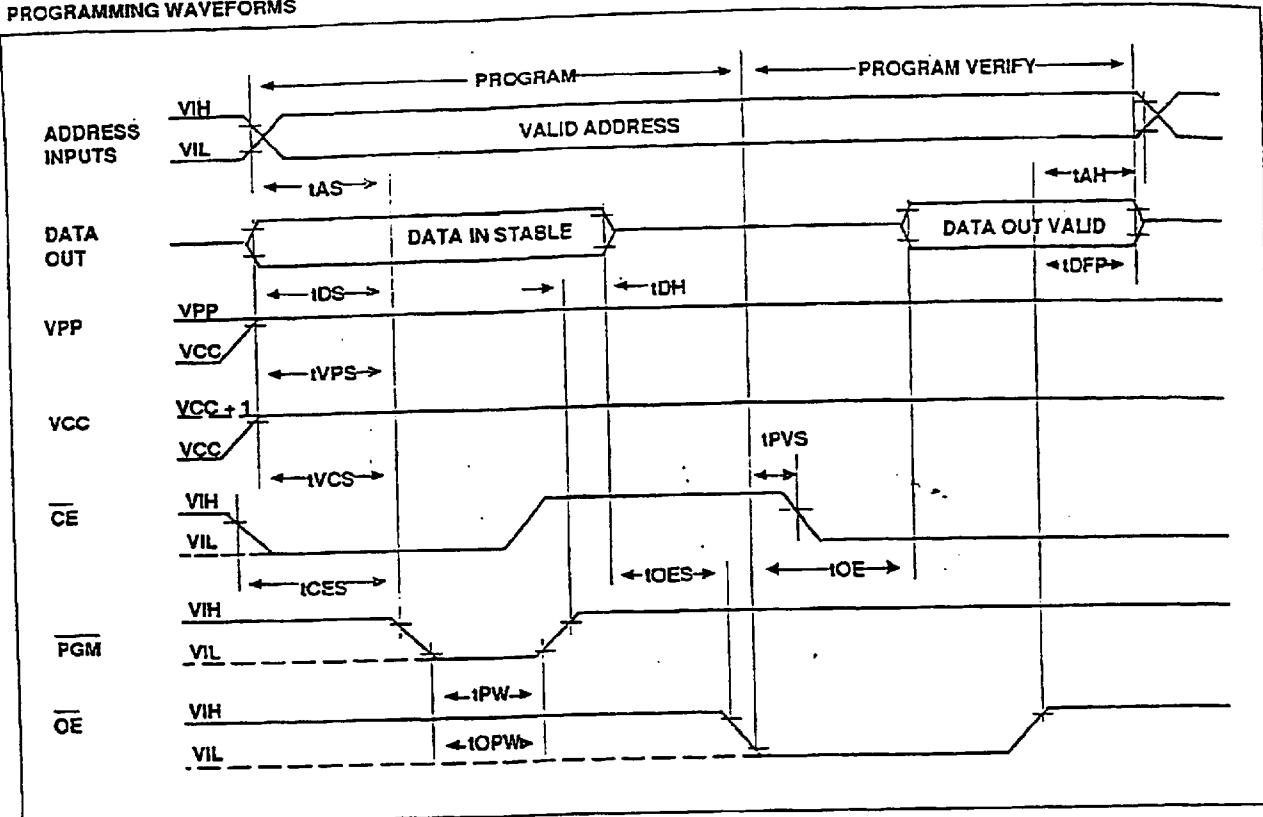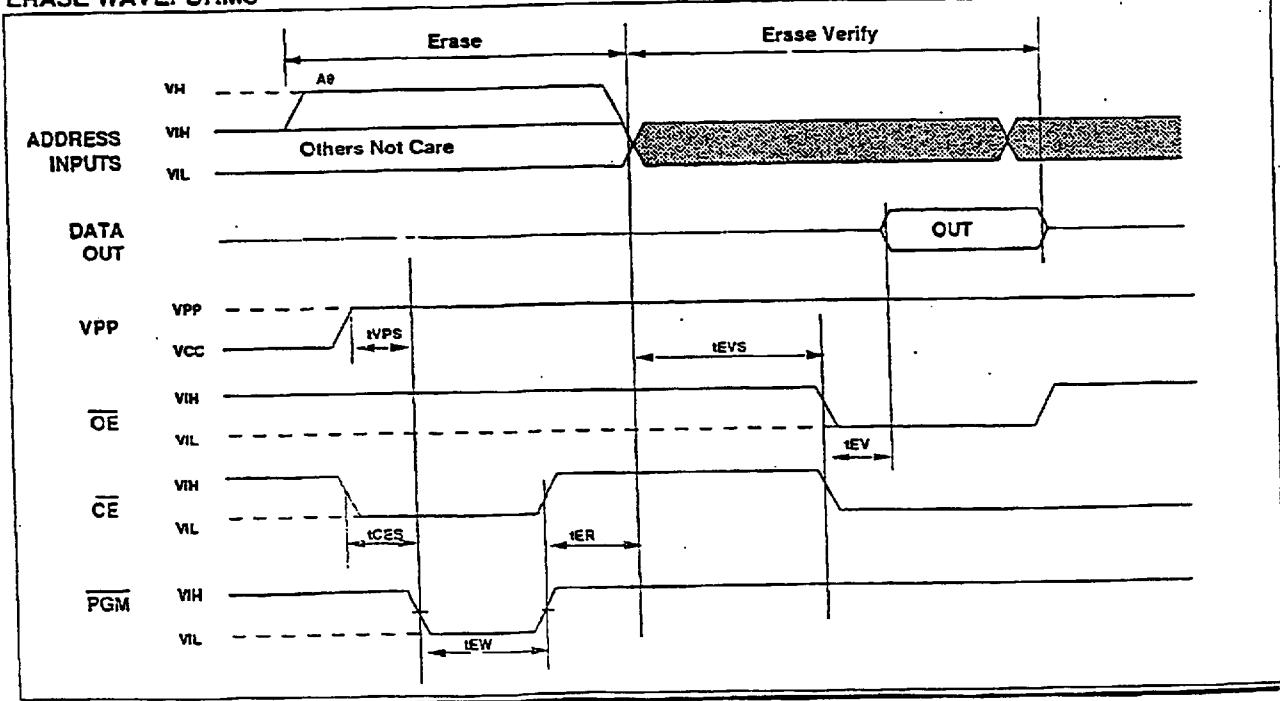
ORDERING INFORMATION
PLASTIC PACKAGE

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(μA)	PACKAGE
MX26C1000PC-70	70	30	100	32 Pin DIP
MX26C1000MC-70	70	30	100	32 Pin SOP
MX26C1000QC-70	70	30	100	32 Pin PLCC
MX26C1000TC-70	70	30	100	32 Pin TSOP
MX26C1000PC-90	90	30	100	32 Pin DIP
MX26C1000MC-90	90	30	100	32 Pin SOP
MX26C1000QC-90	90	30	100	32 Pin PLCC
MX26C1000TC-90	90	30	100	32 Pin TSOP
MX26C1000PC-10	100	30	100	32 Pin DIP
MX26C1000MC-10	100	30	100	32 Pin SOP
MX26C1000QC-10	100	30	100	32 Pin PLCC
MX26C1000TC-10	100	30	100	32 Pin TSOP
MX26C1000PC-12	120	30	100	32 Pin DIP
MX26C1000MC-12	120	30	100	32 Pin SOP
MX26C1000QC-12	120	30	100	32 Pin PLCC
MX26C1000TC-12	120	30	100	32 Pin TSOP
MX26C1000PC-15	150	30	100	32 Pin DIP
MX26C1000MC-15	150	30	100	32 Pin SOP
MX26C1000QC-15	150	30	100	32 Pin PLCC
MX26C1000TC-15	150	30	100	32 Pin TSOP

Revision History

Revision #	Description
1.1	Eraseing mode flow chart: Chip erase(5s)---> (1s). Programming waveforms: $\overline{CE}$ changed.

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PACKAGE INFORMATION

32-PIN PLASTIC DIP(600 mil)

ITEM	MILLIMETERS	INCHES
A	42.13 max.	1.660 max.
B	1.90 [REF]	.075 [REF]
C	2.54 [TP]	.100 [TP]
D	.46 [Typ.]	.018 [Typ.]
E	38.07	1.500
F	1.27 [Typ.]	.050 [Typ.]
G	3.30 ± .25	.130 ± .010
H	.51 [REF]	.020 [REF]
I	3.94 ± .25	.155 ± .010
J	5.33 max.	.210 max.
K	15.22 ± .25	.600 ± .010
L	13.97 ± .25	.550 ± .010
M	.25 [Typ.]	.010 [Typ.]

NOTE: Each lead centerline is located within .25 mm(.01 inch) of its true position [TP] at maximum material condition.
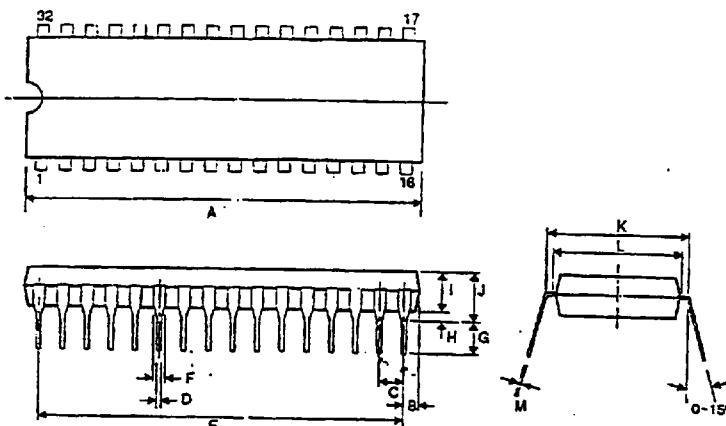
32-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

ITEM	MILLIMETERS	INCHES
A	12.44 ± .13	.490 ± .005
B	11.50 ± .13	.453 ± .005
C	14.04 ± .13	.553 ± .005
D	14.98 ± .13	.590 ± .005
E	1.93	.076
F	3.30 ± .25	.130 ± .010
G	2.03 ± .13	.080 ± .005
H	.51 ± .13	.020 ± .005
I	1.27 [Typ.]	.050 [Typ.]
J	.71 [REF]	.028 [REF]
K	.46 [REF]	.018 [REF]
L	10.40/12.94 (W) (L)	.410/.510 (W) (L)
M	.89 R	.035 R
N	.25 (TYP.)	.010 (TYP.)

NOTE: Each lead centerline is located within .25 mm(.01 inch) of its true position [TP] at maximum material condition.
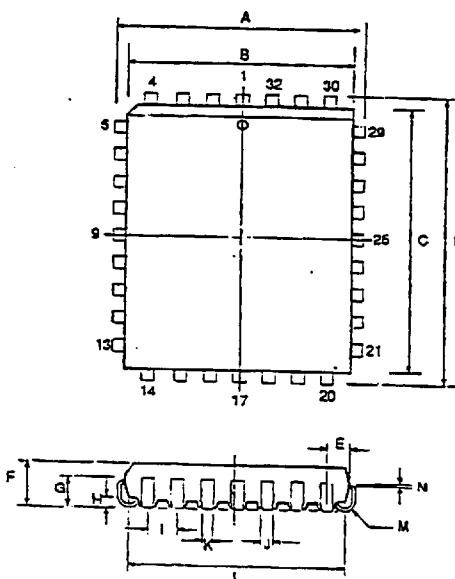
PACKAGE INFORMATION

32-PIN PLASTIC TSOP

ITEM	MILLIMETERS	INCHES
A	20.0 ± .20	.078 ± .008
B	18.40 ± .10	.724 ± .004
C	8.20 max.	.323 max.
D	0.15 (Typ.)	.006 (Typ.)
E	.80 (Typ.)	.031 (Typ.)
F	.20 ± .10	.008 ± .004
G	.30 ± .10	.012 ± .004
H	.50 (Typ.)	.020 (Typ.)
I	.45 max.	.018 max.
J	0 - .20	0 - .008
K	1.00 ± .10	.039 ± .004
L	1.27 max.	.050 max.
M	.50	.020
N	19.00	.748
O	0 - 5	.500

NOTE: Each lead centerline is located within .25 mm(.01 inch) of its true position (TP) at a maximum material condition.
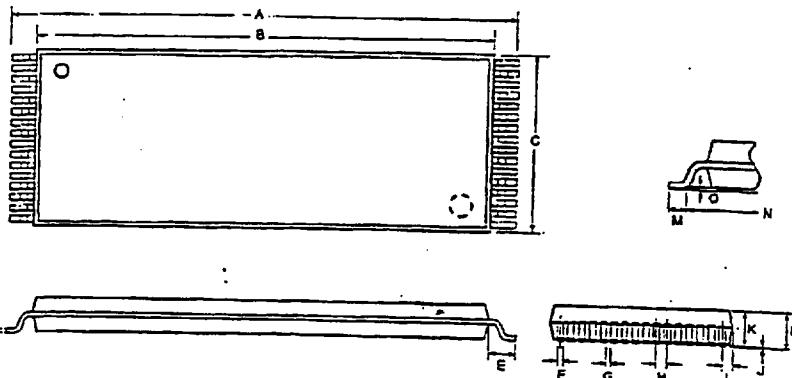
32-PIN PLASTIC SOP (450 mil)

ITEM	MILLIMETERS	INCHES
A	20.95 max.	.825 max.
B	1.00 (REF)	.039 (REF)
C	1.27 (TP)	.050 (TP)
D	.40 (Typ.)	.016 (Typ.)
E	.05 min.	.002 min.
F	3.05 max.	.120 max.
G	2.69 ± .13	.106 ± .005
H	14.12 ± .25	.556 ± .010
I	11.30 ± .13	.445 ± .005
J	1.42	.056
K	.20 (Typ.)	.008 (Typ.)
L	.79	.031

NOTE: Each lead centerline is located within .25 mm(.01 inch) of its true position (TP) at maximum material condition.

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