

Features

- For Intel Pentium CPU based systems
- Operates with clock speeds up to 66MHz
- Separate 5V and 3.3V power supplies
- Low cost and low profile card design using 160 gold plated leads
- Multiple ground pin and decoupling capacitors provide maximum noise protection.
- Conform to Intel COASt 1.4 specification

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Functional Description

The GSM14P256KB-I66 and the GSM14P512KB-I66 are the secondary cache module designed for use with Intel Pentium CPU based system. These modules use GSI's Synchronous Burst SRAMs in plastic surface mount packages mounted on a multilayer epoxy laminate (FR-4) board.

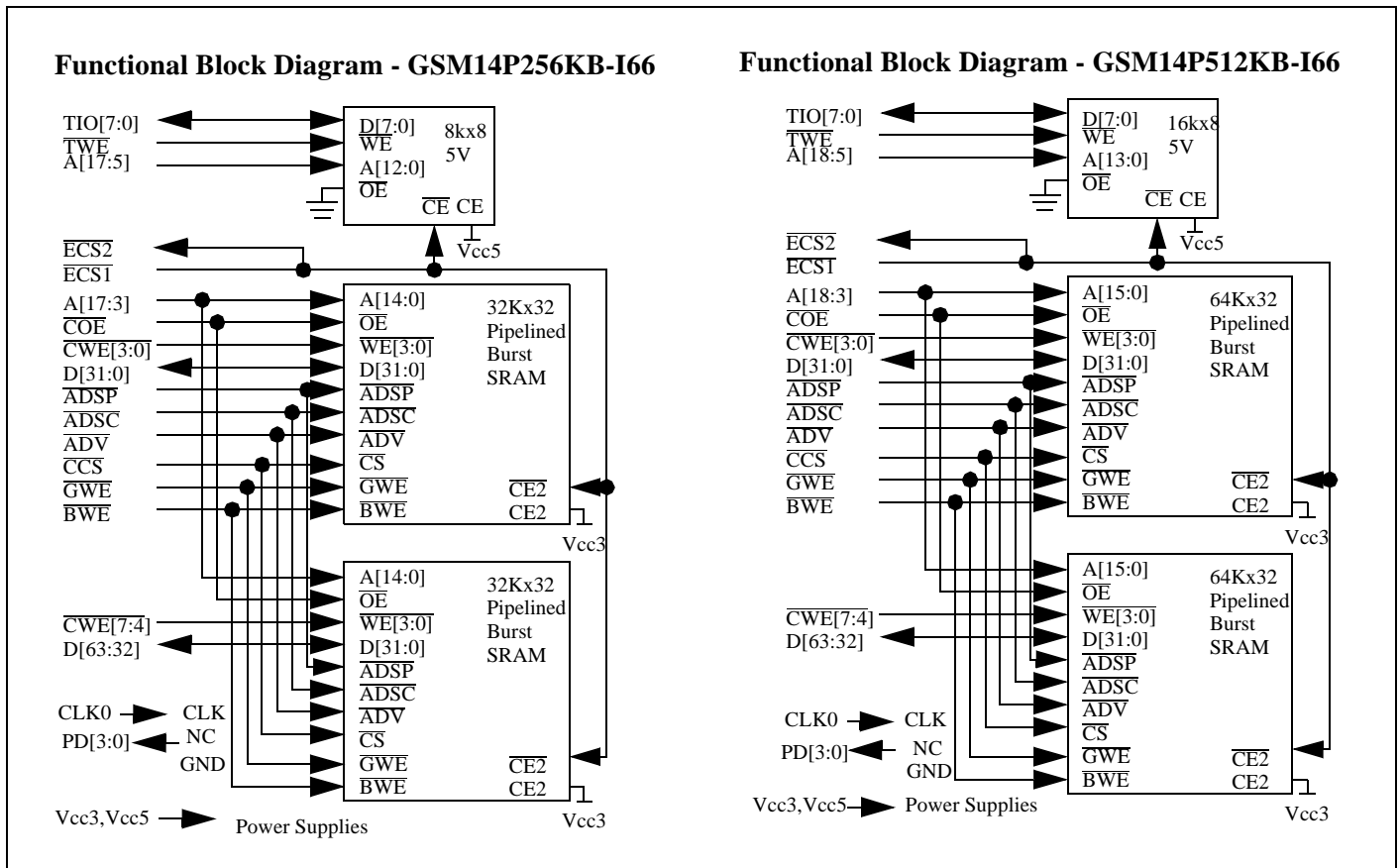
Functional Description (cont'd)

The GSM14P256KB-I66, and 256KB module, use GSI's GS81132Q 32KX32 synchronous burst SRAM and a single 5V 8Kx8 SRAM for the tag. The GSM14P512K-I66, a 512KB module, use GSI's GS82032Q 64KX32 synchronous burst SRAM and a single 5V 32Kx8 SRAM for the tag.

The 3.3V data RAM and the 5V tag RAM provide an exact interface between the module and PC chip set. Four presence detect bits (PD) allow the system to recognize the type of cache configuration present.

The low profile card edge package allows 160 signal leads to be placed on a module, measuring 4.35 inches long, a maximum of 0.310 inches thick and a maximum of 1.14 inches tall. This compact design allows the OEM to make better use of the real estate on the mother-board for added functions or smaller design for cost reduction.

All inputs and outputs and TTL compatible and operate from two separate 5V and 3.3V power supplies. The use of multiple ground pins and decoupling capacitors on-board reduces failure due to noise.



GSM14P256KB-I66 GSM14P512KB-I66 256KB / 512KB Modules

COASt 1.4
Specification

Pin Configuration

GND	81	1	GND	43	GND
TIO1	82	2	D54	44	D52
TIO7	83	3	D53	45	D50
TIO5	84	4	D51	46	D48
TIO3	85	5	D49	47	GND
NC	86	6	GND	48	D46
VCC5	87	7	D47	49	D44
NC	88	8	D45	50	D42
ADV	89	9	D43	51	VCC3
GND	90	10	D37	52	D40
COE	91	11	GND	53	D38
CWE5	92	12	D35	54	D36
CWE7	93	13	D33	55	GND
CWE1	94	14	D31	56	D34
VCC5	95	15	VCC5	57	D32
CWE3	96	16	D29	58	D30
NC	97	17	D27	59	VCC3
NC	98	18	D25	60	D28
GND	99	19	GND	61	D26
NC	100	20	CLK0	62	D24
A4	101	21	GND	63	GND
A6	102	22	D63	64	D22
A8	103	23	VCC5	65	D20
A10	104	24	D61	66	D18
VCC5	105	25	D59	67	VCC3
A17	106	26	D57	68	D16
GND	107	27		69	D14
A9	108	28		70	D12
A14	109	29		71	GND
A15	110	30		72	D10
NC	111	31		73	D8
PD0	112	32		74	D6
PD2	113	33		75	VCC3
NC	114	34		76	D4
GND	115	35		77	D2
CLK0	116	36		78	D0
GND	117	37		79	GND
D63	118	38		80	
VCC5	119	39			
D61	120	40			
D59	121	41			
D57	122	42			
GND	123	43			
D55	124	44			
D53	125	45			
D51	126	46			
D49	127	47			
GND	128	48			
D47	129	49			
D45	130	50			
D43	131	51			
VCC5	132	52			
D41	133	53			
D39	134	54			
D37	135	55			
GND	136	56			
D35	137	57			
D33	138	58			
D31	139	59			
VCC5	140	60			
D29	141	61			
D27	142	62			
D25	143	63			
GND	144	64			
D23	145	65			
D21	146	66			
D19	147	67			
VCC5	148	68			
D17	149	69			
D15	150	70			
D13	151	71			
GND	152	72			
D11	153	73			
D9	154	74			
D7	155	75			
VCC5	156	76			
D5	157	77			
D3	158	78			
D1	159	79			
GND	160	80			

Pin Description

Pin Name	Type	Description
A[18:3]	I	Cache Address Inputs
$\overline{\text{ADSC}}$	I	Cache Address Status
$\overline{\text{ADSP}}$	I	Processor Address Status
$\overline{\text{ADV}}$	I	Burst Address Advance
$\overline{\text{BWE}}$	I	Byte Write Enable
$\overline{\text{CCS}}$	I	Chip Select
CLK0	I	System Clock
$\overline{\text{COE}}$	I	Cache Output Enable
$\overline{\text{CWE}}[7:0]$	I	Cache Write Enables
D[63:0]	I/O	Cache Data Input/Output
$\overline{\text{ECS}}[1:0]$	I	External Chip Select
GWE	I	Global Write Enable
PD[3:0]	O	Presence Detect Outputs
TIO[7:0]	I/O	Tag Inputs/Outputs
$\overline{\text{TWE}}$	I	Tag Write Enable
Vcc3	-	3.3V Power Supply
Vcc5	-	5V Power Supply
GND	-	Ground
NC	-	No Connect

Notes:

- Pin 26, A18, is a no connect in the GSM14P256K-I66 version

Presence Detect Table

PD3	PD2	PD1	PD0	Device Indicated
NC	NC	NC	NC	No Module Present
NC	GND	NC	NC	GSM14P256K-I66
GND	NC	NC	NC	GSM14P512K-I66

Absolute Maximum Ratings

<i>Parameter</i>	<i>Symbol</i>	<i>Value</i>	<i>Unit</i>
Supply Voltage			
3.3V Vcc Pins	Vcc3	-0.5 to +4.6	V
5.0V Vcc Pins	Vcc5	-0.5 to 6.0	V
Operating Temperature	Ta	0 to +70	°C
Storage Temperature	Ts	-55 to +125	°C

Recommended Operating Conditions

<i>Parameter</i>	<i>Symbol</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>
Supply Voltage					
3.3V Vcc Pins	Vcc3	3.135	3.3	3.6	V
5.0V Vcc Pins	Vcc5	4.75	5.0	5.25	V
Operating Temperature	Ta	0	-	+70	°C
Input High Voltage	Vih	2.0	-	Vcc+0.3	°C
Input Low Voltage	Vil	-0.3	-	0.8	

Capacitance

<i>Parameter</i>	<i>Symbol</i>	<i>Max</i>	<i>Unit</i>
Address Input Capacitance	CIN1	20	pF
Control Signal Input Capacitance	CIN2	10	pF
TAG Input Capacitance	CIN3	10	pF
Output Enable Capacitance	CIN4	15	pF
Data I/O Capacitance	CI/O	10	pF

Note: These parameters are guaranteed by design, but not tested.

DC Electrical Characteristics Over the Operating Range

<i>Parameter</i>	<i>Test Condition</i>	<i>Symbol</i>	<i>Min</i>	<i>Max</i>	<i>Unit</i>
Input Leakage Current (Data & Control)	VIN=0 to Vcc3	ILI	-	± 20	uA
Output Leakage Current (Data & Control)	VOUT=0 to Vcc3, $\overline{CS} \geq V_{IH}$	IOUT	-	± 20	uA
Output High Voltage	IOH=-4.0mA	VOH	2.4	-	V
Output Low Voltage	IOL=8.0mA	VOL	-	0.4	V
Operating Supply Current, 5V Power	Vcc5=Max, IOUT=0mA, f=Max	Icc5	-	180	mA
Operating Supply Current, 3.3V Power	Vcc3=Max, IOUT=0mA, f=Max	Icc3	-	500	mA
AC Standby Supply Current, 3.3V Power	Vcc=Max, $\overline{CS} \geq V_{IH}$, f=max	ISB3	-	80	mA
Full CMOS Standby Current	Vcc=Max, $\overline{CS} \geq V_{cc3}-0.2$, f=0MHz, VIN>Vcc3-0.2 or VIN<0.2	ISB31	-	40	mA

Ordering Information

Part Number	Cache Size	Speed
GSM14P256KB-I66	256KB	66MHz
GSM14P512KB-I66	512KB	66MHz

Package Dimension

