

DM74ALS540A Octal Inverting Buffer and Line Driver with TRI-STATE® Outputs

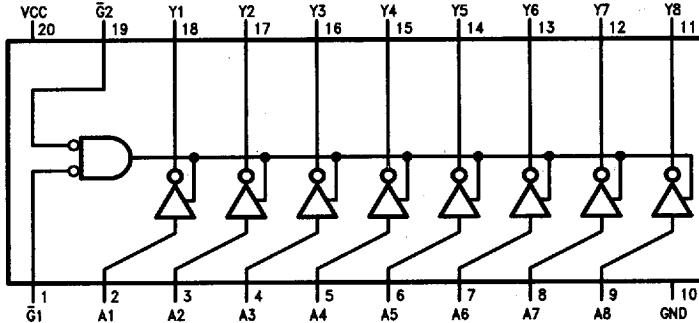
General Description

This octal buffer and line driver is designed to have the performance of the 'ALS240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout. The TRI-STATE control gate is a 2-input NOR such that if either G1 or G2 is high, all eight outputs are in the high impedance state.

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching performance is guaranteed over full temperature and V_{CC} supply range
- Data flow-thru pinout (All inputs on opposite side from outputs)
- P-N-P inputs reduce DC loading

Connection Diagram



TL/F/9170-1

Order Number DM74ALS540AWM, DM74ALS540ASJ or DM74ALS540AN
See NS Package Number M20B, M20D or N20A

Function Table

Inputs			Output Y
G1	G2	A	
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	L	H
L	L	H	L

H = High Logic Level, L = Low Logic Level

X = Don't Care (Either High or Low Logic Level)

Hi-Z = High Impedance (Off) State

Switching Characteristics over recommended free air operating temperature range (Note 1)

Symbol	Parameter	Conditions	From (Input) To (Output)	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	$V_{CC} = 4.5V \text{ to } 5.5V,$ $R_1 = R_2 = 500\Omega,$ $C_L = 50 \text{ pF}$	A or B to Y	2	12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A or B to Y	2	9	ns
t_{PZH}	Output Enable Time to High Level Output		\bar{G} to Y	5	15	ns
t_{PZL}	Output Enable Time to Low Level Output		\bar{G} to Y	8	20	ns
t_{PHZ}	Output Disable Time from High Level Output		\bar{G} to Y	1	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		\bar{G} to Y	2	12	ns

Note 1: See Section 5 for test waveforms and output load.