Semiconductor Corporation

CS5349

Single Supply, Stereo A/D Converter for Digital Audio

Features

- Single +5 V Power Supply
- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz
- 90 dB Dynamic Range
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
  - 0.01dB Passband Ripple
  - 80dB Stopband Rejection
- Low Power Dissipation: 300 mW
  - Power-Down Mode for Portable Applications
- Evaluation Board Available

General Description

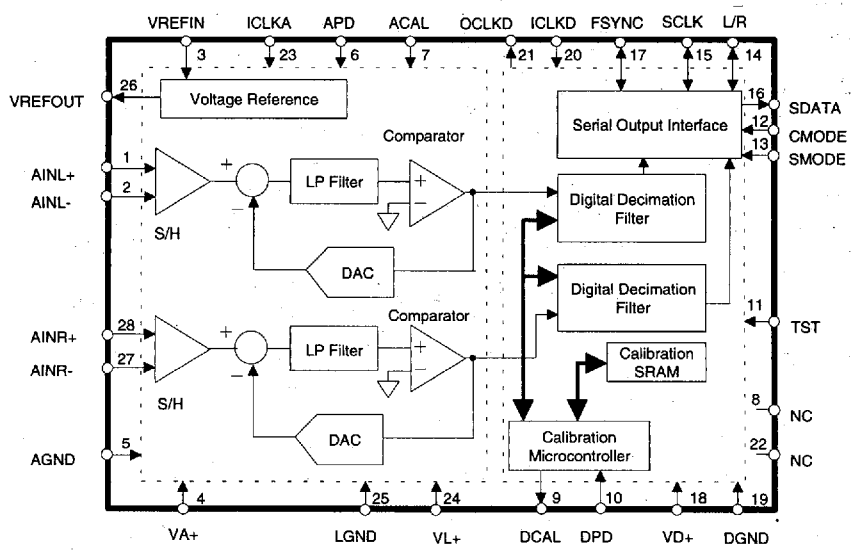
The CS5349 is a complete analog-to-digital converter which operates from a single +5V supply. It performs sampling, analog-to-digital conversion and anti-aliasing filtering, generating 16-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

The ADC uses delta-sigma modulation with 64X oversampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter.

The CS5349 has an SCLK which clocks out data on falling edges and a filter passband of dc to 24 kHz. The filter has linear phase, 0.01 dB passband ripple, and >80 dB stopband rejection.

The device is available housed in a 0.6" wide 28-pin plastic DIP, and also in a 0.3" wide 28-pin SOIC surface mount package.

ORDERING INFORMATION: Page 3-121



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ANALOG CHARACTERISTICS

(T_A = 25°C for K grade, T_A = -40 °C to +85 °C for B grade; VA+, VL+,VD+ = 5V; Full-Scale Input Sinewave, 1kHz; Output word rate = 48 kHz; SCLK = 3.072 MHz; Source Impedance = 100Ω with 500 pF across AIN+, AIN-; VREFIN connected to VREFOUT; DCAL Connected to ACAL; Master Mode; Measurement Bandwidth is 10 Hz to 20 kHz; unless otherwise specified.)

Parameter*	Symbol	CS5349-K Min	CS5349-K Typ	CS5349-K Max	CS5349-B Min	CS5349-B Typ	CS5349-B Max	Units
Specified Temperature Range	T_A		0 to 70			-40 to +85		°C
Resolution		16	-	-	16	-	-	Bits
Dynamic Performance								
Dynamic Range		88	90	-	86	90	-	dB
Signal-to-(Noise+Distortion) THD+N	S/(N+D)	85	87	-	84	87	-	dB
Total Harmonic Distortion V_{in} = -10 dB, 1kHz	THD	-	0.001	0.005	-	0.001	0.005	%
Interchannel Phase Deviation		-	0.0001	-	-	0.0001	-	Degrees
Interchannel Isolation (dc to 20 kHz)		-	100	-	-	100	-	dB
dc Accuracy								
Interchannel Gain Mismatch		-	0.05	-	-	0.05	-	dB
Gain Error		-	±2	±5	-	±2	±5	%
Gain Drift		-	50	-	-	50	-	ppm/°C
Bipolar Offset Error (After Calibration)		-	±3	±10	-	±3	±10	LSB
Offset Calibration Range (ACAL Low)		-	±100	-	-	±100	-	mV
Analog Input								
Differential Input Voltage Range (Full Scale) (Note 1)	VIN	3.8	4.0	-	3.8	4.0	-	Vpp
Input Impedance	ZIN	-	50	-	-	50	-	kΩ
Power Supplies								
Power Supply Current (VA+)+(VL+) with APD, DPD low	IA+	-	30	40	-	30	40	mA
VD+ (Normal Operation)	ID+	-	35	45	-	35	45	mA
Power Supply Current (VA+)+(VL+) with APD, DPD high	IA+	-	10	-	-	10	-	µA
VD+ (Power-Down Mode)	ID+	-	100	-	-	100	-	µA
Power Dissipation (APD, DPD Low)	PDN	-	325	425	-	325	425	mW
(APD, DPD High)	PDS	-	0.5	-	-	0.5	-	mW
Power Supply Rejection Ratio (dc to 26 kHz) (Note 2)	PSRR	-	50	-	-	50	-	dB
(26 kHz to 3.046 MHz)		-	90	-	-	90	-	dB

Notes: 1. Input voltage range is equal to ±{(VA+)-VREFIN}x0.8. (See Figure in Analog Connection Section)

* Refer to Parameter Definitions at the end of this data sheet.

Specifications are subject to change without notice.

DIGITAL FILTER CHARACTERISTICS

(T_A = 25 ° C; VA+, VL+ ,VD+ = 5V ± 5%; Output word rate of 48 kHz)

Parameter	Symbol	Min	Typ	Max	Units
Passband (-3 dB)		0	to	24	kHz
(-0.01 dB)		0	to	22	kHz
Passband Ripple		-	-	± 0.01	dB
Stopband		28	to	3044	kHz
Stopband Attenuation (Note 2)		80	-	-	dB
Group Delay (OWR = Output Word Rate)	t_{gd}	-	18/OWR	-	s
Group Delay Variation vs. Frequency	$\triangle t_{gd}$	-	-	0.0	us

Notes: 2. The analog modulator samples the input at 3.072MHz for an output word rate of 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency (that is: there is no rejection for n x 3.072MHz ±22kHz where n = 0,1,2,3...).

DIGITAL CHARACTERISTICS

(T_A = 25 °C; VA+, VL+ ,VD+ = 5V ± 5%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	70%VD+	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	30% VD+	V
High-Level Output Voltage at Io = -20uA	V_{OH}	4.4	-	-	V
Low-Level Output Voltage at Io = 20uA	V_{OL}	-	-	0.1	V
Input Leakage Current	Iin	-	1.0	-	uA

ABSOLUTE MAXIMUM RATINGS (AGND, LGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Analog	VA+	-0.3	-	+6.0	V
	Positive Logic	VL+	-0.3	-	(VA+)+0.3	V
	Positive Digital	VD+	-0.3	-	+6.0	V
Input Current, Any Pin Except Supplies		Iin	-	-	±10	mA
Analog Input Voltage	(AIN and VREFIN pins)	V_{INA}	-0.3	-	(VA+)+0.3	V
Digital Input Voltage		V_{IND}	-0.3	-	(VD+)+0.3	V
Ambient Temperature (power applied)		T_A	-55	-	+125	°C
Storage Temperature		T_{stg}	-65	-	+150	°C

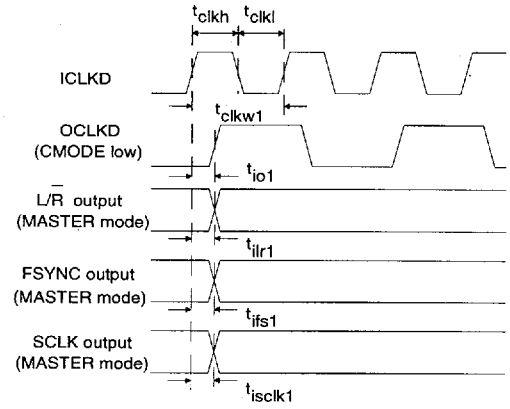
WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS

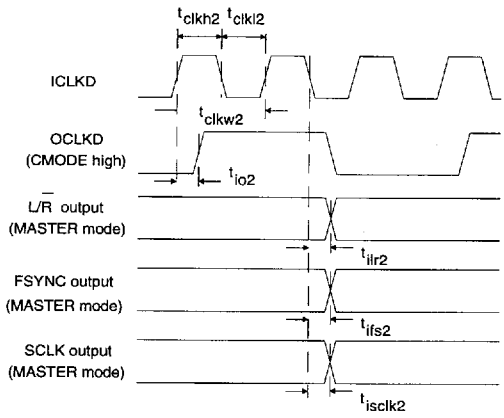
(T_A = 25 °C; VA+, VL+, VD+ = 5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VA+, VD+; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
ICLKD Period (CMODE low)	t_{clkw1}	78	-	3906	ns
ICLKD Low (CMODE low)	t_{clkl1}	31	-	-	ns
ICLKD High (CMODE low)	t_{clkh1}	31	-	-	ns
ICLKD rising to OCLKD rising (CMODE low)	t_{io1}	5	-	40	ns
ICLKD Period (CMODE high)	t_{clkw2}	52	-	2604	ns
ICLKD Low (CMODE high)	t_{clkl2}	20	-	-	ns
ICLKD High (CMODE high)	t_{clkh2}	20	-	-	ns
ICLKD rising or falling to OCLKD rising (CMODE high, Note 3)	t_{io2}	5	-	45	ns
ICLKD rising to L/$\overline{R}$ edge (CMODE low, MASTER mode)	t_{ilr1}	5	-	50	ns
ICLKD rising to FSYNC edge (CMODE low, MASTER mode)	t_{ifs1}	5	-	50	ns
ICLKD rising to SCLK edge (CMODE low, MASTER mode)	t_{isclk1}	5	-	50	ns
ICLKD falling to L/$\overline{R}$ edge (CMODE high, MASTER mode)	t_{ilr2}	5	-	50	ns
ICLKD falling to FSYNC edge (CMODE high, MASTER mode)	t_{ifs2}	5	-	50	ns
ICLKD falling to SCLK edge (CMODE high, MASTER mode)	t_{isclk2}	5	-	50	ns
SCLK falling to SDATA valid (MASTER mode)	t_{sdo}	0	-	50	ns
SCLK duty cycle (MASTER mode)		40	50	60	%
SCLK falling to L/$\overline{R}$ (MASTER mode)	t_{mslr}	-20	-	20	ns
SCLK falling to FSYNC (MASTER mode)	t_{msfs}	-20	-	20	ns
SCLK Period (SLAVE mode)	t_{sclkw}	155	-	-	ns
SCLK Pulse Width Low (SLAVE mode)	t_{sclkl}	60	-	-	ns
SCLK Pulse Width High (SLAVE mode)	t_{sclkh}	60	-	-	ns
SCLK falling to SDATA valid (SLAVE mode)	t_{dss}	-	-	50	ns
L/$\overline{R}$ edge to MSB valid (SLAVE mode)	t_{lrdss}	-	-	50	ns
Rising SCLK to L/$\overline{R}$ edge delay (SLAVE mode)	t_{slr1}	30	-	-	ns
L/$\overline{R}$ edge to rising SCLK setup time (SLAVE mode)	t_{slr2}	30	-	-	ns
Rising SCLK to rising FSYNC delay (SLAVE mode)	t_{sfs1}	30	-	-	ns
Rising FSYNC to rising SCLK setup time (SLAVE mode)	t_{sfs2}	30	-	-	ns
DPD pulse width	t_{pdw}	$2t_{clkw}$	-	-	ns
DPD rising to DCAL rising	t_{pcr}	-	-	50	ns
DPD falling to DCAL falling (OWR = Output Word Rate)	t_{pcf}		4096		1/OWR

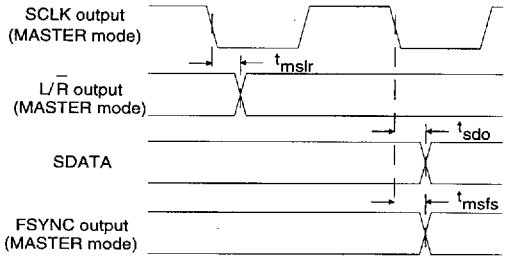
Notes: 3. ICLKD rising or falling depends on DPD to L/$\overline{R}$ timing (see Figure 2).



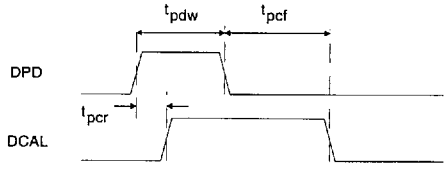
ICLKD to Outputs Propagation Delays (CMODE low)



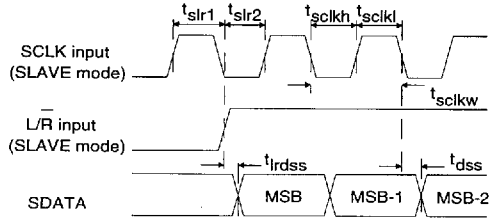
ICLKD to Outputs Propagation Delays (CMODE high)



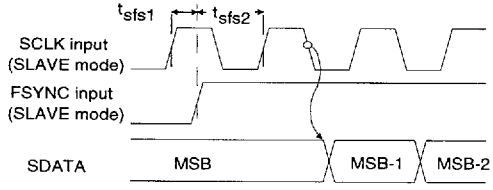
SCLK to SDATA, L/R & FSYNC - MASTER Mode



Power Down & Calibration Timing



SCLK to L/R & SDATA - SLAVE mode, FSYNC high



FSYNC to SCLK - SLAVE Mode, FSYNC Controlled.

RECOMMENDED OPERATING CONDITIONS

(AGND, LGND, DGND = 0V; all voltages with respect to ground)

Parameter			Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	(Note 5)	VD+	4.75	5.0	5.25	V
	Positive Logic		VL+	4.75	5.0	VA+	V
	Positive Analog		VA+	4.75	5.0	5.25	V
Differential Analog Input Voltage		(Note 6)	V_{AIN}	3.8	4.0	-	Vpp
Analog Input Bias Voltage			V_{BIAS}	-	0.5VA+	-	V

Notes: 5. VD+ must be within 0.3V of VA+.

6. The output codes will clip at full scale with input signals >4Vpp, but <8Vpp. Input signals >8Vpp will cause indeterminate output codes. These voltages are subject to the gain error tolerance specification. Additional tag bits are output to indicate a near to clipping and overdrive condition.

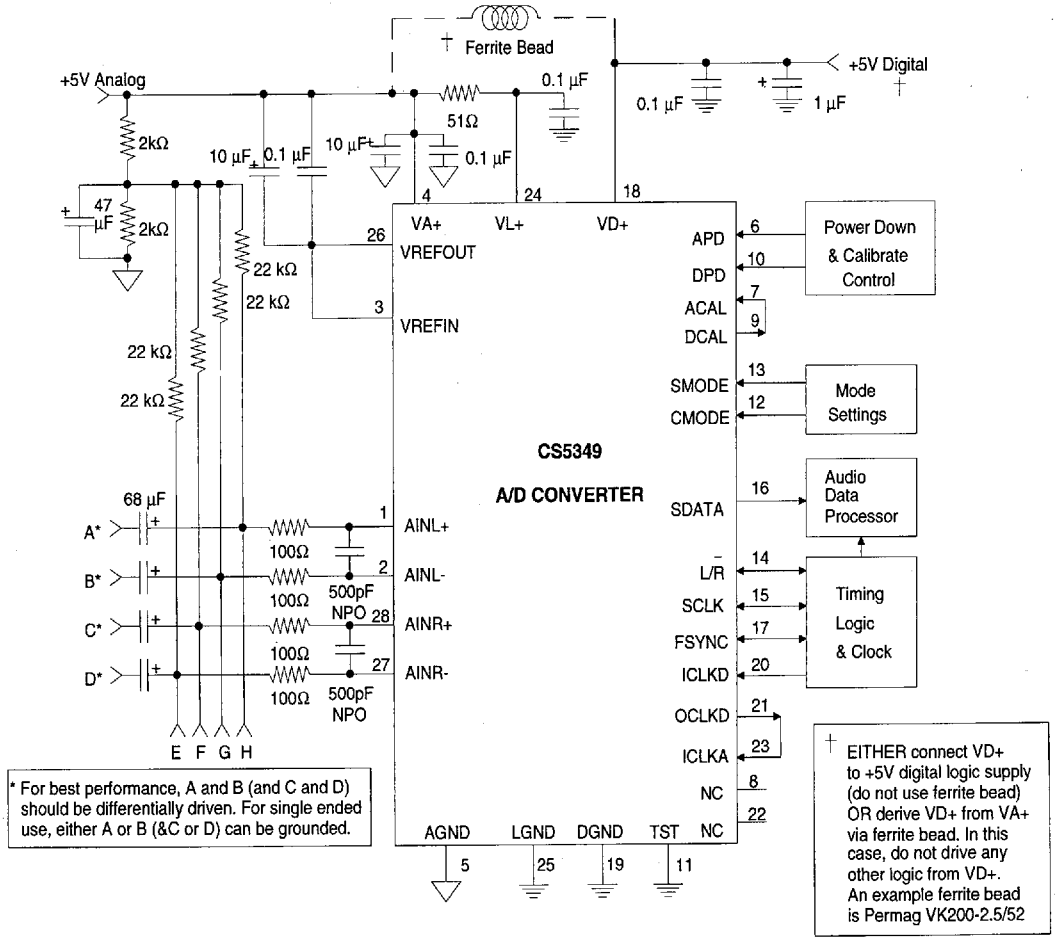


Figure 1. Typical Connection Diagram

GENERAL DESCRIPTION

The CS5349 is a 16-bit, 2-channel A/D converter designed specifically for stereo digital audio applications that require a single +5V supply. The device uses two one-bit delta-sigma modulators which simultaneously sample the analog input signals at a 64 X sampling rate. The resulting serial bit streams are digitally filtered, yielding pairs of 16-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converters do not require difficult-to-design or expensive anti-alias filters, and do not require external sample-and-hold amplifiers or a voltage reference.

An on-chip voltage reference provides for a differential input signal range of 4Vpp. Any zero offset is internally calibrated out during a power-up self-calibration cycle. Output data is available in serial form, coded as 2's complement 16-bit numbers. Typical power consumption of only 300 mW can be further reduced by use of the power-down mode.

For more information on delta-sigma modulation and the particular implementation inside this ADC, see the references at the end of this data sheet.

L/$\overline{R}$ (kHz)	CMODE	ICLKD (MHz)	OCLKD/ ICLKA (MHz)	SCLK (MHz)
32	low	8.192	4.096	2.048
32	high	12.288	4.096	2.048
44.1	low	11.2896	5.6448	2.8224
44.1	high	16.9344	5.6448	2.8224
48	low	12.288	6.144	3.072
48	high	18.432	6.144	3.072

Table 1. Common Clock Frequencies

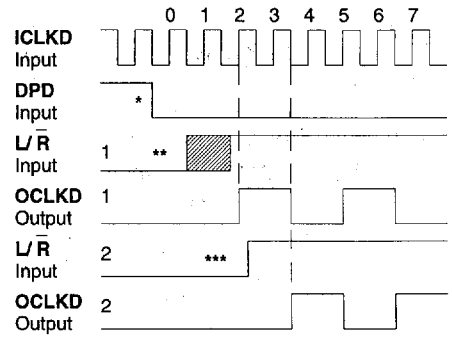
SYSTEM DESIGN

Very few external components are required to support the ADC. Normal power supply decoupling components, voltage reference bypass capacitors and a resistor and capacitor on each input for anti-aliasing are all that's required, as shown in Figure 1.

Master Clock Input

The master input clock (ICLKD) into the ADC runs the digital filter, and is used to generate the modulator sampling clock. ICLKD frequency is determined by the desired Output Word Rate (OWR) and the setting of the CMODE pin. CMODE high will set the required ICLKD frequency to 384 X OWR, while CMODE low will set the required ICLKD frequency to 256 X OWR. Table 1 shows some common clock frequencies. The digital output clock (OCLKD) is always equal to 128 X OWR, which is always 2 X the input sample rate. OCLKD should be connected to ICLKA, which controls the input sample rate.

The phase alignment between ICLKD and OCLKD is determined as follows: when



* DPD low is recognized on the next ICLKD rising edge (#0)
** L/$\overline{R}$ rising before ICLKD rising #2 causes OCLKD -1
*** L/$\overline{R}$ rising after ICLKD rising #2 causes OCLKD - 2

Figure 2. ICLKD to OCLKD Timing with CMODE high (384 X OWR)

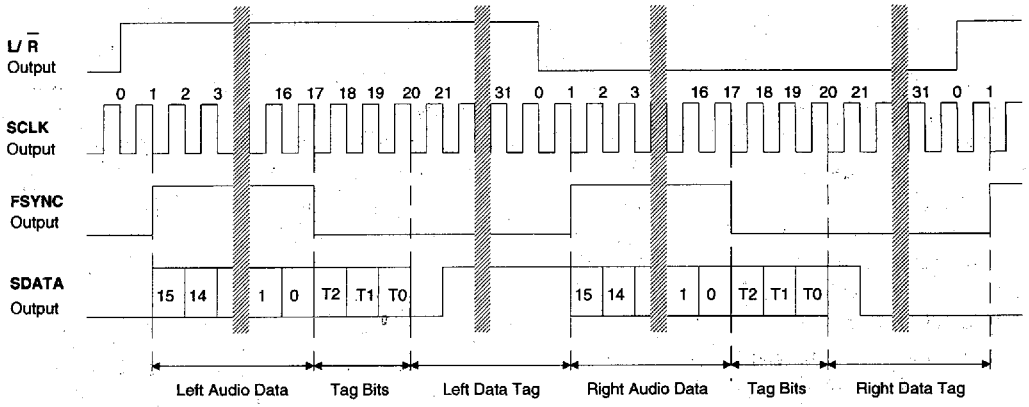


Figure 3. Data Output Timing - MASTER mode

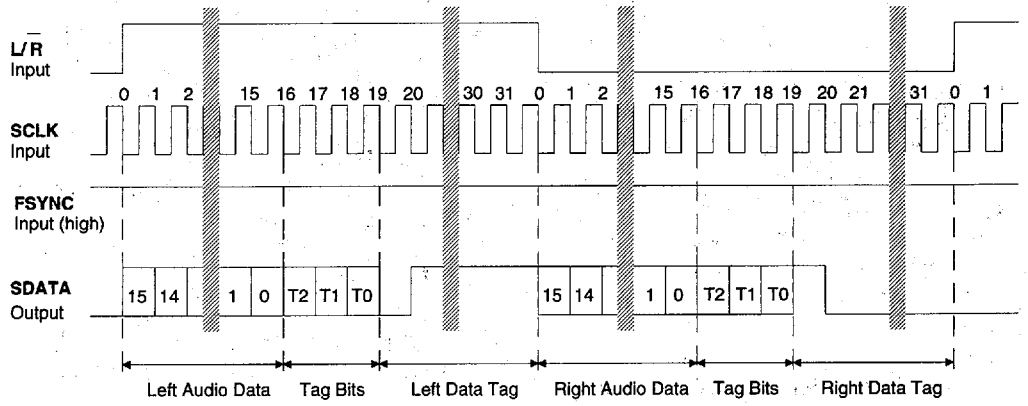


Figure 4. Data Output Timing - SLAVE Mode, FSYNC high

CMODE is low, ICLKD is divided by 2 to generate OCLKD. The phase relationship between ICLKD and OCLKD is always the same, and is shown in the Switching Characteristics Timing Diagrams. When CMODE is high, OCLKD is ICLKD divided by 3. There are two possible phase relationships between ICLKD and OCLKD, which depend on the start-up timing between DPD and L/$\overline{R}$, shown in Figure 2.

Serial Data Interface

The serial data output interface has 3 possible modes of operation: MASTER mode, SLAVE mode with FSYNC high, and SLAVE mode with FSYNC controlled. In MASTER mode, the A/D converter is driven from a master clock (ICLKD) and outputs all other clocks, derived from ICLKD (see Figure 3). Notice the one SCLK cycle delay between L/$\overline{R}$ edges and FSYNC rising edges. FSYNC brackets the 16 data bits for each channel.

In SLAVE mode, L/$\overline{R}$ and SCLK are inputs. L/$\overline{R}$ must be externally derived from ICLKD, and should be equal to the Output Word Rate. SCLK should be equal to the input sample rate, which is equal to OCLKD/2. Other SCLK frequencies are possible, but may degrade dynamic range because of interference effects. Data bits are clocked out via the SDATA pin using the SCLK

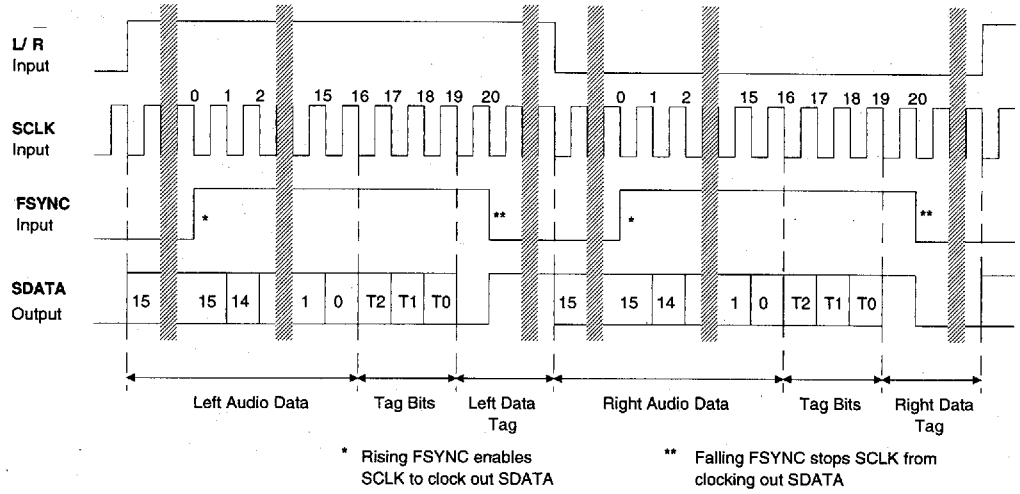


Figure 5 Data Output Timing-SLAVE Mode, FSYNC controlled

and L/$\overline{R}$ inputs. The falling edge of SCLK causes the ADC to output each bit, except the MSB, which is clocked out by the L/$\overline{R}$ edge. As shown in Figure 4, when FSYNC is high, serial data bits are clocked immediately following the L/$\overline{R}$ edge.

In SLAVE mode with FSYNC controlled, as shown in Figure 5, when FSYNC is low, only the MSB is clocked out after the L/$\overline{R}$ edge. With FSYNC low, SCLK is ignored. When it is desired to start clocking out data, bring FSYNC high which enables SCLK to start clocking out data. Bringing FSYNC low will stop the data being clocked out. This feature is particularly useful to position in time the data bits onto a common serial bus.

Input Level	T2	T1	T0
1.375 x FS	1	1	1
1.250 x FS to 1.375 x FS	1	1	0
1.125 x FS to 1.250 x FS	1	0	1
1.000 x FS to 1.125 x FS	1	0	0
-1.006dB to 0.000dB	0	1	1
-3.060dB to -1.006dB	0	1	0
-6.000dB to -3.060dB	0	0	1
< -6.000dB	0	0	0

FS = Full Scale (0dB) Input

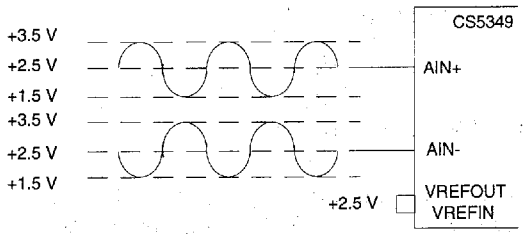
Table 2. Tag Bit Definition

The serial nature of the output data results in the left and right data words being read at different times. However, the words within an L/$\overline{R}$ cycle represent simultaneously sampled analog inputs.

In all modes, additional bits are output after the data bits: 3 tag bits and a left/right indicator. The tag bits indicate a near-to-clipping input condition for the data word to which the tag bits are attached. Table 2 shows the relationship between input level and the tag bit values. The serial bit immediately following the tag bits is 0 for the left channel, and 1 for the right channel. The remaining bits before the next L/$\overline{R}$ edge will be 1's for the left channel and 0's for the right channel. Normally, the tag bits are separated from the audio data by the digital signal processor. However, if the tag bits are interpreted as audio data, their position below the LSB would result as a very small dc offset.

Analog Connections

Figure 1 shows the analog input connections. The analog inputs are presented differentially to the modulators via the AINR+, AINR- and AINL+, AINL- pins. Each analog input will accept a maximum of 2 Vpp centered at +2.5 V. The + and - input signals are 180° out of phase resulting in an effective input voltage of 4 Vpp. Figure 6 shows the input signal levels for full scale.



Full Scale Input level= (AIN+) - (AIN-)= 2 Vp or 4 Vpp

Figure 6. Full Scale Input Voltage

The CS5349 samples the analog inputs at 3.072 MHz for a 12.288 MHz ICLKD (CMODE low). The digital filter rejects all noise between 28 kHz and (3.072 MHz-28 kHz). However, the filter will not reject frequencies right around 3.072 MHz (and multiples of 3.072 MHz). Most audio signals do not have significant energy at 3.072 MHz. Nevertheless, a 100 Ω resistor in series with the analog input, and a 500 pF NPO or COG capacitor across the inputs will attenuate any noise energy at 3.072 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) should be avoided since these will degrade signal linearity. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins. The above example frequencies scale linearly with output word rate.

As an alternative to Figure 1 input arrangements, Figure 7 shows an active input buffer circuit which produces a differential output and level

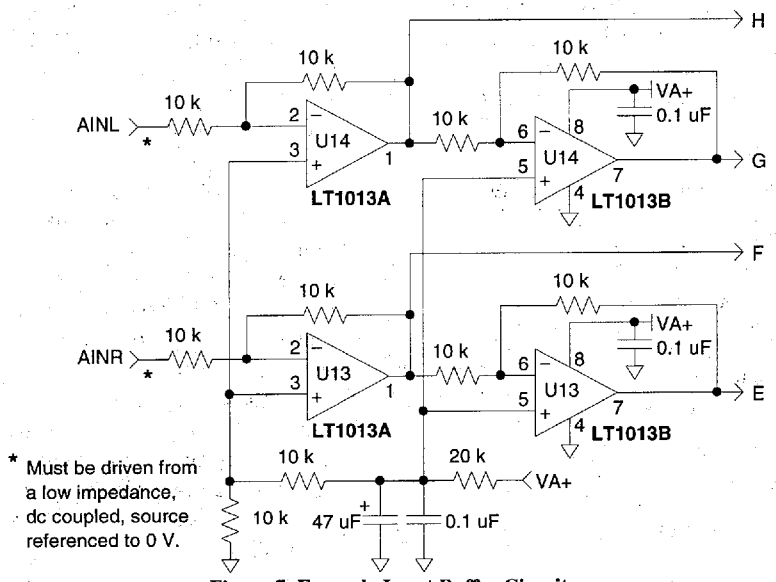


Figure 7. Example Input Buffer Circuit

shifts up to +2.5 V. This circuit must be driven from a source which is referred to 0V dc. If this circuit is used, then the level shifting and AC coupling components shown in Figure 1 are not required.

The on-chip voltage reference output (2.5 V) is brought out to the VREFOUT pin, and normally connected to VREFIN. External reference voltages between 1.5 V and 3.0 V may be used. A 10 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor attached between VREFIN and VA+ eliminates the effects of high frequency noise. No load current may be taken from the VREFOUT output pin.

Power-Down and Offset Calibration

The ADC has a power-down mode wherein typical consumption drops to 0.5 mW. In addition, exiting the power-down state initiates an offset calibration procedure.

APD and DPD are the analog and digital power-down pins. When high, they place the analog and digital sections in the power-down mode. Bringing these pins low takes the part out of power-down mode. DPD going low initiates a calibration cycle. If not using the power down feature, APD should be tied to AGND. When using the power down feature, DPD and APD may be tied together if the capacitor on VREF is not greater than 10 µF, as stated in the "Power-Up Considerations" section.

During the offset calibration cycle, the digital section of the part measures and stores the value of the calibration input of each channel in registers. The calibration input value is subtracted from all future outputs. The calibration input comes from either the analog input signals or by the value obtained from shorting the differential inputs together. This input is determined by the state of the ACAL pin. With ACAL low, the calibration input is obtained from the analog inputs. With ACAL in a high state, the differential inputs are disconnected from the device input pins and shorted internally to provide the calibration input value.

As shown in Figure 8, the DCAL output is high during calibration, which takes 4096 L/$\overline{R}$ clock cycles. If DCAL is connected to the ACAL input, the calibration routine will measure the voltage resulting from the shorted inputs. Internal offsets of each channel will thus be measured and subsequently subtracted.

Alternatively, ACAL may be permanently connected low and DCAL utilized to control a multiplexer which grounds the user's front end. In this case, the calibration routine will measure and store not only the internal offsets but also any offsets present in the front end input circuitry.

During calibration, the digital output of both channels is forced to a 2's complement zero. Subtraction of the calibration input from conversions after calibration substantially reduces any

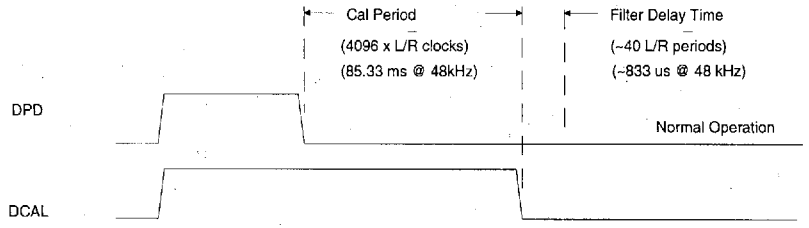


Figure 8. Initial Calibration Cycle Timing

power-on click that might otherwise be experienced. A short delay of approximately 40 output words will occur following calibration for the digital filter to begin accurately tracking audio band signals.

Power-up Considerations

Upon initial application of power to the supply pins, the data in the calibration registers will be indeterminate. A calibration cycle should always be initiated after application of power to replace potentially large values of data in these registers with the correct values.

The modulators settle very quickly (a matter of microseconds) after the analog section is powered on, either through the application of power, or by exiting the power-down mode. The voltage reference can take a much longer time to reach a final value due to the presence of large external capacitance on the VREF pin; allow approximately 5 ms/µF. The calibration period is long enough to allow the reference to settle for capacitor values of up to 10 µF. If a larger capacitor is used, additional time between APD going low and DPD going low should be allowed for VREF settling before a calibration cycle is initiated.

Grounding and Power Supply Decoupling

As with any high resolution converter, the ADC requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA+ and VL+ connected to a clean +5 V supply. VD+, which powers the digital filter, may be run from the system +5V logic supply, provided that it is not excessively noisy (< ± 50 mV pk-to-pk). Alternatively, VD+ may be powered from VA+ via a ferrite bead. In this case, no additional devices should be powered from VD+. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest.

The printed circuit board layout should have separate analog and digital regions and ground planes, with the ADC straddling the boundary. All signals, especially clocks, should be kept away from the VREF pin in order to avoid unwanted coupling into the modulators. An evaluation board is available which demonstrates the optimum layout and power supply arrangements, as well as allowing fast evaluation of the ADC.

To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

Synchronization of Multiple CS5349

In systems where multiple ADC's are required, care must be taken to insure that the ADC internal clocks are synchronized between converters to insure simultaneous sampling. In the absence of this synchronization, the sampling difference could be one ICLKD period which is typically 81.4 nsec for a 48 kHz sample rate.

SLAVE MODE

Synchronous sampling in the slave mode is achieved by connecting all DPD and APD pins to a single control signal and supplying the same ICLKD and $L/\overline{R}$ to all converters.

MASTER MODE

The internal counters of the CS5349 are reset during DPD/APD high and will start simultaneously by insuring that the release of DPD/APD for all converters is internally latched on the same rising edge of ICLKD. This can be achieved by connecting all DPD/APD pins to the same control signal and insuring that the

DPD/APD falling edge occurs outside a ±30 ns window either side of an ICLKD rising edge.

PERFORMANCE

Digital Filter

Figures 10 through 12 show the performance of the digital filter included in the ADC. All the plots assume an output word rate of 48 kHz. The filter frequency response will scale precisely with changes in output word rate. The passband ripple is flat to ± 0.01 dB maximum. Stopband rejection is greater than 80 dB. Figure 12 is an expanded view of the transition band.

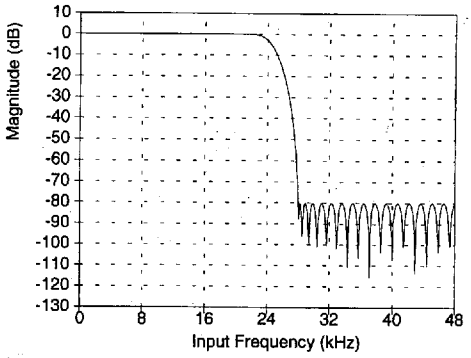


Figure 10. CS5349 Digital Filter Stopband Rejection

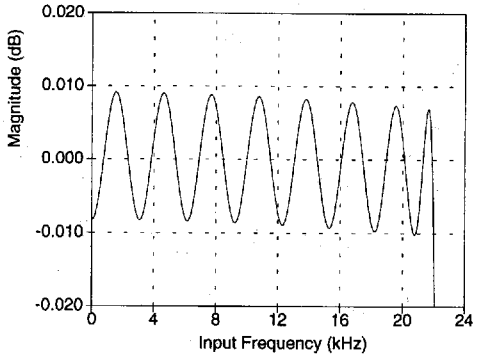


Figure 11. CS5349 Digital Filter Passband Ripple

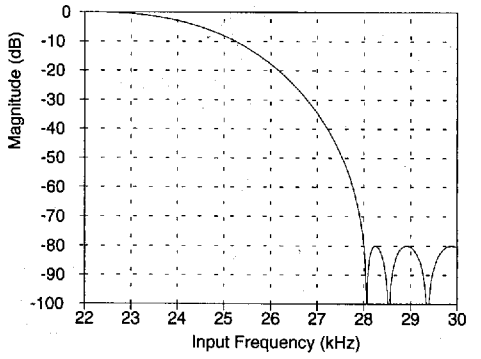


Figure 12. CS5349 Digital Filter Transition Band

Performance Measurements

All the following performance measurements were taken using an Audio Precision System One Dual Domain tester. The CS5349 was in a CDB5349 evaluation board, running at 48 kHz word rate and interfaced to the System One Via the AES/EBU input using a CS8402 AES/EBU transmitter.

Figure 13 shows the frequency response, which is essentially flat.

Figure 14 shows the noise floor with zero input signal level. A 16 K point FFT was used.

Figure 15 shows a 1 kHz, -10 dB input signal FFT plot. Notice the low 2nd harmonic at -110 dB.

Figure 16 shows a 1 kHz, -80 dB input signal FFT plot. Notice the lack of harmonic distortion components. This is a direct result of the perfect differential non-linearity, which is one of the benefits of the delta-sigma technique.

Figure 17 shows the THD+N versus input level at 1 kHz. This plot indicates a dynamic range of 90 dB, with a small increase in distortion with a full scale input.

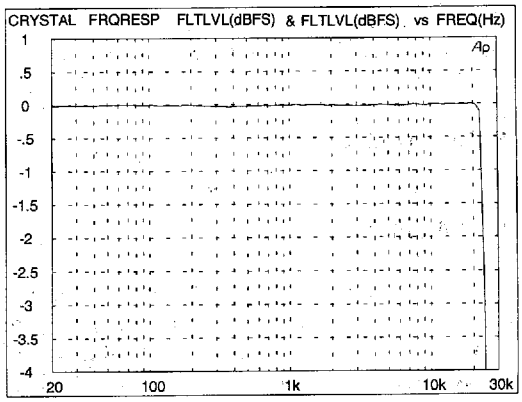


Figure 13. Frequency Response

Figure 18 shows THD+N versus frequency at -10 dB input. This indicates a value of 90 dB, with minor degradation at high frequency.

Figure 19 shows the linearity of the CS5349. The input signal is at 500 Hz and is varied from 0 dB (full scale) to -120 dB. At each input level, the output level is measured and compared to the perfect value. Any deviation is plotted as a deviation away from 0 dB. Notice the close conformance to perfect linearity, until the noise starts to influence the readings at about -100 dB.

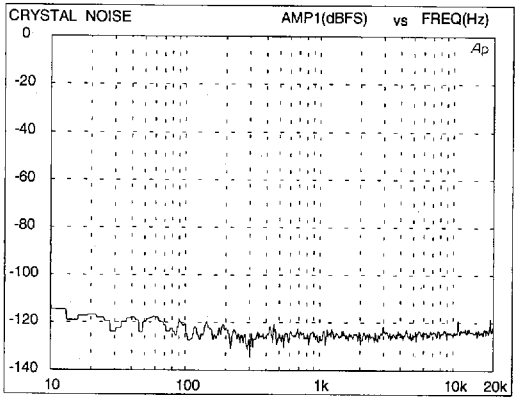


Figure 14 Noise Floor

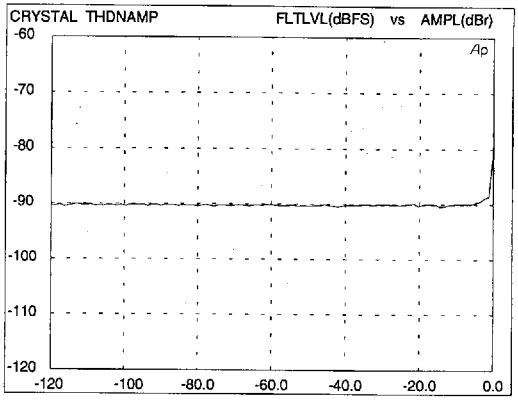


Figure 17. THD+N vs Input level at 1 kHz

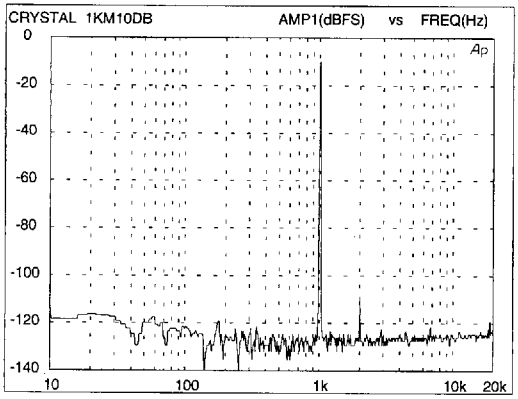


Figure 15. 1 kHz, -10 dB input FFT

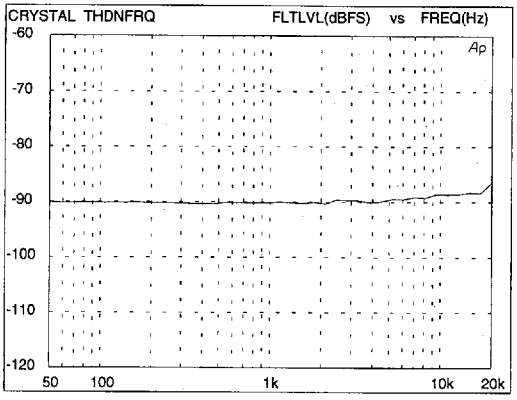


Figure 18. THD+N vs Frequency at -10 dB

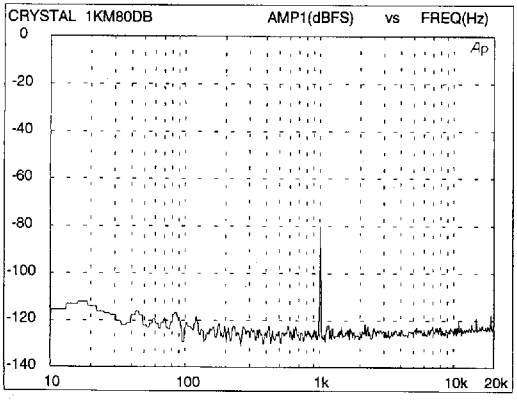


Figure 16. 1 kHz, -80 dB input FFT

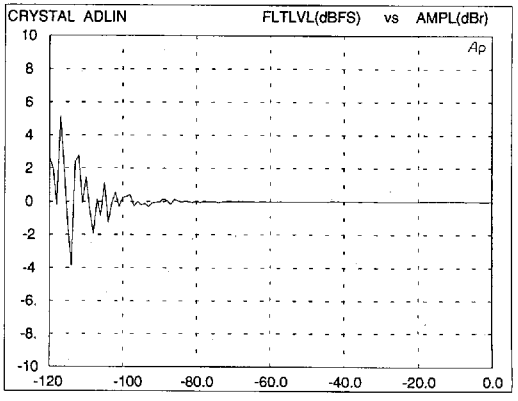
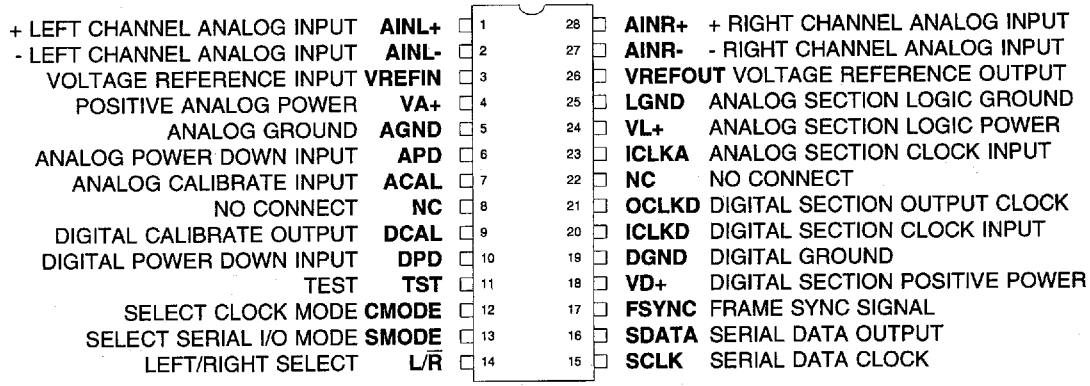


Figure 19. Output level Error vs. Input level at 500 Hz

PIN DESCRIPTIONS



Power Supply Connections

VA+ - Positive Analog Power, PIN 4.
Positive analog supply. Nominally +5 volts.

VL+ - Positive Logic Power, PIN 24.
Positive logic supply for the analog section. Nominally +5 volts.

AGND - Analog Ground, PIN 5.
Analog ground reference.

LGND - Logic Ground, PIN 25
Ground for the logic portions of the analog section.

VD+ - Positive Digital Power, PIN 18.
Positive supply for the digital section. Nominally +5 volts.

DGND - Digital Ground, PIN 19.
Digital ground for the digital section.

Analog Inputs

±AINL, ±AINR - Differential Left and Right Channel Analog Inputs, PINS 1, 2, 27, 28
Analog input connections for the left and right input channels. Nominally 4Vpp full scale.

VREFIN - Voltage Reference Input, Pin 3
Normally tied to VREFOUT for 4Vpp differential input levels.

Analog Outputs

VREFOUT - Voltage Reference Output, PIN 26.

Nominally +2.5 volts. Must be bypassed to VA+ with a 0.1 µF ceramic capacitor in parallel with a 10 µF electrolytic capacitor. Normally connected to VREFIN.

Digital Inputs

ICLKA - Analog Section Input Clock, PIN 23.

This clock is internally divided by 2 to set the modulators' sample rate. Sampling rates, output rates, and digital filter characteristics scale to ICLKA frequency. ICLKA frequency is 128 X the output word rate. For example, a 6.144 MHz ICLKA corresponds to an output word rate of 48 kHz per channel. Normally connected to OCLKD.

ICLKD - Digital Section Input Clock, PIN 20.

This is the clock which runs the digital filter. ICLKD frequency is determined by the required output word rate and by the CMODE pin. If CMODE is low, ICLKD frequency should be 256 X the desired output word rate. If CMODE is high, ICLKD should be 384 X the desired output word rate. For example, with CMODE low, ICLKD should be 12.288 MHz for an output word rate of 48 kHz. This clock also generates OCLKD, which is always 128 X the output word rate.

APD - Analog Power Down, PIN 6.

Analog section power-down command. When high, the analog circuitry is in power-down mode. APD is normally connected to DPD when using the power down feature. If power down is not used, then connect APD to AGND.

DPD - Digital Power Down, PIN 10

Digital section power-down command. Bringing DPD high puts the digital section into power-down mode. Upon returning low, the ADC starts an offset calibration cycle. This takes 4096 L/R periods (85.33 ms with a 12.288 MHz ICLKD). DCAL is high during the calibrate cycle and goes low upon completion. DPD is normally connected to APD when using the power down feature. A calibration cycle should always be initiated after applying power to the supply pins.

ACAL - Analog Calibrate, PIN 7.

Analog section calibration command. When high, causes the left and right channel modulator differential inputs to be shorted together. May be connected to DCAL.

CMODE - Clock Mode Select, PIN 12.

CMODE should be tied low to select an ICLKD frequency of 256 X the output word rate. CMODE should be tied high to select an ICLKD frequency of 384 X the output word rate.

SMODE - Serial Interface Mode Select, PIN 13.

SMODE should be tied high to select serial interface master mode, where SCLK, FSYNC and L/R are all outputs, generated by internal dividers operating from ICLKD. SMODE should be tied low to select serial interface slave mode, where SCLK, FSYNC and L/R are all inputs. In slave mode, L/R, FSYNC and SCLK need to be derived from ICLKD using external dividers.

Digital Outputs

SDATA - Serial Data Output, PIN 16.

Audio data bits are presented MSB first, in 2's complement format. Additional tag bits, which indicate input overload and left/right channel data, are output immediately following each audio data word.

DCAL - Digital Calibrate Output, PIN 9.

DCAL rises immediately upon entering the power-down state (DPD brought high). It returns low 4096 L/R periods after leaving the power down state (DPD brought low), indicating the end of the offset calibration cycle (which = 85.33 ms with a 12.288 MHz ICLKD). May be connected to ACAL.

OCLKD - Digital Section Output Clock, PIN 21.

OCLKD is always 128 X the output word rate. Normally connected to ICLKA.

Digital Inputs or Outputs

SCLK - Serial Data Clock, PIN 15.

Data is clocked out on the falling edge of SCLK.

In master mode (SMODE high), SCLK is a continuous output clock at 64 X the output word rate.

In slave mode (SMODE low), SCLK is an input, which requires a clock at any frequency from 32 X to 128 X the output word rate (64 X is preferred). When FSYNC is high, SCLK clocks out serial data, except for the MSB which appears on SDATA when L/R changes.

L/$\overline{R}$ - Left/Right Select, PIN 14.

In master mode (SMODE high), L/$\overline{R}$ is an output whose frequency is at the output word rate. L/$\overline{R}$ edges occur 1 SCLK cycle before FSYNC rises. When L/R is high, left channel data is on SDATA, except for the first SCLK cycle. When L/R is low, right channel data is on SDATA, except for the first SCLK cycle. The MSB data bit appears on SDATA one SCLK cycle after L/R changes.

In slave mode (SMODE low), L/$\overline{R}$ is an input which selects the left or right channel for output on SDATA. The rising edge of L/R starts the MSB of the left channel data. L/R frequency must be equal to the output word rate.

Although the outputs of each channel are transmitted at different times, the two words in an L/R cycle represent simultaneously sampled analog inputs.

FSYNC - Frame Synchronization Signal, PIN 17.

In master mode (SMODE high), FSYNC is an output which goes high coincident with the start of the first SDATA bit (MSB) and falls low immediately after the last SDATA audio data bit (LSB).

In slave mode (SMODE low), FSYNC is an input which controls the clocking out of the data bits on SDATA. FSYNC is normally tied high, which causes the data bits to be clocked out immediately following L/R transitions. If it is desired to delay the data bits from the L/R edge, then FSYNC must be low during the delay period. Bringing FSYNC high will then enable the clocking out of the SDATA bits. Note that the MSB will be clocked out based on the L/R edge, independent of the state of FSYNC.

Miscellaneous

NC - No Connection, PINS 8, 22.

These two pins are bonded out to test outputs. They must not be connected to any external component or any length of PC trace.

TST -Test Input, PIN 11.

Allows access to the ADC test modes, which are reserved for factory use. Must be tied to DGND.

PARAMETER DEFINITIONS

Resolution - The total number of possible output codes is equal to 2^N, where N = the number of bits in the output word for each channel.

Dynamic Range - Full scale (RMS) signal to broadband noise ratio. The broadband noise is measured over the specified bandwidth, and with an input signal 60dB below full-scale. Units in decibels.

Signal-to-Noise plus Distortion Ratio - The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Total Harmonic Distortion - The ratio of the rms sum of all harmonics up to 20 kHz to the rms value of the signal. Units in percent.

Interchannel Phase Deviation - The difference between the left and right channel sampling times.

Interchannel Isolation - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test grounded and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch - The gain difference between left and right channels. Units in decibels.

Gain Error - The deviation of the measured full scale amplitude from the ideal full scale amplitude value.

Gain Drift - The change in gain value with temperature. Units in ppm/°C.

Bipolar Offset Error - The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (1/2 LSB below AGND). Units in LSBs.

REFERENCES - All reprinted in this data book.

1) "A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio" by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.

2) " The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's" by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

3) " An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example" by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

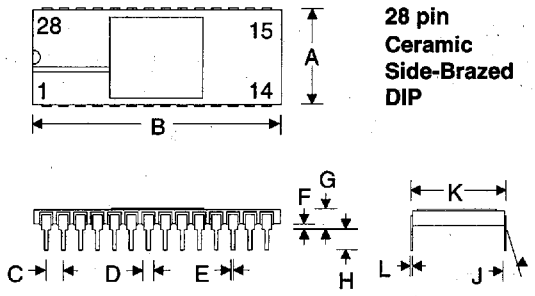
Ordering Guide

Model	Resolution	Passband	SCLK	Temperature	Package
CS5349-KP	16-bits	24 kHz	↓ active	0°C to 70 °C	28-pin Plastic DIP
CS5349-BP	16-bits	24 kHz	↓ active	-40°C to 85 °C	28-pin Plastic DIP
CS5349-KS	16-bits	24 kHz	↓ active	0°C to 70 °C	28-pin SOIC
CS5349-BS	16-bits	24 kHz	↓ active	-40°C to 85 °C	28-pin SOIC

CDB5349 CS5349 Evaluation Board

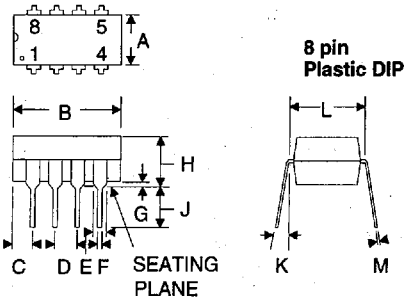
"KP" and "KS" suffix parts are guaranteed to operate over 0°C to 70°C, but tested only at 25°C. "BP" and "BS" suffix parts are tested at the temperature extremes -40°C and +85°C.

MECHANICAL DATA



28 pin Ceramic Side-Brazed DIP

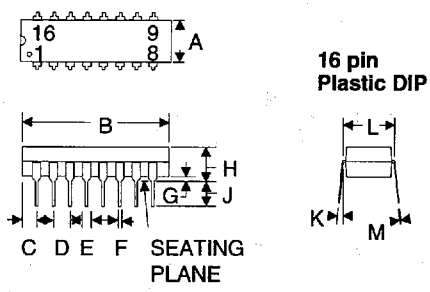
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.73	15.34	0.580	0.604
B	35.20	35.92	1.386	1.414
C	2.54 BSC		0.100 BSC	
D	0.76	1.40	0.030	0.055
E	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.79	4.32	0.110	0.170
H	2.54	4.57	0.100	0.180
J	-	10°	-	10°
K	14.99	15.49	0.590	0.610
L	0.20	0.30	0.008	0.012



8 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	9.14	10.2	0.360	0.400
C	0.38	1.52	0.015	0.060
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

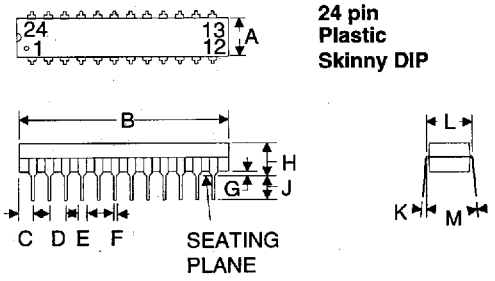
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



16 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	18.80	19.30	0.740	0.760
C	1.32	2.89	0.015	0.035
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

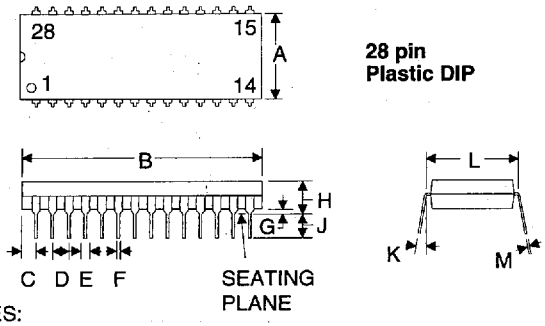
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



24 pin
Plastic
Skinny DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	31.37	32.13	1.235	1.265
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	4.57	0.155	0.180
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	7.62 BSC		0.300 BSC	
M	0.20	0.38	0.008	0.015

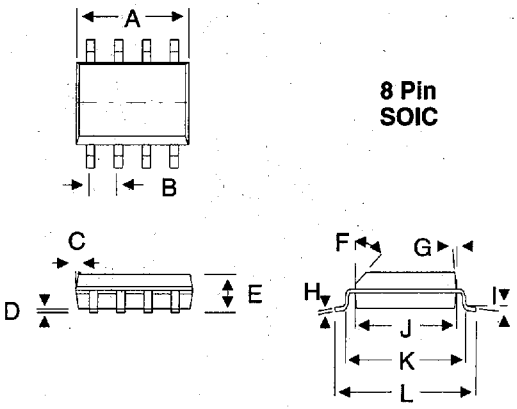
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



28 pin
Plastic DIP

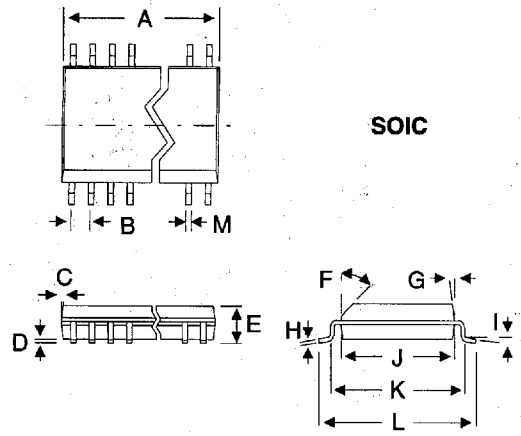
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	36.45	37.21	1.435	1.465
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



8 Pin
SOIC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.25	5.30	0.207	0.209
B	1.27 TYP		0.050 TYP	
C	7° NOM		7° NOM	
D	0.120	0.180	0.005	0.007
E	1.80	1.86	0.071	0.073
F	45° NOM		45° NOM	
G	7° NOM		7° NOM	
H	0.195	0.205	0.0078	0.0082
I	2°	4°	2°	4°
J	-	-	-	-
K	6.57	6.63	0.259	0.261
L	7.85	7.95	0.308	0.312

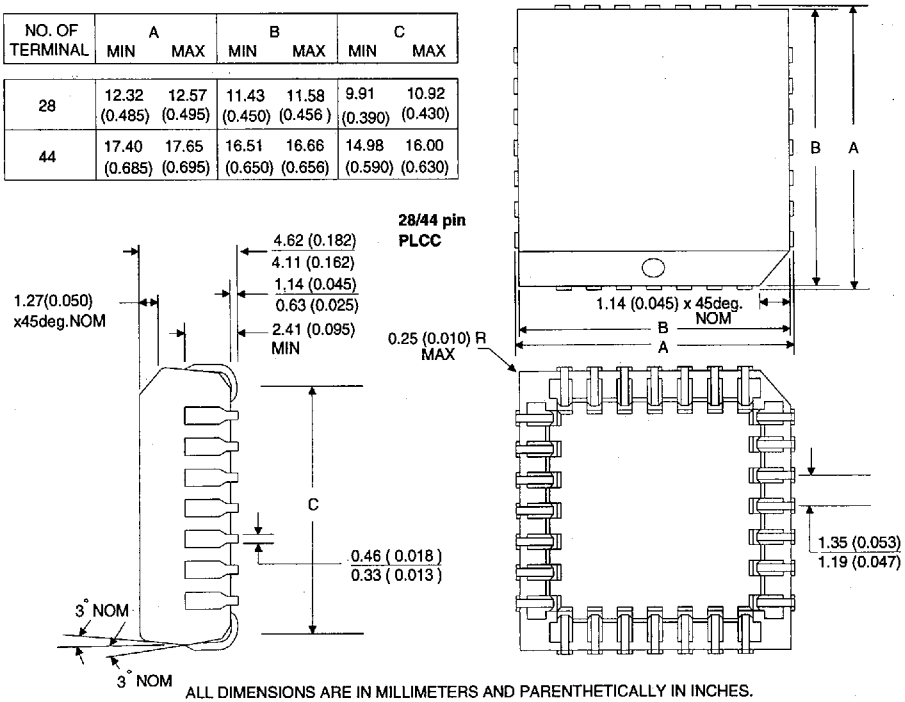


SOIC

pins	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
16	9.91	10.41	0.390	0.410
20	12.45	12.95	0.490	0.510
24	14.99	15.50	0.590	0.610
28	17.53	18.03	0.690	0.710

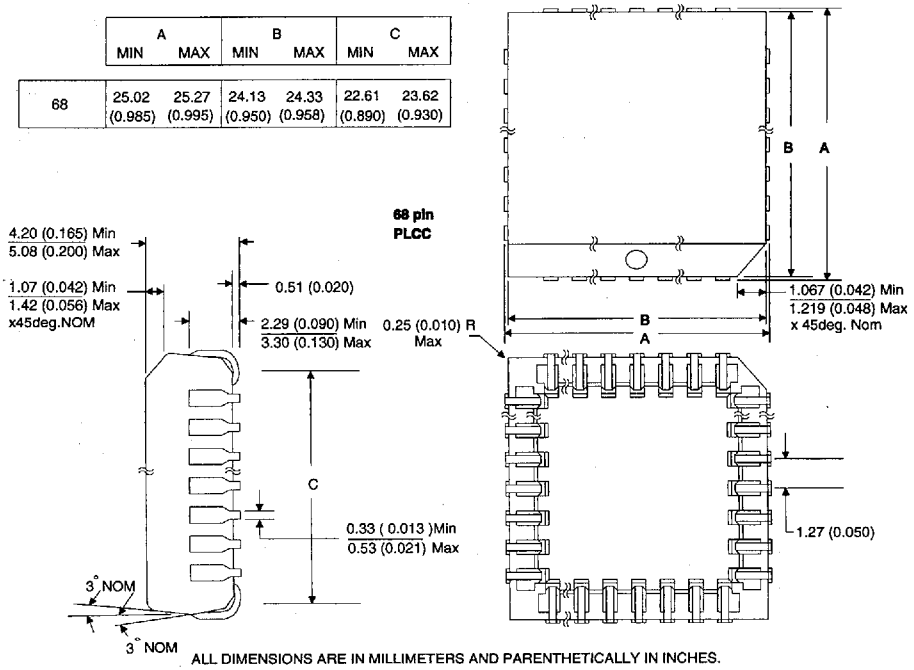
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	see table above			
B	1.27	BSC	0.050	BSC
C	7°	NOM	7°	NOM
D	0.127	0.330	0.005	0.013
E	2.41	2.67	0.095	0.105
F	45°	NOM	45°	NOM
G	7°	NOM	7°	NOM
H	0.203	0.381	0.008	0.015
I	2°	8°	2°	8°
J	7.42	7.59	0.292	0.298
K	8.76	9.02	0.345	0.355
L	10.16	10.67	0.400	0.420
M	0.33	0.51	0.013	0.020

NO. OF TERMINAL	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
28	12.32 (0.485)	12.57 (0.495)	11.43 (0.450)	11.58 (0.456)	9.91 (0.390)	10.92 (0.430)
44	17.40 (0.685)	17.65 (0.695)	16.51 (0.650)	16.66 (0.656)	14.98 (0.590)	16.00 (0.630)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

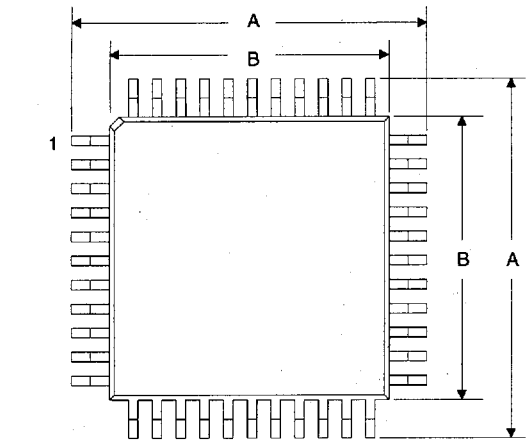
	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
68	25.02 (0.985)	25.27 (0.995)	24.13 (0.950)	24.33 (0.958)	22.61 (0.890)	23.62 (0.930)



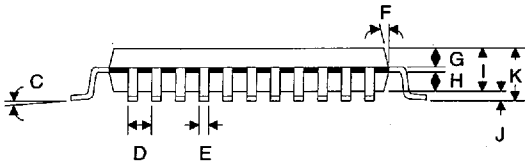
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

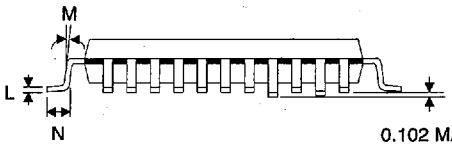
11

44 PIN QUAD FLATPACK

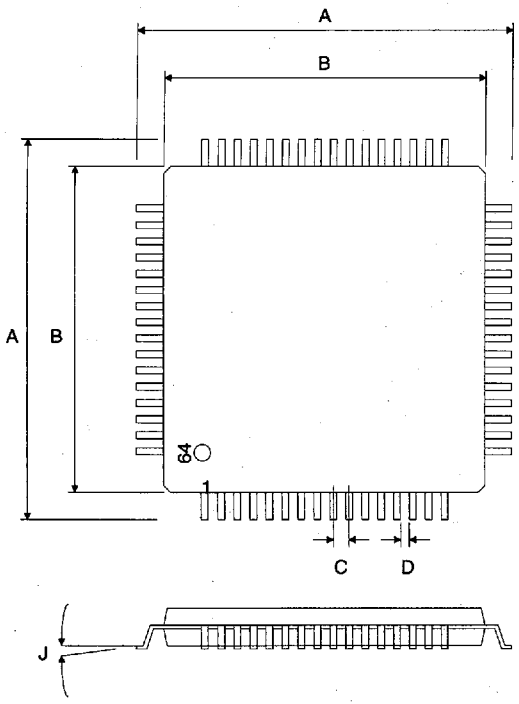


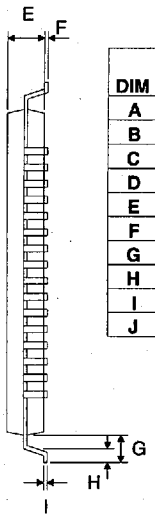
	44 Pin TQFP 1.4 mm Package Thickness			
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	11.75	12.25	0.463	0.482
B	9.90	10.10	0.390	0.398
C	0°	7°	0°	7°
D	0.80 BSC		0.031 BSC	
E	0.35 BSC		0.014 BSC	
F		12°		12°
G	0.54	0.74	0.021	0.029
H	0.54	0.74	0.021	0.029
I	1.35	1.50	0.053	0.059
J	0.05		0.002	
K		1.60		0.063
L		0.17		0.007
M	2°	10°	2°	10°
N	0.35	0.65	0.014	0.026





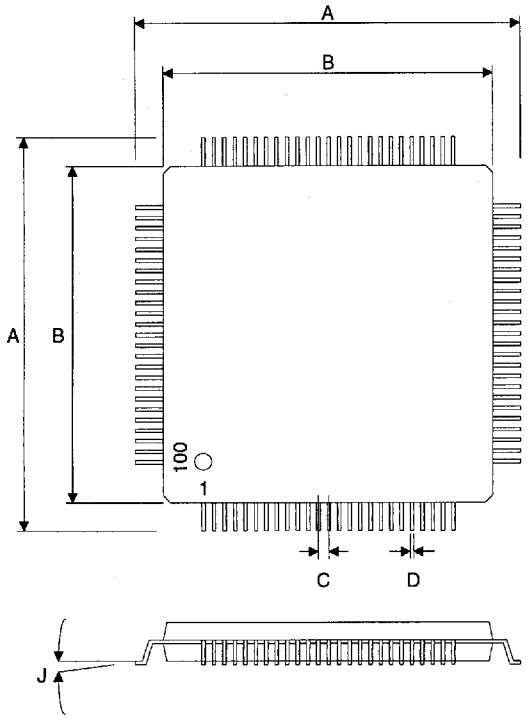
0.102 MAX
Lead Coplanarity

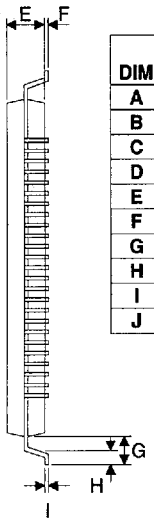




64 Pin TQFP

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.00 BSC		0.472 BSC	
B	10.00 BSC		0.393 BSC	
C	0.50 BSC		0.020 BSC	
D	0.14	0.30	0.005	0.012
E	0.95	1.12	0.037	0.044
F	0.05	0.15	0.002	0.006
G	1.00 BSC		0.039 BSC	
H	0.45	0.75	0.018	0.030
I	0.09	0.18	0.003	0.007
J	0°	7°	0°	7°





100-pin TQFP

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.75	16.25	0.620	0.640
B	13.90	14.10	0.547	0.555
C	0.50 BSC		0.020 BSC	
D	0.10	0.20	0.004	0.012
E	1.25	1.55	0.049	0.061
F	0.00	0.20	0.000	0.008
G	1.00 BSC		0.039 BSC	
H	0.35	0.65	0.014	0.026
I	0.077	0.177	0.003	0.007
J	0°	10°	0°	10°

11