

September 1996

Fast CMOS 3.3V 16-Bit Bidirectional Transceiver

Features

- Advanced 0.6 micron CMOS Technology
- Compatible with LCX™ and LVT™ Families of Products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input Can Be 3V or 5V
 - Output Can Be 3V or Connected to 5V Bus
- Advanced Low Power CMOS Operation
- Excellent Output Drive Capability:
 - Balanced Drives (24mA Sink and Source)
- Pin Compatible with Industry Standard Double-Density Pinouts
- Low Ground Bounce Outputs
- Hysteresis on All Inputs
- Multiple Center Pin and Distributed V_{CC}/GND Pins Minimize Switching Noise

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT16245AMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74LPT16245ASM	-40 to 85	48 Ld SSOP	M48.300-P
CD74LPT16245CMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74LPT16245CSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74LPT16245MT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74LPT16245SM	-40 to 85	48 Ld SSOP	M48.300-P

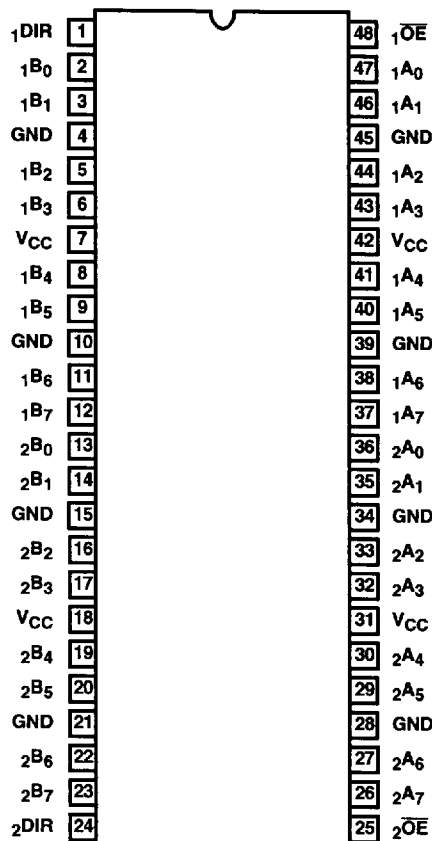
Description

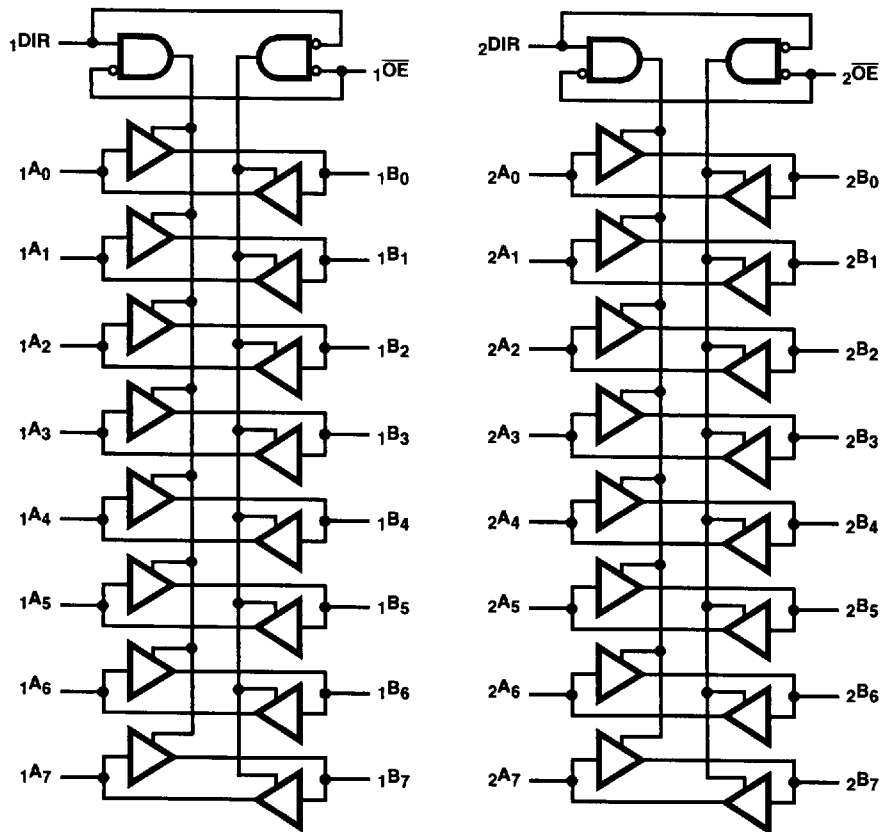
The CD74LPT16245 is a 16-bit bidirectional transceiver designed for asynchronous two-way communication between data buses. The direction control input pin (χ DIR) determines the direction of data flow through the bidirectional transceiver. The Direction and Output Enable controls are designed to operate this device as either two independent 8-bit transceivers or one 16-bit transceiver. The output enable (\overline{OE}) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

The CD74LPT16245 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Pinout

CD74LPT16245
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram

TRUTH TABLE (NOTE 1)

INPUTS		OUTPUTS
\overline{xOE}	\overline{xDIR}	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

NOTE:

1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
\overline{xOE}	Three-State Output Enable Inputs (Active LOW)
\overline{xDIR}	Direction Control Input
\overline{xAx}	Side A Inputs or Three-State Outputs
\overline{xBx}	Side B Inputs or Three-State Outputs
GND	Ground
V_{CC}	Power

CD74LPT16245

Absolute Maximum Ratings

DC Input Voltage -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only. -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only. -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
TSSOP Package 94
SSOP Package 76
Maximum Junction Temperature 150°C
Maximum Storage Temperature Range -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETERS	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T _A = -40°C to 85°C, V _{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V _{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V _{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V _{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I _{IH}	V _{CC} = Max	V _{IN} = 5.5V	-	-	±1	μA
Input HIGH Current (I/O Pins)	I _{IH}	V _{CC} = Max	V _{IN} = V _{CC}	-	-	±1	μA
Input LOW Current (Input Pins)	I _{IL}	V _{CC} = Max	V _{IN} = GND	-	-	±1	μA
Input LOW Current (I/O Pins)	I _{IL}	V _{CC} = Max	V _{IN} = GND	-	-	±1	μA
High Impedance Output Current (Three-State Output Pins)	I _{OZH}	V _{CC} = Max	V _{OUT} = 5.5V	-	-	±1	μA
	I _{OZL}	V _{CC} = Max	V _{OUT} = GND	-	-	±1	μA
Clamp Diode Voltage	V _{IK}	V _{CC} = Min, I _{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I _{ODH}	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V (Note 5)		-36	-60	-110	mA
Output LOW Current	I _{ODL}	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V (Note 5)		50	90	200	mA
Output HIGH Voltage	V _{OH}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -0.1mA	V _{CC} - 0.2	-	-	V
			I _{OH} = -3mA	2.4	3.0	-	V
		V _{CC} = 3.0V, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -8mA	2.4 (Note 7)	3.0	-	V
			I _{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 0.1mA	-	-	0.2	V
			I _{OL} = 16mA	-	0.2	0.4	V
			I _{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETERS	SYMBOL	(NOTE 3) TEST CONDITIONS	MIN	(NOTE 4) TYP	MAX	UNITS
Short Circuit Current (Note 6)	I_{OS}	$V_{CC} = \text{Max (Note 5), } V_{OUT} = \text{GND}$	-60	-85	-240	mA
Power Down Disable	I_{OFF}	$V_{CC} = 0V, V_{IN} \text{ or } V_{OUT} \leq 4.5V$	-	-	± 100	μA
Input Hysteresis	V_H		-	150	-	mV
CAPACITANCE $T_A = 25^\circ C, f = 1\text{MHz}$						
Input Capacitance (Note 8)	C_{IN}	$V_{IN} = 0V$	-	4.5	6	pF
Output Capacitance (Note 8)	C_{OUT}	$V_{OUT} = 0V$	-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS						
Quiescent Power Supply Current	I_{CC}	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$	-	0.1	10	μA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	$V_{CC} = \text{Max}$ $V_{IN} = V_{CC} - 0.6V$ (Note 9)	-	2.0	30	μA
Dynamic Power Supply Current (Note 10)	I_{CCD}	$V_{CC} = \text{Max, Outputs Open}$ $\overline{xOE} = \overline{xDIR} = \text{GND}$ One Bit Toggling 50% Duty Cycle	-	50	75	$\mu A/\text{MHz}$
Total Power Supply Current (Note 12)	I_C	$V_{CC} = \text{Max, Outputs Open}$ $f_1 = 10\text{MHz, 50\% Duty Cycle}$ $\overline{xOE} = \overline{xDIR} = \text{GND}$ One Bit Toggling	-	0.5	0.8	mA
		$V_{CC} = \text{Max, Outputs Open}$ $f_1 = 2.5\text{MHz, 50\% Duty Cycle}$ $\overline{xOE} = \overline{xDIR} = \text{GND}$ 16 Bits Toggling	-	2.0	3.3 (Note 11)	mA

CD74LPT16245

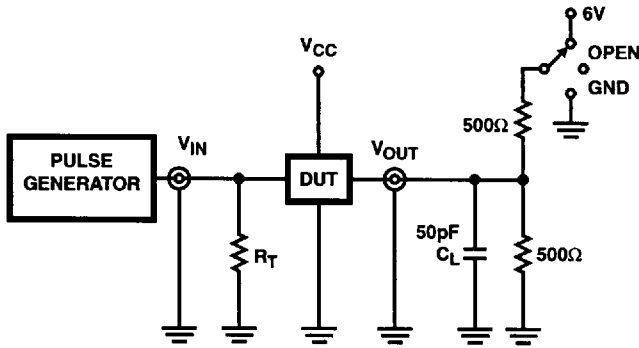
Switching Specifications Over Operating Range (Note 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74LPT16245		CD74LPT16245A		CD74LPT16245C		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay A to B, B to A	t_{PLH} , t_{PHL}	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	5.2	1.5	4.6	1.5	4.1	ns
Output Enable Time $\chi\overline{OE}$ to A or B	t_{PZH} , t_{PZL}		1.5	7.2	1.5	6.2	1.5	5.8	ns
Output Disable Time (Note 16) $\chi\overline{OE}$ to A or B	t_{PHZ} , t_{PLZ}		1.5	7.2	1.5	5.0	1.5	4.8	ns
Output Enable Time $\chi\overline{DIR}$ to A or B	t_{PZH} , t_{PZL}		1.5	7.2	1.5	6.2	1.5	5.8	ns
Output Disable Time $\chi\overline{DIR}$ to A or B (Note 16)	t_{PHZ} , t_{PLZ}		1.5	7.2	1.5	5.0	1.5	4.8	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	ns

NOTES:

- For conditions shown as Max or Min, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3\text{V}$, 25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- $V_{OH} = V_{CC} - 0.6\text{V}$ at rated current.
- This parameter is determined by device characterization but is not production tested.
- Per TTL driven input; all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
 I_{CC} = Quiescent Current (I_{CCL} , I_{CCH} and I_{CCZ})
 ΔI_{CC} = Power Supply Current for a TTL High Input
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 N_{CP} = Number of Clock Inputs at f_{CP}
 f_I = Input Frequency
 N_I = Number of Inputs at f_I
 All currents are in milliamps and all frequencies are in megahertz.
- Propagation Delays and Enable/Disable times are with $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, normal range. For $V_{CC} = 2.7\text{V}$, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
- See test circuit and wave forms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not production tested.
- Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



NOTE:

18. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_{\text{OUT}} \leq 50\Omega$;
 $t_f, t_r \leq 2.5\text{ns}$.

FIGURE 1. TEST CIRCUIT

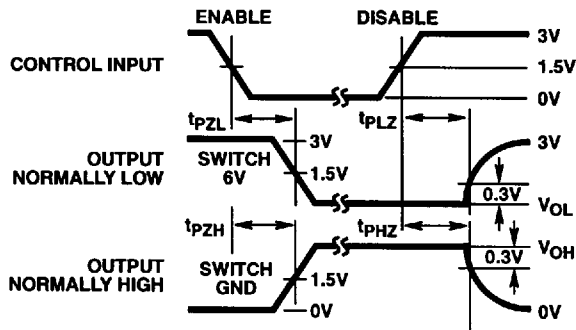


FIGURE 2. ENABLE AND DISABLE TIMING

SWITCH POSITION	
TEST	SWITCH
$t_{\text{PLZ}}, t_{\text{PZL}}, \text{Open Drain}$	6V
$t_{\text{PHZ}}, t_{\text{PZH}}$	GND
$t_{\text{PLH}}, t_{\text{PHL}}$	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

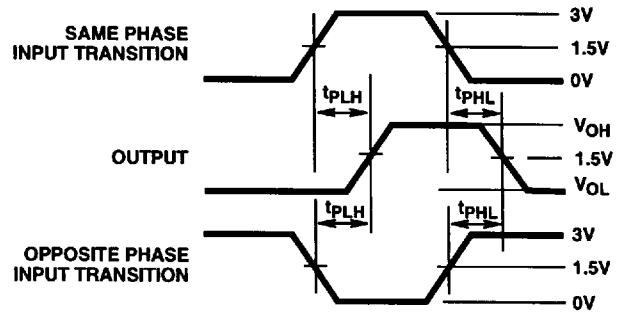
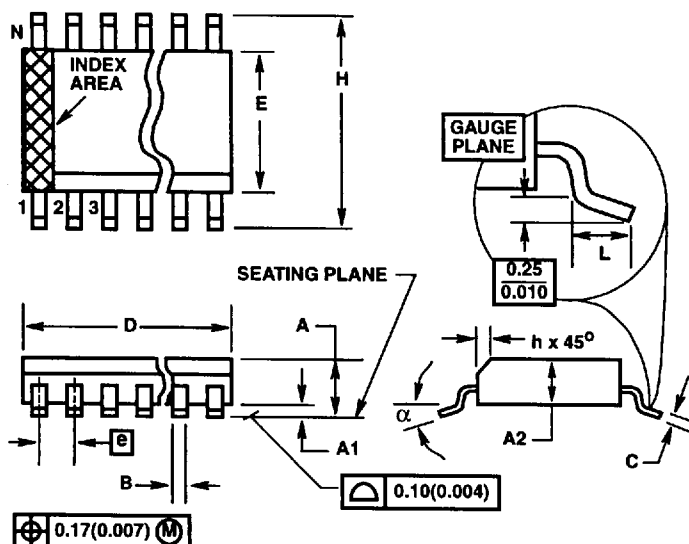


FIGURE 3. PROPAGATION DELAY

Shrink Small Outline Plastic Packages (SSOP)**NOTES:**

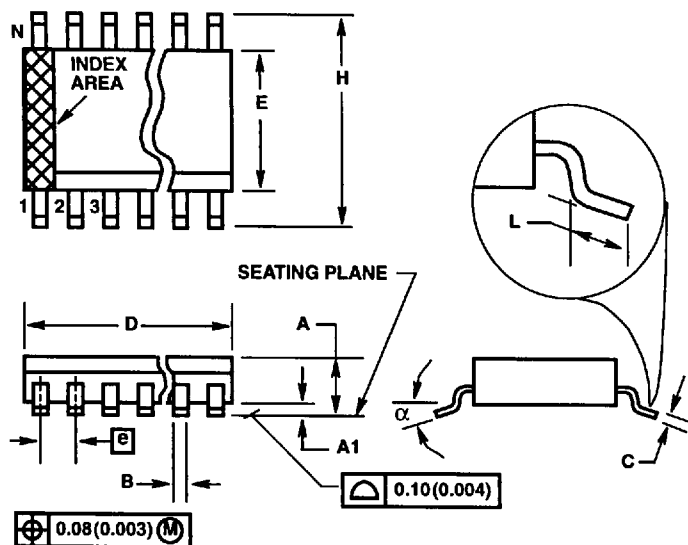
1. These package dimensions are within allowable dimensions of JEDEC MO-118-AA, Issue B.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
3. Dimension "E" does not include interlead flash or protrusions.
4. "L" is the length of terminal for soldering to a substrate.
5. "N" is the number of terminal positions.
6. Terminal numbers are shown for reference only.
7. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

M48.300-P**48 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.096	0.108	2.44	2.74	-
A1	0.008	0.016	0.20	0.41	-
A2	0.088	0.092	2.24	2.34	-
B	0.008	0.0135	0.20	0.34	-
C	0.005	0.010	0.13	0.25	-
D	0.620	0.630	15.75	16.00	2
E	0.291	0.299	7.39	7.59	3
e	0.025 BSC		0.635 BSC		-
H	0.395	0.415	10.03	10.54	-
h	0.015	0.025	0.381	0.635	-
L	0.020	0.040	0.51	1.01	4
N	48		48		5
α	0°	8°	0°	8°	-

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Thin Shrink Small Outline Plastic Packages (TSSOP)



M48.240-P

48 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.041	0.047	1.05	1.20	-
A1	0.002	0.006	0.05	0.15	-
B	0.007	0.010	0.178	0.254	-
C	0.004	0.008	0.102	0.203	-
D	0.488	0.496	12.40	12.59	1
E	0.236	0.244	6.00	6.19	2
e	0.0197 BSC		0.50 BSC		-
H	0.307	0.330	7.80	8.38	-
L	0.020	0.030	0.51	0.76	3
N	48		48		4
α	0°	8°	0°	8°	-

Rev. 0 6/96

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

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