CALMOS™

CA424

DC - DC CONVERTER

- Low power
- High efficiency
- Few external components
- Input voltage as low as 0.9V
- Standby supply current less than 400μA
- Output switch transistor current to 250mA
- Output current limit protection at 600mA
- Low battery monitor/indicator

The CA424 is a low power, high efficiency DC-DC Converter. It can operate from single battery cell voltages as low as 0.9 volts. Only five external components are required.

The I.C. consists of a temperature compensated voltage reference, an oscillator, a duty cycle modulation circuit, a low saturation voltage O/P transistor switch and a dual comparator. Output voltages of 3V or 5.5V are selectable by voltage level on the VCCSEL pin. One comparator monitors battery voltage and the other can be used to sense the output of a photo-transistor circuit.

It converts single battery voltage (0.9V - 1.7) to either 3V or 5.5V. As well, other O/P voltages can be available.

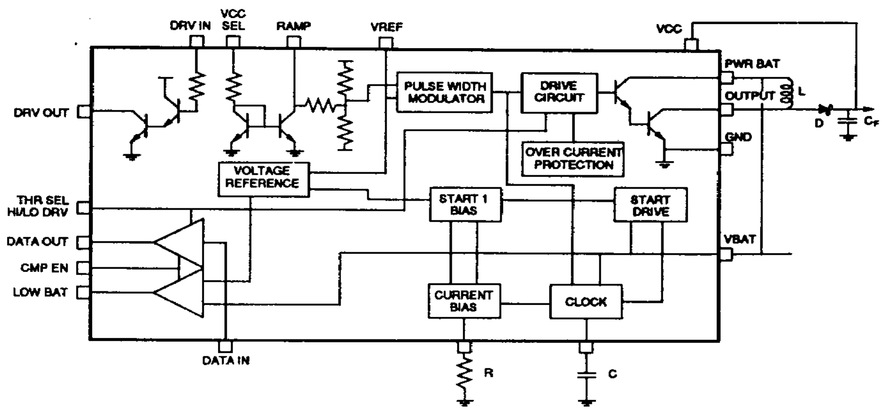

Figure 1 : CA424 BLOCK DIAGRAM

CA424 M-16 PACKAGE

1	VCC
2	VCCSEL
3	VBAT
4	PWR BAT
5	OUTPUT
6	GND
7	DRV OUT
8	DRV IN
9	THR SEL H/L DRV
10	DATA IN
11	CMP EN
12	DATA OUT
13	LOW BAT
14	C
15	R
16	RAMP

CA424 M-8 PACKAGE

1	VCC
2	PWR BAT
3	OUTPUT
4	GND
5	THR SEL H/L DRV
6	LOW BAT
7	C
8	R

This package option gives a *non-selectable* output of 3 V.

CA424 M-8 'S' PACKAGE

1	VCC
2	VBAT
3	OUTPUT
4	GND
5	LOW BAT
6	C
7	R
8	RAMP

The 'S' package option provides a *selectable* output of 3 or 5.5V, as set by the value of RAMP.
RAMP *open-circuit* = 3.0V.
RAMP *@ gnd* = 5.5V.

Figure 2 : PIN CONFIGURATIONS

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Table 1 : ELECTRICAL CHARACTERISTICS

(V_{BAT} = 0.9V to 1.7V; T_A = -20°C to +70°C; VCC = 3V; CMP EN High; VCCSEL, THR SEL Low; R = 300K; C = 150pF)

Parameter		Conditions	Min	Typ	Max	Units
Supply Currents Output Stage OFF	V_{BAT}			70	120	µA
	V_{CC}			45	75	µA
	PWR BAT	PWR BAT = 3.3V			10	µA
Supply Currents Output stage ON	V_{BAT}			70	120	µA
	V_{CC}			350	550	µA
	PWR BAT	I_{OUT} = 100mA		1	4	mA
		I_{OUT} = 250mA, PWR BAT ≥ 1.1V		3	12	mA
$V_{OUTPUT LOW}$		I_{OUT} = 100mA			0.3	V
		I_{OUT} = 250mA, PWR BAT ≥ 1.1V			0.5	V
Voltage Reference, VREF			1.19		1.25	V
V_{CC} Voltage Accuracy	3.0V		2.7	3.0	3.3	V
	5.5V		5.0	5.5	6.0	V
Auxillary Driver	V_{OL}	I_{OL} = 10mA, V_{IH} = 3V			0.4	V
	V_{OL}	I_{OL} = 25mA, V_{IH} = 3V, V_{BAT} ≥ 1.1V			0.4	V
	I_{OH}	V_{OH} = 6V, V_{IL} = 0.3V			10	µA
Control Inputs: VCCSEL, DRV IN, THR SEL, CMP EN	V_{IL}				0.3	V
	V_{IH}		V_{CC} - 0.5			V
	I_{IL}	V_{IL} = 0V	-50			µA
	I_{IH}	V_{IH} = 3V			60	µA
Clock Frequency			20.5	23.5	26.5	KHz
Battery Monitor	Threshold, +70°C	CMP EN = 0V	0.91	0.95	0.99	V
	Threshold, +20°C		0.98	1.02	1.06	V
	Threshold, -20°C		1.00	1.04	1.08	V
Photo Comparator: HighLevel Threshold		CMP EN = 0V, THR SEL = 3V				
	V_{OH}	I_{IN} > 24µA, I_{OH} = -5µA	2.4			V
	V_{OL}	I_{IN} < 5µA, I_{OL} = 5µA			0.6	V
Photo Comparator: LowLevel Threshold		CMP EN = THR SEL = OV[1]				
	V_{OH}	I_{IN} > 1.5µA, I_{OH} = -5µA	2.4			V
	V_{OL}	I_{IN} < 0.5µA, I_{OL} = 5µA			0.6	V
Comparator Delay		DATA OUT CL = 10pF		10		µs
RAMP Time		VCCSEL = VCC, C_{RAMP} = 0.1µF				
		3.3V to 5.0 V	30		70	ms

Notes: 1. Average switch threshold is 0.7V. Low threshold set by external 680K resistor form DATA IN pin to Ground.

2. Operating temperature range is: –20° to +70°C

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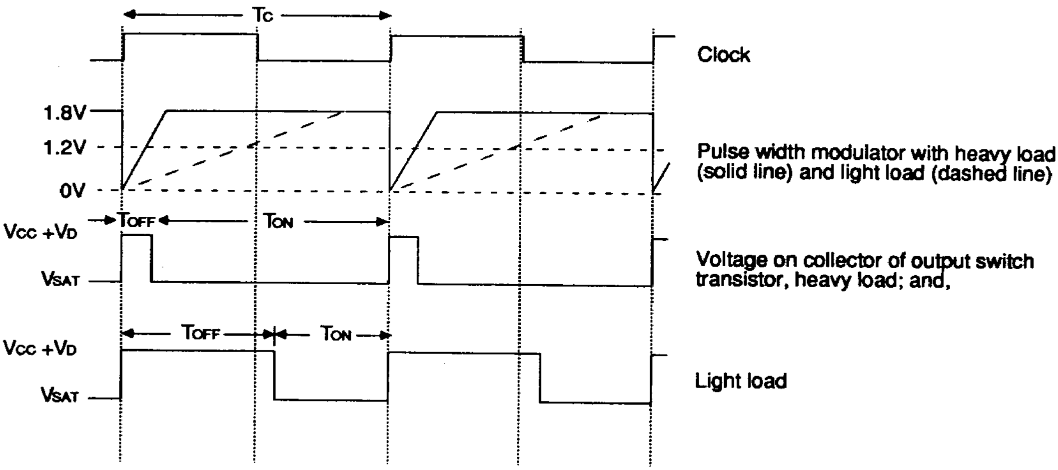

Figure 3 : CA424 TIMING DIAGRAM

Table 2 : ABSOLUTE MAXIMUM RATINGS

Battery Voltage	6V
Supply Voltage (VCC)	6V
Storage Temperature Range	–65° to +150°C

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FUNCTIONAL DESCRIPTION

The CA424 is a pulse width modulation switching regulator. When connected with an inductor, a Schottky diode and a capacitor, it can generate a nominal 3V supply from a single cell battery source (0.9V to 1.7V).

Pulse width modulation is accomplished by comparing the pulse width modulator output sawtooth waveform and the bandgap reference voltage. When the sawtooth voltage is above the bandgap voltage, the output switch is on; otherwise it is off. The capacitor is discharged at the beginning of every clock cycle, and is charged up by a charging current generated by a transconductance amplifier. The charging current is proportional to the difference between the bandgap voltage and the attenuated output voltage. A lower output voltage corresponds to a higher charging current, which in turn gives a longer on time. More power is delivered to the load and the output voltage is increased.

The output switch is designed with a controlled base drive. The drive current from the PWR BAT pin is limited to Ioutput/50 (typ.), or Ioutput/25 (max.). If Ioutput exceeds 600mA (typ.), the current limit circuit will shut the output stage off for the remainder of the clock cycle.

A high voltage level on the HI/LO DRV pin boosts the available OUTPUT current level by a factor of ≈ 3 times.

The 3V rail can be raised to 5.5V by asserting the VCCSEL pin. The rate of change from 3V to 5.5V is set up by an external capacitor, which is connected across the RAMP pin and ground.

The switching frequency is controlled by an internal clock. Its frequency is set by an external resistor and an external capacitor. The nominal switching frequency is 25KHz (R=300K, C=150pF). The bias voltage of the R pin is 0.7V.

The CA424 contains two comparators: the battery comparator and the photo comparator. To save power, both comparators are disabled unless the CMP EN pin is grounded.

The Battery Monitor Comparator output has a *low* level when the battery drops below an internal 1.02V reference.

The photo comparator is designed to operate with an external photo-transistor and an external resistor in two different modes. One mode is using an external resistor to set up a very low current threshold which is approximately 1μA. That threshold can be used to indicate high or low ambient illumination. The other mode with approximately 10μA threshold, which is set up by an internal resistor, can be used to read optically coupled date from the phototransistor.

The CA424 also contains an auxiliary open collector driver. When the DRV IN pin is 5V, the driver will sink 25mA at the DRV OUT pin.

An internal 1.22V bandgap circuit provides reference voltage for the regulators as well as the battery monitor comparator.

Table 3 : FUNCTION TABLE

VCCSEL	H	V_{cc} = 5.5V
	L	V_{cc} = 3.0V
CMP EN	H	Comparators disabled
	L	Comparators enabled
DRV IN	H	Auxiliary driver ON
	L	Auxiliary driver OFF
THR SEL - HI/LO DRV	H	Output current high - Photo current high threshold
	L	Output current low - Photo current low threshold
DATA IN	H	DATA OUT high
	L	DATA OUT low
LOW BAT	H	Battery okay
	L	Battery low

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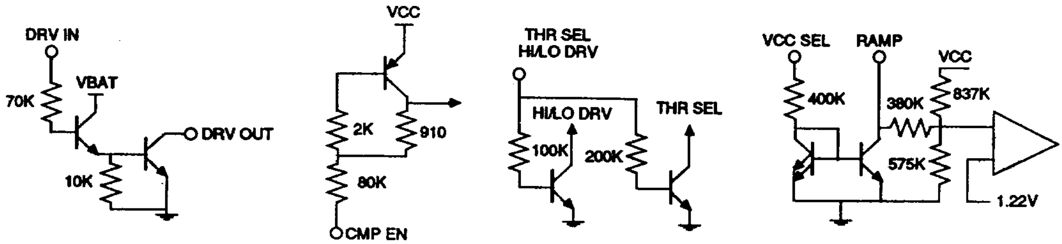
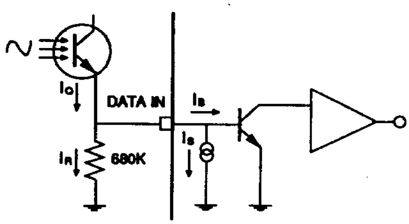


Figure 4 : INTERFACE SCHEMATICS (simplified)



Threshold Is = 5µA @ VBE = 500mV, 25°C

1. Receive optical data: Is = 10µA
   IR = 680mV/680K = 1 µA
   Io = 12µA
2. Detect low ambient light: Is = 0(current source not connected)
   Io = 2µA

Figure 5 : PHOTO - TRANSISTOR INTERFACE

Table 4 : ELECTRICAL CHARACTERISTICS (CA424 connected as in Figure 1, with component values below):
L = 300µH (16 turns on TDK H5B2T4-8-4 core), D = IOR10JQ, C_F = 47µF, R = 300K, C = 150pF, V_{BAT} = 1.3V, CMP EN = V_{CC}

Parameter		Conditions	Min	Typ	Max	Unit
Supply Currents, V_{CC} = 3V		VCCSEL = 0V				
	VBAT	I load = 0		320		µA
	VBAT	I load = 15mA		50		mA
Supply Currents, V_{CC} = 5.5V		VCCSEL = V_{CC}				
	VBAT	I load = 0		800		µA
	VBAT	I load = 10mA		62		mA
Load Regulation	V_{CC} = 3.0V	I load = 0 to 15mA		0.1		V
	V_{CC} = 5.5V	I load = 0 to 10mA		0.2		V

APPLICATION NOTES

Calculating the Power Output

The output power must be transferred from the CA424 through the inductor to the load. During the *on* time of the output switch transistor, the current in the inductor increases lineally from zero to a maximum value of:

$$I_P = \frac{(VBAT - V_{SAT})}{L} \times T_{on} \quad [1]$$

where

V_{SAT} = saturation voltage of output switch transistor, 0.3V
I_P = peak (maximum) current through the inductor.

The input power is the energy transferred to the inductor per cycle divided by the clock period:

$$P_{IN} = \frac{\left(\frac{1}{2} L I_P^2\right)}{T_C} = \frac{(VBAT - V_{SAT})^2}{2L} \times \frac{T_{on}^2}{T_C} \quad [2]$$

The output power is:

$$P_{OUT} = (VCC + V_D)(I_L + I_S) \quad [3]$$

where

I_L = load current;
I_S = CA424 VCC supply current = 0.1 mA;
V_D = Schottky diode forward voltage = 0.5 V.

For a lossless inductor

$$P_{IN} = P_{OUT}$$

Efficiency

$$\text{Efficiency} = \frac{VCC}{VBAT} \times \frac{I_L}{I_{BATTERY}}$$

Efficiencies for the circuit connections described in this Datasheet are typically 65 - 80%.

Example

Calculate an inductor value for

VCC = 5.5V
I_L = 10mA
VBAT = 1.3V
Tc = 40 µsec (F_{CLOCK} = 25KHz)

Choose Ton (max) = 36µsec

Set [2] = [3]:

$$\frac{(1.3-0.3)^2}{2L} \times \frac{(36\times10^{-6})^2}{40\times10^{-6}} = (5.5+0.5)(10+0.1)\times10^{-3}$$

ie: L = 267µH

Caution:

It is easy to underestimate the peak value of current through the inductor. The ratio of load current to peak inductor current, assuming an ideal diode and inductor is:

$$I_L = \frac{I_P}{2} \times \frac{T_{on}}{T_C} \times \frac{VBAT}{VCC}$$

eg: if $I_L = \frac{I_P}{2} \times \frac{3}{5} \times \frac{0.9V}{5.5V}$

then $I_P = 20 I_L$

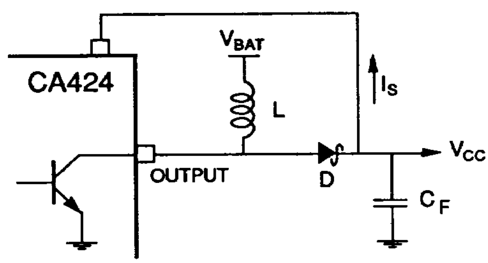


Figure 6 : APPLICATION DIAGRAM

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