BiCMOS PLL Universal Clock Distribution Chip

Features

- Generate twelve outputs from the reference input clock frequency, with near zero skew between the input and output clocks.
- Multiple selectable phase/frequency relations for the clock outputs.
- Compensate for clock skew down to 2.5 ns increments.
- Controlled edge rate TTL outputs with less than ±250 ps pin to pin skew.
- Maximum phase error ± 250 ps.
- Proven 0.8-micron BiCMOS technology.
- Single +5V power supply operation
- 44 pin PLCC package.

Applications

- High-speed Microprocessor Systems
- Board-to-Board Clock Synchronization
- Trace Delay/Loading Compensation
- Backplane Clock Deskew and Distribution
- High performance ASIC Systems

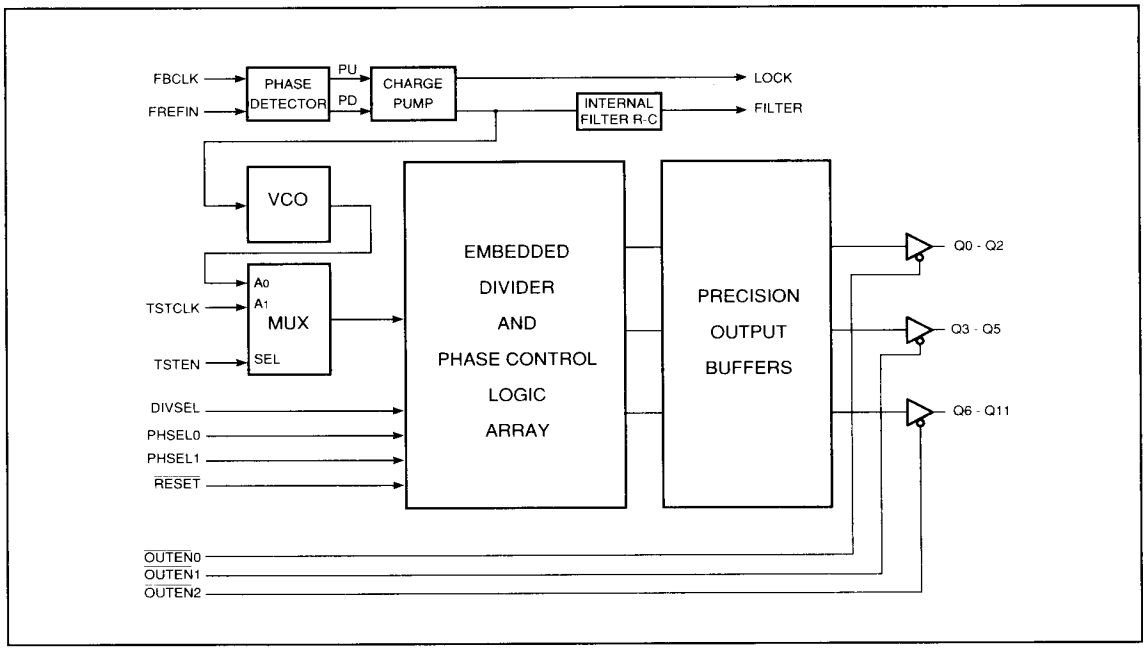
General Description

The PI6B2407 PLL (Phase-locked loop) universal clock distribution chip in BiCMOS technology allows the user to generate twelve TTL outputs with multiple clock phases programmed by two input pins PHSEL0 and PHSEL1. A high frequency on chip VCO and a divider control pin allow the clock outputs with the selectable frequency inputs.

The Test Enable input allows VCO bypass for open loop operation.

By using the programmable divider and the phase selector the user can generate output clocks at same or twice the reference clock input frequency. The outputs can be phase-adjusted in increments as small as 2.5 ns to tailor the clocks to exact system requirements. Multiple output phase relationships are available from the different configuration of the divider, the phase selectors and the selected output for FBCLK.

Block Diagram



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Functional Description

The PI6B2407 clock generator provides multiple outputs synchronized both in frequency and phase to a periodic clock signal input that is synthesized on the chip. An external feedback of a PLL and two select pins allow the user to phase-adjust the twelve outputs relative to the input clock.

The phase selection inputs PHSEL0 and PHSEL1 allow the user to select different phase relations among the 12 TTL clock outputs as shown in Table 1a and 1b.

Different combinations of output frequencies and clock phase relationships are available on a semi-custom design base. Please contact factory for special semi-custom designs.

Example:

In a typical system, designers may need several low skew outputs, early clocks, one late clock, clocks at half the input clock frequency, and at twice the input clock frequency. These different systems requirements can be satisfied by choosing different phase input and output feedback combinations as shown in Table 1.

Table 1a. Output selection matrix (Divsel = 0, Div 8)

Conf.	Sel. Pins		Output Fed	Outputs			Input Freq. (MHz)		Output Freq. (MHz)	
No.	PHSEL1	PHSEL0	to FBCLK	Q0,Q1,Q2	Q3,Q4,Q5	Q6-Q11	Min	Max	Min	Max[7]
1	0	0	Q0-Q2	0	0	0	24	50	24	50
2			Q3-Q5	0	0	0	24	50	24	50
3			Q6-Q11	0	0	0	24	50	24	50
4	0	1	Q0-Q2	0	1t	2(0)	24	50	24	100
5			Q3-Q5	–1t	0	2(–1t)	24	50	24	100
6			Q6-Q11	0/2	2t/2	0	50	100	25	100
7	1	0	Q0-Q2	0	2t	2(0)	24	50	24	100
8			Q3–Q5	–2t	0	2(–2t)	24	50	24	100
9			Q6-Q11	0/2	4t/2	0	50	100	25	100
10	1	1	Q0-Q2	0	2(0)	2(0)	24	50	24	100
11			Q3-Q11	0/2	0	0	50	100	25	100

Table 1b. Output selection matrix (Divsel = 1, Div 16)

Conf.	Sel. Pins		Output Fed	Outputs			Input Freq. (MHz)		Output Freq. (MHz)	
No.	PHSEL1	PHSEL0	to FBCLK	Q0,Q1,Q2	Q3,Q4,Q5	Q6-Q11	Min	Max	Min	Max[7]
1	0	0	Q0-Q2	0	2t	0	14	33	14	33
2			Q3-Q5	–2t	0	–2t	14	33	14	33
3			Q6-Q11	0	2t	0	14	33	14	33
4	0	1	Q0-Q2	0	2t	2(0)	14	30	14	60
5			Q3-Q5	–2t	0	2(–2t)	14	30	14	60
6			Q6-Q11	0/2	4t/2	0	24	50	12	50
7	1	0	Q0-Q2	0	3t	2(0)	14	30	14	60
8			Q3–Q5	–3t	0	2(–3t)	14	30	14	60
9			Q6-Q11	0/2	6t/2	0	24	50	12	50
10	1	1	Q0-Q2	0	2(0)	2(0)	14	30	14	60
11			Q3-Q11	0/2	0	0	24	50	12	50

Notes:
1. "0" implies the output is aligned with FREFIN.
2. "t" implies the output lags FREFIN by a minimum phase delay.
3. "-t" implies the output leads FREFIN by a minimum phase delay.
4. "2( )" implies the output is at twice the frequency of FREFIN.
5. "/2" implies the output is at half the frequency of FREFIN.
6. See Table 2b for Phase Shift Increments. 6, 9, and 11 in Table 1b.
7. The output frequency is further defined by the FOUT in the Table "AC Switching Characteristics Over Operating Range." For example, PI6B2407DX-66 part has the maximum output frequency of 66MHz, not 100MHz as shown in some configurations of Table 1a or 1b.

Table 2a. Example of Phase Shift Increment (t) at different input frequencies.

Phase Increment	Input Frequency				Unit
DIVSEL	25	33	40	50	MHz
0	NA	3.8	3.1	2.5	ns
1	2.5	1.9	1.6	1.2	ns

NA = Not allowed

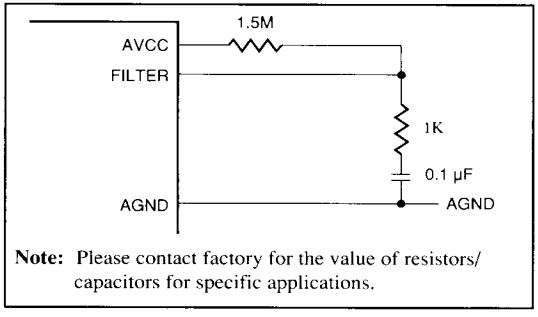
Enabling Outputs

The PI6B2407 has three output enable inputs that control which outputs toggle. When held LOW, $\overline{OUTEN0}$ enables outputs (Q0–Q2). $\overline{OUTEN1}$ enables outputs (Q3-Q5) and $\overline{OUTEN2}$ enables outputs (Q6-Q11). When an output enable pin is held high, its associated outputs are disabled and held in a high impedance state.

Filter

The FILTER output is a tap between the analog output of the phase detector and the VCO input. This pin allows a simple external filter (Figure 1) to be included in the PLL. PSC recommends the use of the filter component values shown. This filter was chosen for its ability to reduce the output jitter.

Figure 1. External PLL Filter.



Note: Please contact factory for the value of resistors/capacitors for specific applications.

Reset

When the RESET pin is pulled low, all the internal states go to zero. After the chip is reset, the PLL requires a resynchronization time before lock is again achieved.

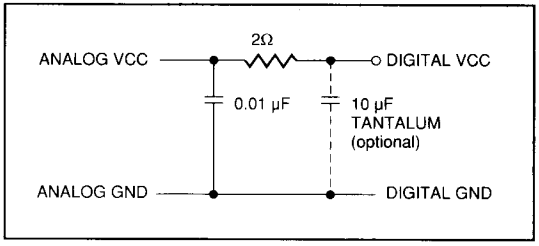
Lock Detect

A lock indicator output (LOCK) will go high when the loop is in steady-state phase and frequency lock. The lock output will go low if phase-lock is lost or when the TSTEN is high.

Power Supply Considerations

Power for the analog portion of the PI6B2407 chip must be isolated from the digital power supplies to minimize noise on the analog power supply pins. This isolation between the analog and digital power supplies can be accomplished with a simple external power supply filter (Figure 2). Ceramic chip capacitors are recommended as decoupling capacitors.

Figure 2. External Power Supply Filter.



Test Capabilities

The TSTEN input allows users to bypass the VCO and provide their own clock through the TSTCLK input. When TSTEN is High, the VCO is turned off and the TSTCLK signal drives the divider/phase adjust circuitry, directly sequencing the outputs.

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PIN DESCRIPTIONS

Input Signals

FREFIN. Frequency reference supplied by the user that, along with the output tied to the FBCLK input, determines the frequency of the Q0-Q11 outputs.

FBCLK. Feedback clock that, along with the FREFIN input, determines the frequency of the Q0-Q11 outputs. One output is selected to feed back to this input.

DIVSEL. Controls the divider circuit that follows the VCO. When DIVSEL is low, the VCO frequency is divided by eight. When DIVSEL is high, the VCO frequency is divided by 16.

PHSEL0. This input, along with PHSEL1, allows selection of the phase relationship.

PHSEL1. Along with PHSEL0, allows selection of the phase relationship.

$\overline{\text{OUTEN0}}$. Active Low. Output enable signal that controls which outputs toggle. Controls outputs Q0-Q2

$\overline{\text{OUTEN1}}$. Active Low. Output enable signal that controls which outputs toggle. Controls outputs Q3-Q5

$\overline{\text{OUTEN2}}$. Active Low. Output enable signal that controls which outputs toggle. Controls outputs Q6-Q11

$\overline{\text{RESET}}$. Active Low. Initializes internal states for test purposes.

TSTCLK. Replaces the VCO output when TSTEN is high (after first divide-by-two stage in divider phase control logic). See TSTEN.

TSTEN. Active High. Allows TSTCLK to drive the divider and phase adjust circuitry.

Output Signals

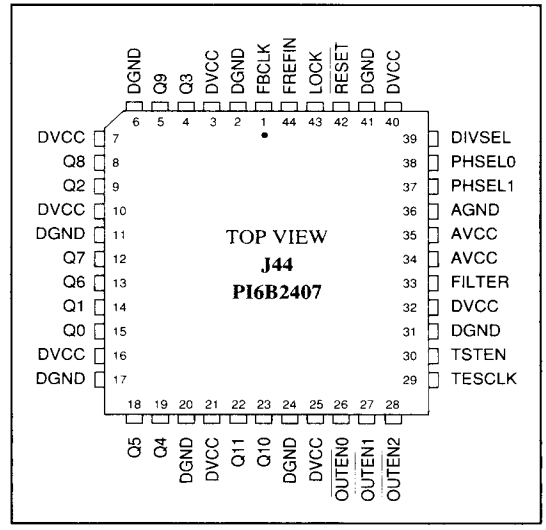
FILTER. A tap between the analog output of the phase detector and the VCO input. Allows a simple external filter (a single resistor and two capacitors) to be included in the PLL.

Q0 - Q2. 1X Clock outputs.

Q3 - Q5. 1X or 2X Clock outputs.

Q6 - Q11. 1X or 2X Clock outputs.

LOCK. Goes high when FREFIN and FBCLK are in steady-state phase and frequency lock, demonstrating that the PLL is in lock.



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to Vcc
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Operating Range, T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%)

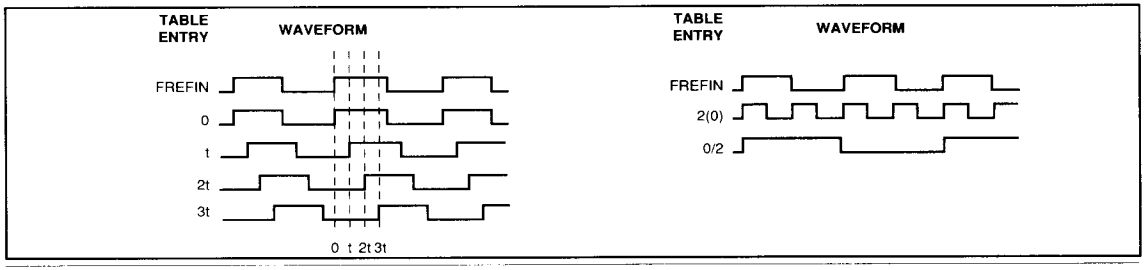
Parameters	Description	Test Conditions		Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –24 mA	2.4	3.0		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA		0.3	0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IN}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V				15	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.5 V				–15	µA
I_{OS}	Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = 0.5 V				120	mA
I_{CC}	Power Supply Current	V_{CC} = Max				160	mA

Note 1.: No more than one output should be shorted at any one time. Duration of the short circuit should not be more than one second.

Capacitance and Maximum Output Frequency

Parameters	Description	Test Conditions	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0 V, f = 1 MHz, 25°C	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V, f = 1 MHz, 25°C	8	12	pF
F_{MAX}	Max. Output Frequency	(PI6B2407DXJ-50)		50	MHz
F_{MAX}	Max. Output Frequency	(PI6B2407DXJ-60)		60	MHz
F_{MAX}	Max. Output Frequency	(PI6B2407DXJ-66)		66	MHz
F_{MAX}	Max. Output Frequency	(PI6B2407DXJ-80)		80	MHz

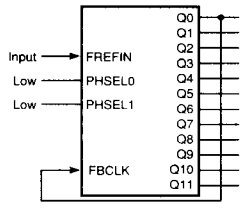
Legend

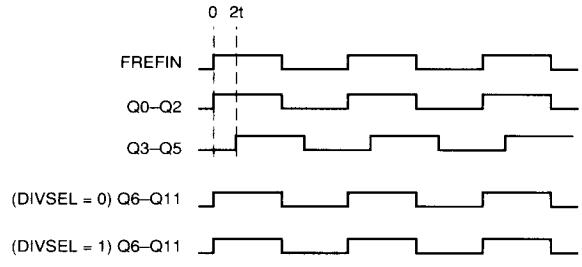


Configuration Examples

Configuration No. 1 (See Table 2a)

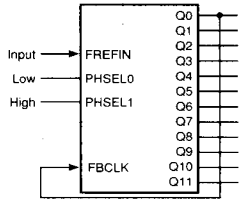
FBCLK = Q0
PHSEL1 = 0
PHSEL0 = 0

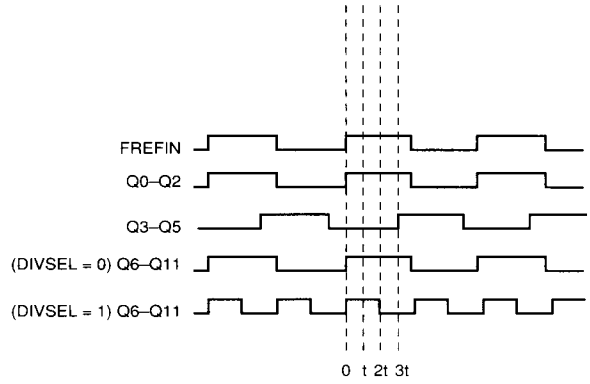




Configuration No. 7 (See Table 2b)

FBCLK = Q0
PHSEL1 = 1
PHSEL0 = 0



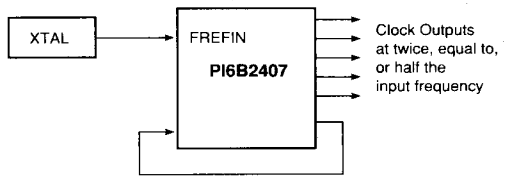


TYPICAL APPLICATIONS

The PI6B2407 chip is designed to meet a large variety of system clocking requirements. Several typical applications are provided below.

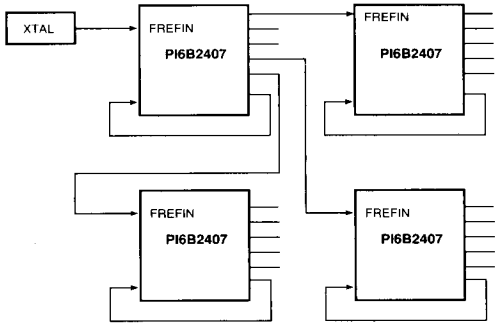
Application 1. High-Frequency, Low-Skew Clock Generation.

One of the most basic capabilities of the PI6B2407 device is generating multiple phase-aligned low-skew clocks at various multiples of the input clock frequency. For example, in a multiple-board system a half-frequency clock can be generated for use across the backplane, where it is simpler to route a low-speed signal. This signal can then be doubled on the boards and synchronization will be maintained.



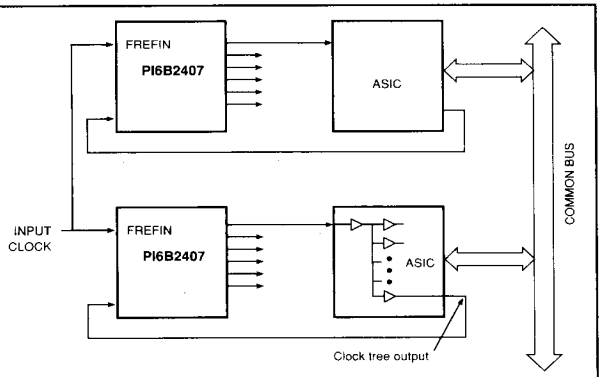
Application 2. Low-Skew Clock Distribution.

One common problem in clocking high-speed systems is that of distributing several copies of a system clock while maintaining low skew throughout the system. The PI6B2407 device guarantees low skew among all the clocks in the system, as they have effectively zero delay between their input and output signals, with an output skew of less than ±250 ps. The user can also adjust the phases of the outputs in increments as small as 1.6 ns, for load and trace length matching.



Application 3. Delay Compensation.

Since the relative edges of the PI6B2407 outputs can be precisely controlled, this chip can be used to compensate for different delays due to trace lengths or to internal chip delays, simplifying board layout and bus timing. In the example shown, the two ASICs have a difference of several nanoseconds in their propagation delays. The PI6B2407 ensures that the output signals are aligned, so that the data valid uncertainty on the common bus is minimized.



AC Switching Characteristics over Operating Range

Symbol	Description	Min	Typ	Max	Unit
F_{OUT}	Output frequency[6] (PI6B2407DX-50)	28		50	MHz
F_{OUT}	Output frequency[6] (PI6B2407DX-60)	28		60	MHz
F_{OUT}	Output frequency[6] (PI6B2407DX-66)	26		66	MHz
F_{OUT}	Output frequency[6] (PI6B2407DX-80)	26		80	MHz
t_{CP}	FREFIN period[6]	20		40	ns
t_{CPW}	FREFIN pulse width[6]	9		20	ns
t_{RI}/t_{FI}	Input rise/fall time[1]		1.8	3.0	ns
t_{RO}/t_{FO}	Output rise/fall time[1]			1.5	ns
t_{PE}	Phase error			± 250	ps
t_{JIT}	Period-to-Period Jitter[2]			75	ps
t_{SKEW}	Pin-to-Pin Skew[3]			± 250	ps
t_{CYC}	Duty-cycle variation[4]		1.0		ns
t_{SYNC}	Synchronization time[5]			500	µs
t_{OFD}	Output Disable			7	ns
t_{OFE}	Output Enable			7	ns

Notes:
1. Specified for a TTL swing from 0.8 to 2.0 volt
2. Period-to-period jitter for each individual output.
3. The output skew is measured from the middle of the output window swing from 0.8 to 2.0 volt.
4. This specification represents the deviation from 50/50 on the outputs; it is sampled periodically but is not guaranteed.
5. t_{SYNC} is the time for the PLL to synchronize; this assumes the presence of a FREFIN signal and a connection from one of the outputs to FBCLK.
6. DIV. 8, CONF. 10 is used as reference configuration.

Timing Waveforms