NEC

User's Manual

IE-703204-G1-EM1

Emulation Board

Target Devices
V850ES/SA2
V850ES/SA3

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[MEMO]

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
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INTRODUCTION

Target Readers

This manual is intended for users who design and develop application systems using the V850ES/SA2 and V850ES/SA3 microcontrollers.

Purpose

The purpose of this manual is to describe the basic specifications of the IE-703204-G1-EM1 and its proper operation.

Organization

This manual is broadly divided into the following parts.

- Outline
- Part names and functions
- Setup procedure
- Cautions
- Restrictions

How to Read This Manual

It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers. Use the IE-703204-G1-EM1 connected to the in-circuit emulator (IE-V850ES-G1). This manual describes the basic setup procedures and switch settings of the IE-703204-G1-EM1 and IE-V850ES-G1. For the part names, functions, and configuration parts of the IE-V850ES-G1, refer to the **IE-V850ES-G1 User's Manual (U16313E)** provided separately.

To learn about the basic specifications and operation
→Read this manual in the order listed in **CONTENTS**.

To learn software settings such as the operation methods, command functions, etc., of the IE-V850ES-G1 or IE-703204-G1-EM1
→Read the user's manual of the debugger (sold separately) that is used.

Conventions

Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeral representation:	Binary ··· ×××× or ××××B
	Decimal ··· ××××
	Hexadecimal ··· ××××H

Prefix representing a power of 2 (address space, memory capacity):
K (kilo): $2^{10} = 1024$
M (mega): $2^{20} = 1024^2$

Terminology

The meanings of terms used in this manual are listed below.

Target device	This is the device to be emulated.
Target system	The system (user-built system) to be debugged. This includes the target program and hardware configured by the user.
Emulation CPU	The CPU that executes the program created by the user in the emulator.

Related Documents When using this manual, refer to the following manuals.
The related documents (user's manuals) indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Development Tools (User's Manuals)

Document Name		Document Number
IE-V850ES-G1 (In-Circuit Emulator for V850ES)		U16313E
IE-703204-G1-EM1 (Emulation Board for V850ES/SA2, V850ES/SA3)		This manual
V850ES/SA2, V850ES/SA3 Hardware		U15905E
CA850 Ver.2.50 C Compiler Package	Operation	U16053E
	C Language	U16054E
	Assembly Language	U16042E
PM Plus Ver. 5.10		U16559E
ID850 Ver.2.50 Integrated Debugger	Operation Windows™ based	U16217E
SM850 Ver.2.50 System Simulator	Operation Windows based	U16218E
SM850 Ver.2.00 or Later System Simulator	External Part User Open Interface Specifications	U14873E
RX850 Ver.3.13 or Later (Real-Time OS)	Basics	U13430E
	Installation	U13410E
	Technical	U13431E
RX850 Pro Ver.3.13 (Real-Time OS)	Basics	U13773E
	Installation	U13774E
	Technical	U13772E
RD850 Ver.3.01 Task Debugger		U13737E
RD850 Pro Ver.3.01 Task Debugger		U13916E
AZ850 Ver.3.10 System Performance Analyzer		U14410E
PG-FP4 Flash Memory Programmer		U15260E

Caution The related documents listed above are subject to change without notice.
Be sure to use the latest version of each document when designing.

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LIST OF FIGURES

LIST OF TABLES

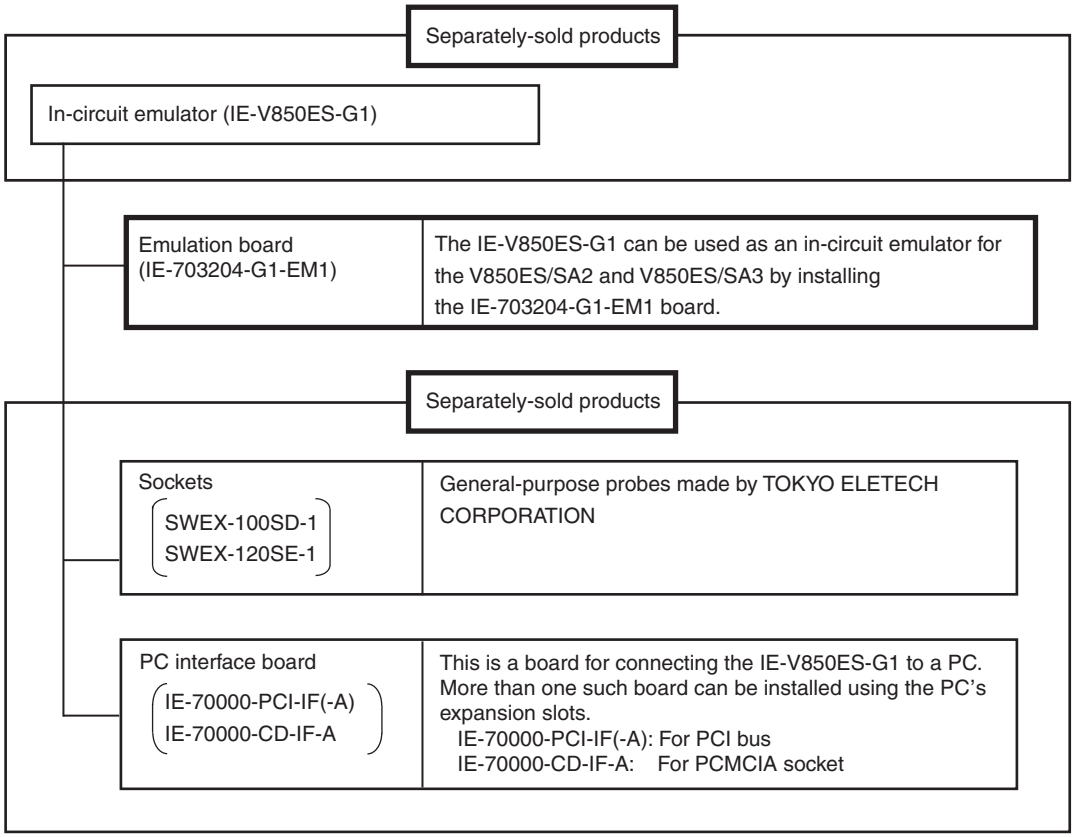
CHAPTER 1 OUTLINE

The IE-703204-G1-EM1 is an emulation board for the IE-V850ES-G1 in-circuit emulator.

Connected to the IE-V850ES-G1, the IE-703204-G1-EM1 can be used for efficient hardware and software debugging during system development using the V850ES/SA2 and V850ES/SA3.

This manual describes the basic setup procedure and the switch settings of the IE-V850ES-G1 when connected to the IE-703204-G1-EM1. For the part names and functions of the IE-V850ES-G1, refer to the separate **IE-V850ES-G1 User's Manual (U16313E)**.

1.1 Product Configuration



1.2 Features (When Connected to IE-V850ES-G1)

- Maximum operating frequency: 20 MHz (2.2 V to 2.7 V)
- The following pins can be masked.
  NMI, $\overline{\text{WAIT}}$, $\overline{\text{RESET}}$, $\overline{\text{HLDRQ}}$
- The external dimensions of the IE-703204-G1-EM1 are listed below

Item		Value
External dimensions	Height	35 mm
	Width	205 mm
	Depth	140 mm

1.3 Function Specifications (When Connected to IE-V850ES-G1)

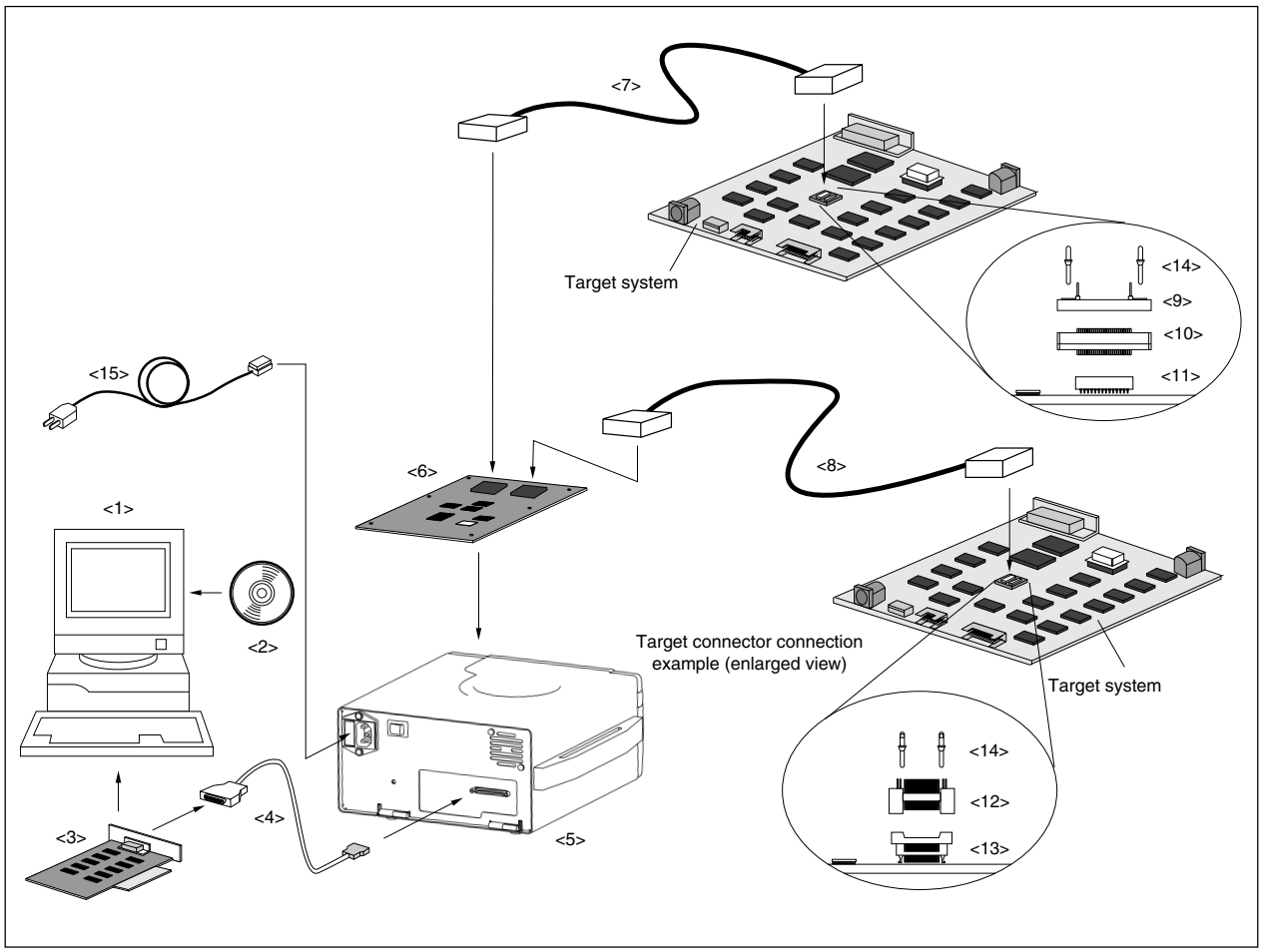
Item		Specification
Emulation memory capacity	Internal ROM	1 MB
	For user memory	4 MB
Execution/pass detection coverage memory capacity	Internal ROM	256 KB
	External memory	1 MB
Memory access detection coverage memory capacity	External memory	1 MB
Branch destination entry count calculation coverage memory capacity	Internal ROM	256 KB
	External memory	1 MB
Trace memory capacity		168 bits × 32 K frames
Time measurement function		Internal timers × 3
External logic probe		8-bit external trace possible
		Trace/break event setting possible
Break function		Event break
		Step execution break
		Forced break
		Fail-safe break • Illegal access to peripheral I/O • Access to guard area • Write to ROM area

Caution Some functions may not be supported depending on the debugger that is used.

1.4 System Configuration

The system configuration when using the IE-703204-G1-EM1 connected to the IE-V850ES-G1, which itself is connected to a PC (PC-9800 series or PC/AT™ compatible) is shown below.

Figure 1-1. System Configuration



Remarks <1>: PC (PC-9800 series or PC/AT compatible)

<2>: Debugger (sold separately), device file (obtained separately)[Note 1]

<3>: PC interface board (IE-70000-PCI-IF(-A), IE-70000-CD-IF-A: Sold separately)

<4>: PC interface cable (supplied with IE-V850ES-G1: Sold separately)

<5>: IE-V850ES-G1 (sold separately)

<6>: Emulation board (this product)

<7>: Probe[Note 2] (SWEX-120SE-1: Sold separately)

<8>: Probe[Note 2] (SWEX-100SD-1: Sold separately)

<9>: CSICE121A1312N03[Note 2] (sold separately)

<10>: LSPACK121A1312N01[Note 2] (sold separately)

<11>: CSSOCKET121A1312N01[Note 2] (sold separately) or CSSOCKET121A1312N01N[Note 2] (sold separately)
(CSSOCKET121A1312N01S1[Note 2] (sold separately) can be used for stacking.)
CSSOCKET121A1312N01N is a type with no guide pins.

<12>: YQPACK100SD[Note 2] (supplied with this product)

<13>: NQPACK100SD[Note 2] (supplied with this product)

<14>: YQGUIDE[Note 2] (supplied with this product)

<15>: Power supply cable (supplied with IE-V850-G1: Sold separately)

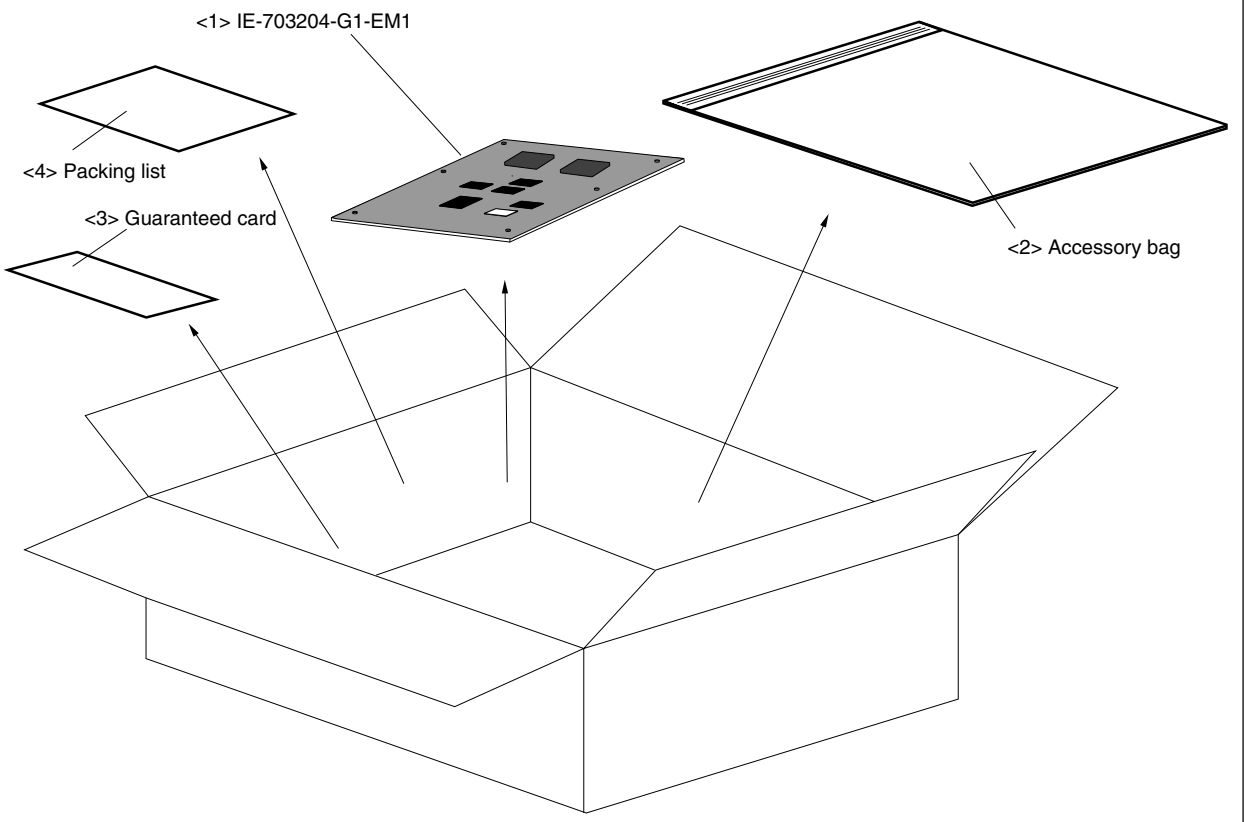
Notes 1. The device file can be downloaded from the NEC Electronics website. (URL: http://www.necel.com/micro)

2. These are products of TOKYO ELETECH CORPORATION.
For further information, contact Daimaru Kogyo Co., Ltd.
Tokyo Electronics Department (TEL: +81-3-3820-7112)
Osaka Electronics Department (TEL: +81-6-6244-6672)

1.5 Contents in Carton

The IE-703204-G1-EM1 package contains the IE-703204-G1-EM1 emulation board, a guarantee card, a packing list, this manual, and an accessory bag. Check whether the accessory bag contains the items listed below. If you find any missing or damaged items, contact an NEC Electronics sales representative or distributor.

Figure 1-2. Contents in Carton



<1> IE-703204-G1-EM1 × 1
<2> Accessory bag × 1
<3> Guarantee card × 1
<4> Packing list × 1

Check whether the accessory bag contains the following items in addition to this manual and the packing list (× 1).

(a) 7-pin header (for resonator replacement): × 1
(b) NQPACK100SD (for mounting board): × 1
YQPACK100SD (for mounting probe): × 1
HQPACK100SD (for mounting IC): × 1
YQ-GUIDE (guide pin): × 4
(c) Screws/washers: 6 sets (6 screws + 6 washers are included)

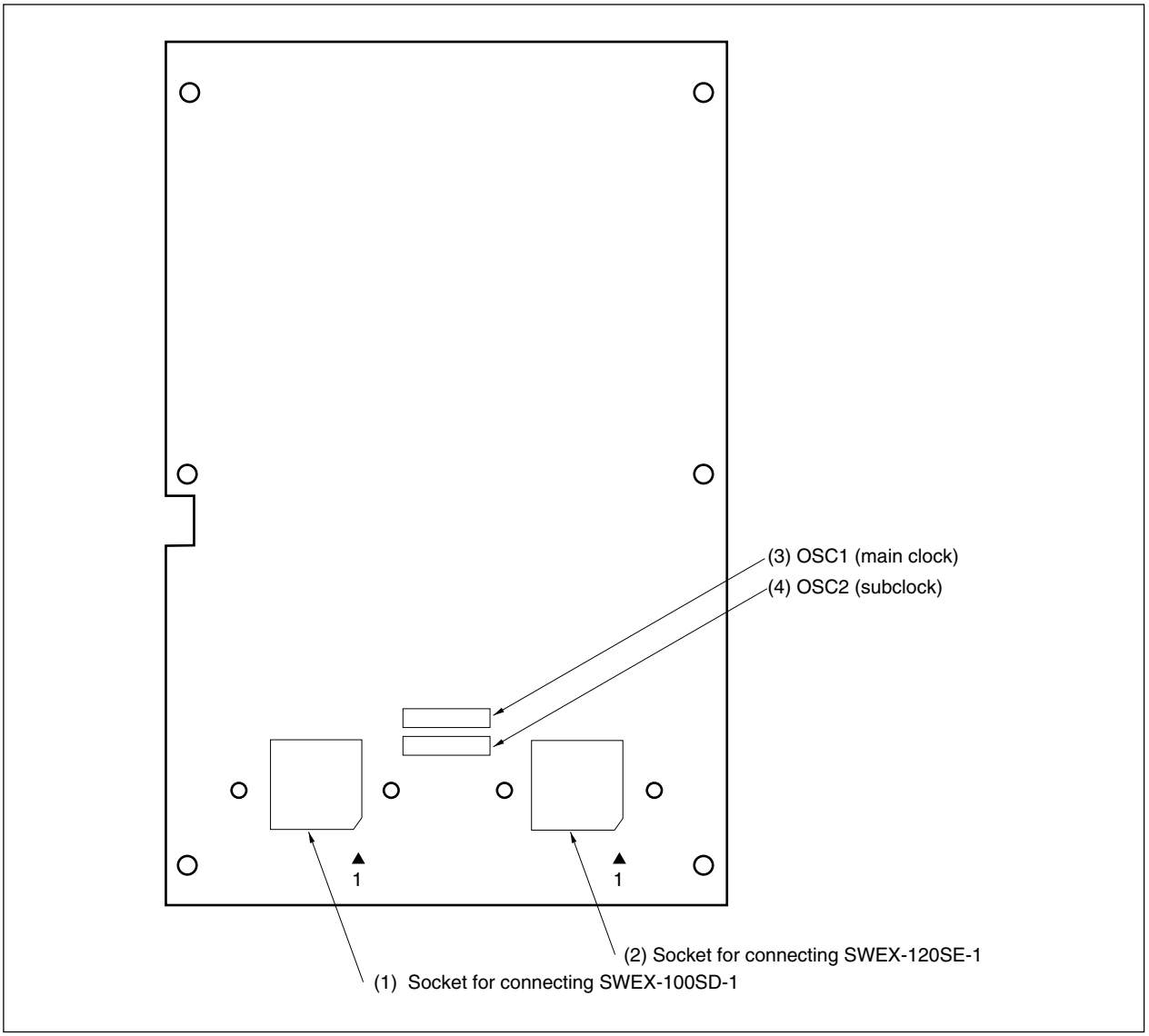
CHAPTER 2 PART NAMES AND FUNCTIONS

This chapter describes the part names and functions of the IE-703204-G1-EM1.

For the part names and functions of the IE-V850ES-G1, refer to the **IE-V850ES-G1 User's Manual (U16313E)**.

2.1 Part Names and Functions of IE-703204-G1-EM1

Figure 2-1. Part Names of IE-703204-G1-EM1



(1) Socket for connecting SWEX-100SD-1

Connect the SWEX-100SD-1 when using the IE-703204-G1-EM1 as the emulator of the V850ES/SA2.

(2) Socket for connecting SWEX-120SE-1

Connect the SWEX-120SE-1 when using the IE-703204-G1-EM1 as the emulator of the V850ES/SA3.

(3) OSC1 (main clock)

This is the socket in which the resonator that generates the main clock is mounted. Use this socket when replacing the resonator for the main clock. For details, refer to **3.2 Resonator Replacement**.

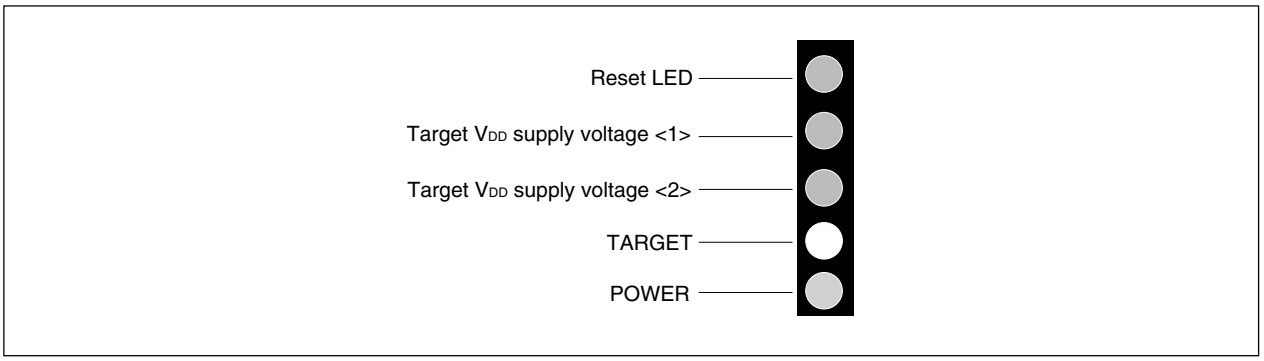
(4) OSC2 (subclock)

This is the socket in which the resonator that generates the subclock is mounted. The frequency of the subclock is fixed to 32.768 kHz, so the resonator for subclock cannot be replaced.

2.2 LEDs Controlled by IE-703204-G1-EM1

Some of the LEDs mounted in the IE-V850ES-G1 are controlled by the IE-703204-G1-EM1.
For the LEDs that are controlled by the IE-V850ES-G1, refer to the **IE-V850ES-G1 User's Manual (U16313E)**.

Figure 2-2. LEDs Controlled by IE-703204-G1-EM1



(1) Reset LED

The status of the $\overline{\text{RESET}}$ signal connected to the target system is indicated as follows.

Lit (ON): The target system is connected and the $\overline{\text{RESET}}$ signal is active (GND level).

Unlit (OFF): Either the target system is not connected, or the $\overline{\text{RESET}}$ signal is inactive (V_{DD} level).

(2) Target V_{DD} supply voltage <1>

The status of the V_{DD} signal connected to the target system is indicated as follows.

(This LED indicates the status of pin 11 during V850ES/SA2 emulation, and the status of the F3 pin during V850ES/SA3 emulation.)

Lit (ON): The target system is connected, and voltage is being applied to the V_{DD} pin.

Unlit (OFF): Either the target system is not connected, or voltage is not being applied to the V_{DD} pin.

(3) Target V_{DD} supply voltage <2>

The status of the V_{DD} signal connected to the target system is indicated as follows.

(This LED indicates the status of pin 19 during V850ES/SA2 emulation, and the status of the H2 pin during V850ES/SA3 emulation.)

Lit (ON): The target system is connected and voltage is being applied to the V_{DD} pin.

Unlit (OFF): Either the target system is not connected, or voltage is not being applied to the V_{DD} pin.

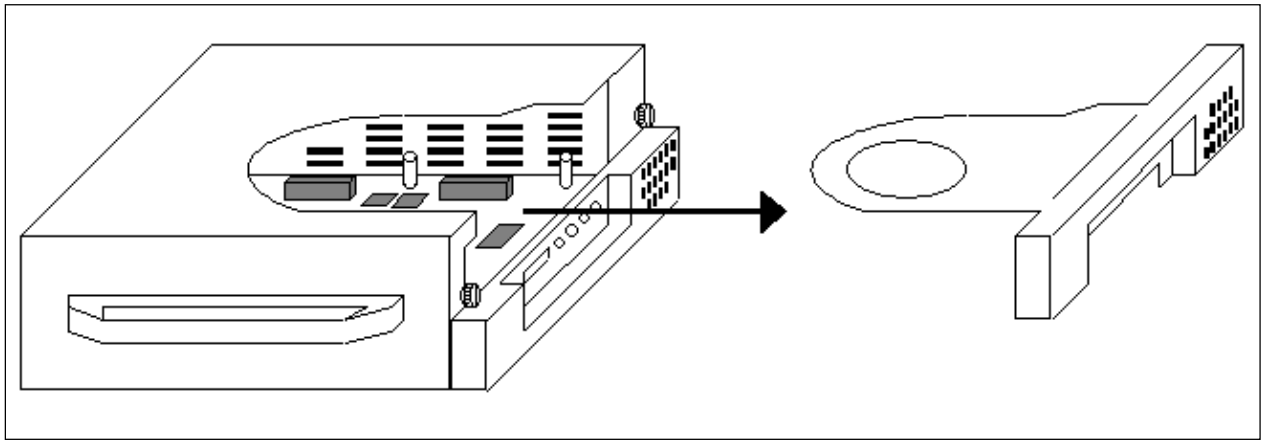
CHAPTER 3 SETUP PROCEDURE

This chapter describes how to connect the IE-703204-G1-EM1 to related products and how to replace the resonator.

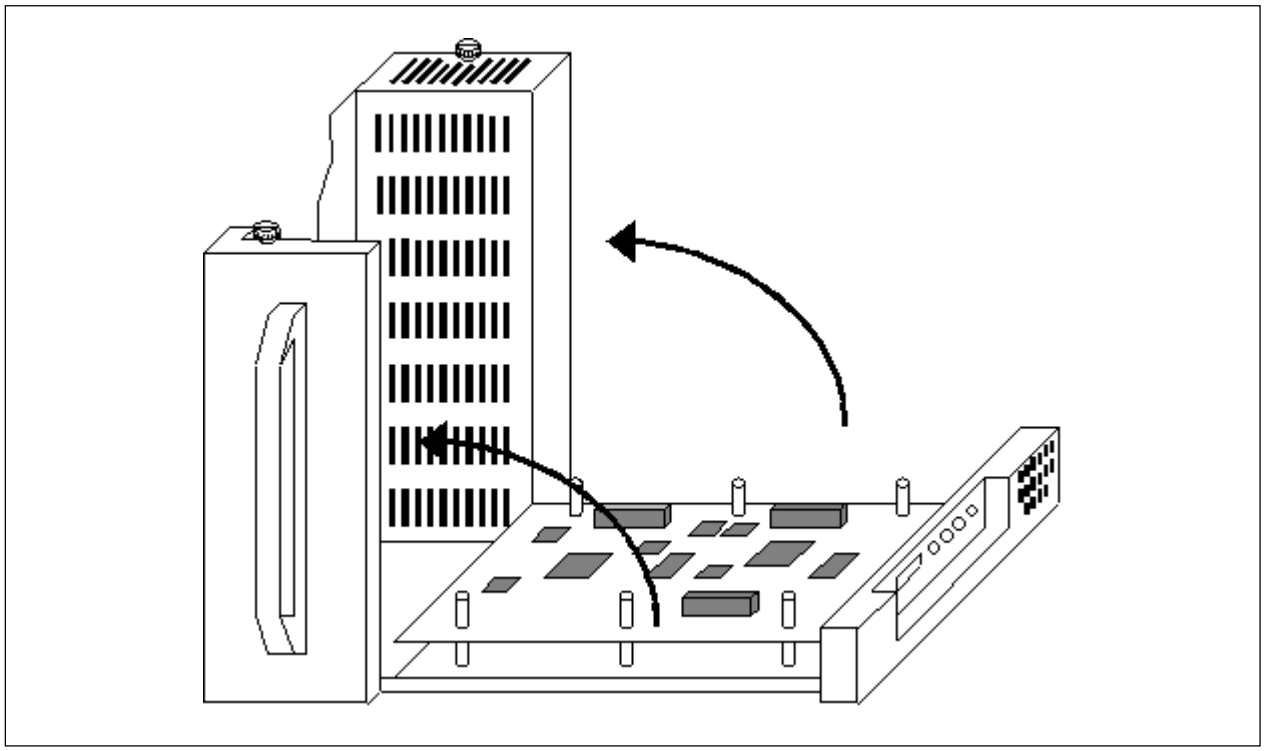
3.1 Connecting IE-V850ES-G1 and IE-703204-G1-EM1 with Probe

The following shows the procedure to connect the IE-V850ES-G1 and IE-703204-G1-EM1 with the probe.

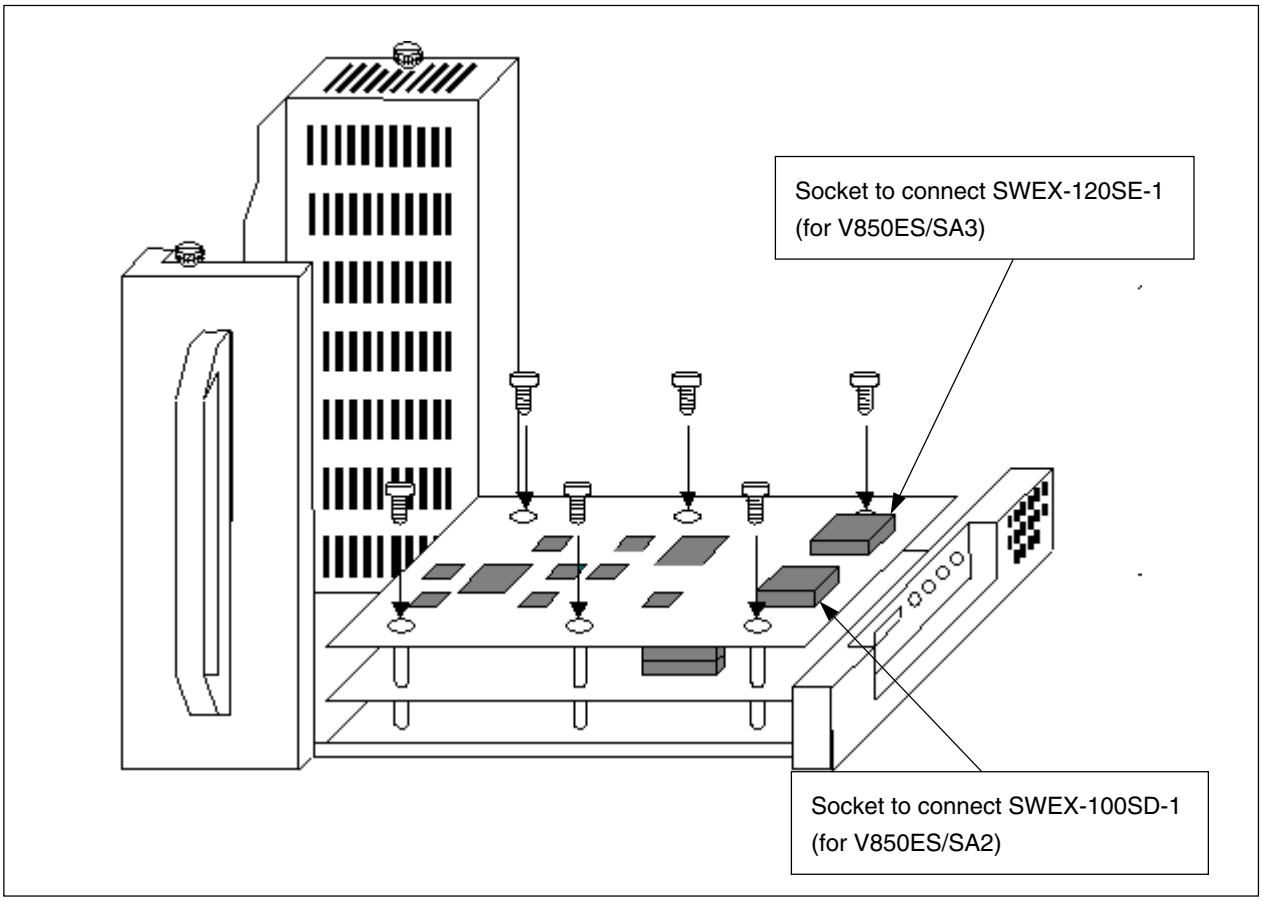
<1> Pull off the front cover of the IE-V850ES-G1.



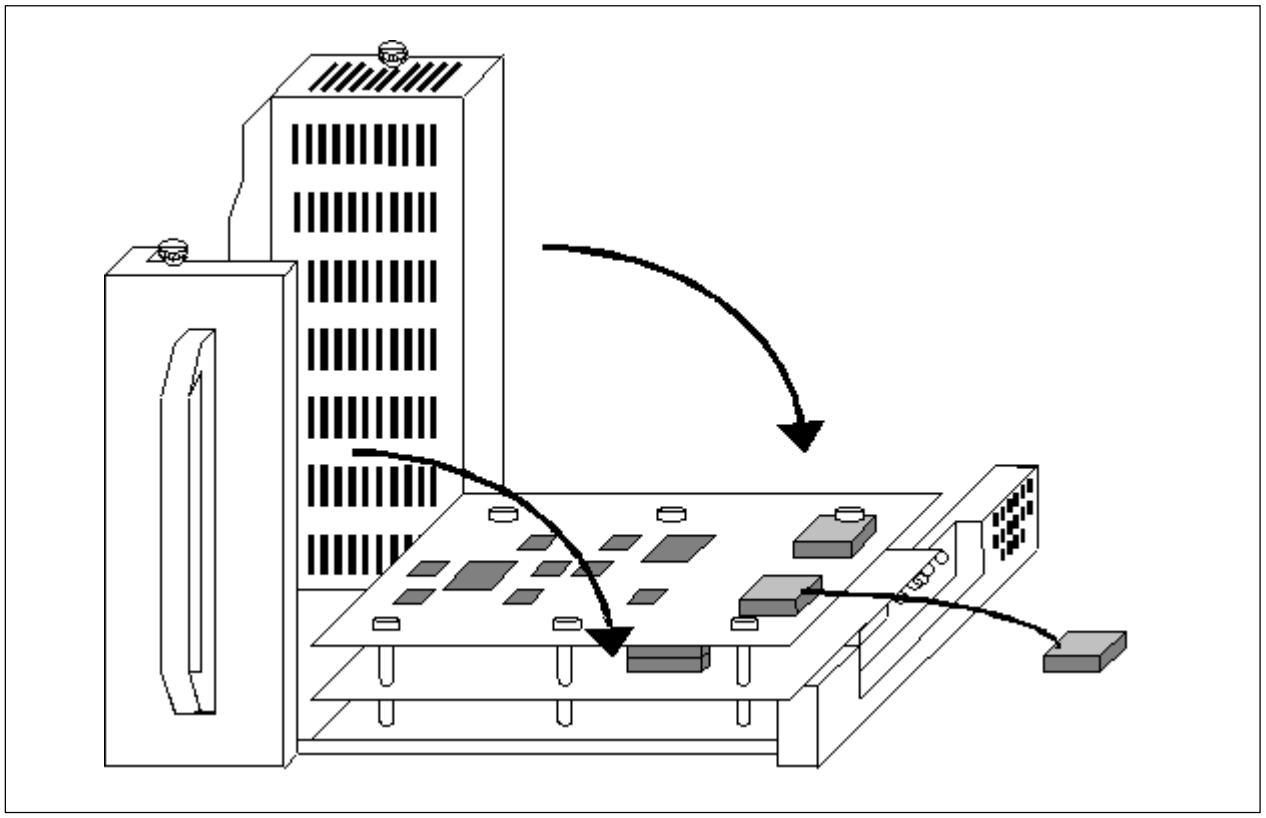
<2> Raise the frame of the IE-V850ES-G1 as shown.



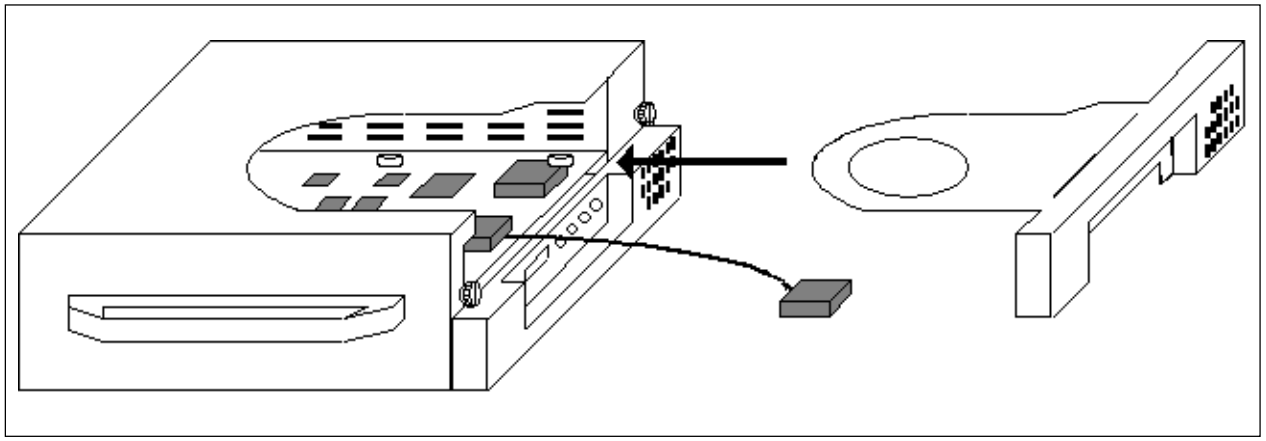
<3> With the main board and the IE-703204-G1-EM1 aligned as shown, insert three connectors on each side.
At this time align the board so that the socket (YQSOCKET) to connect the prove faces towards the probe exit side.
Insert the probe (SWEX-100SD-1 or SWEX-120SE-1) in the socket corresponding to the target device (refer to the following figure).



<4> Slowly lower the frame of the IE-V850ES-G1.



<5> Replace the front cover of the IE-V850ES-G1.

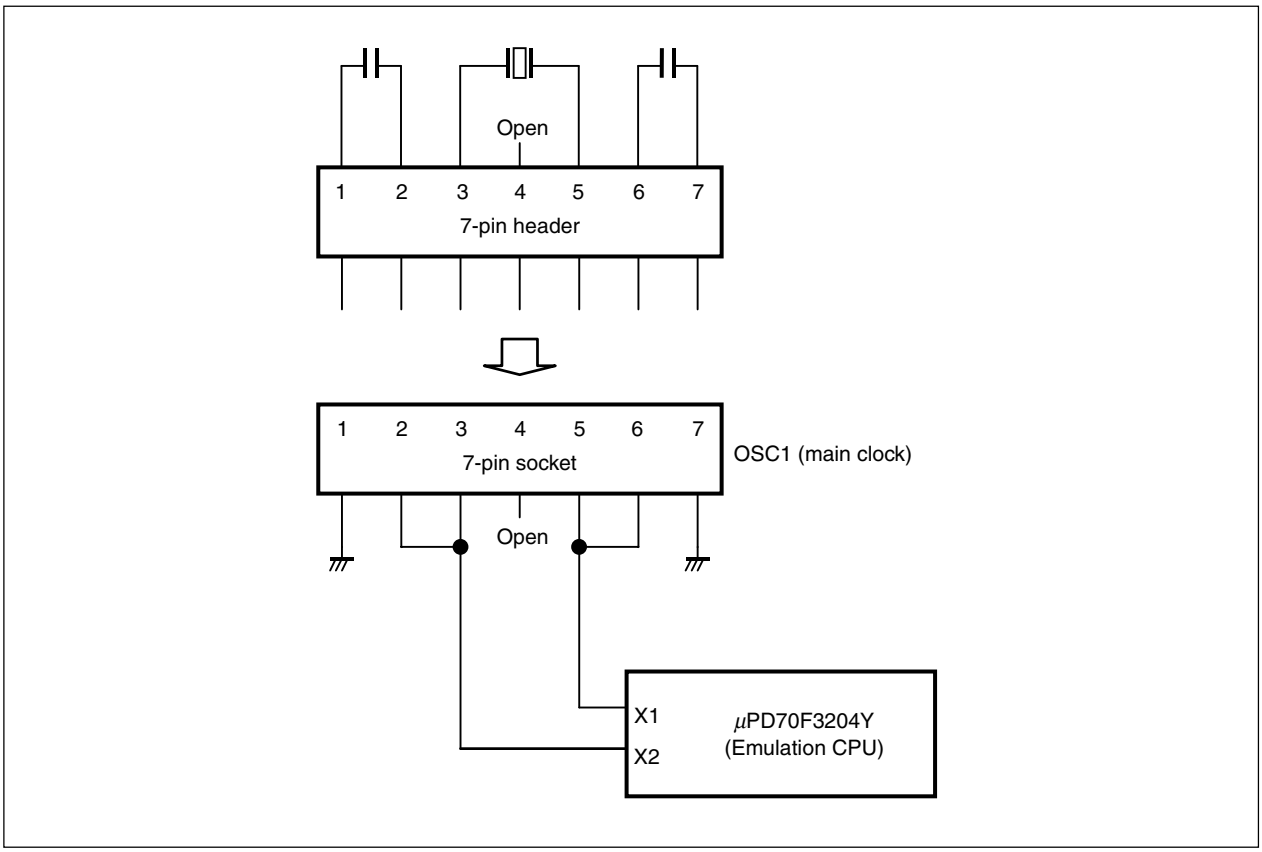


3.2 Replacing Resonator

The IE-703204-G1-EM1 does not support clock oscillation by the resonator on the target system. Therefore, to change the main clock frequency, replace the resonator mounted in OSC1 (main clock) on the IE-703204-G1-EM1 with a resonator with the desired frequency. After shipment, the following oscillators are mounted as oscillators for generating each clock.

Item	Setting
OSC1 (main clock)	20 MHz oscillator
OSC2 (subclock)	32.768 kHz oscillator

To change the main clock frequency, mount the resonator and capacitor on the included 7-pin header as shown and substitute it for the 7-pin header already mounted on OSC1 (main clock).



The frequency of the subclock is fixed to 32.768 kHz, so the resonator for the subclock cannot be replaced. The IE-703204-G1-EM1 does not support clock oscillation by the resonator on the target system. Therefore, operation between the resonator on the target system and the oscillator in the target device cannot be emulated using the IE-703204-G1-EM1.

CHAPTER 4 CAUTIONS

The following must be observed when using the IE-703204-G1-EM1.

4.1 Connection with Target System

Turn off power to the IE-V850ES-G1 before connecting the IE-703204-G1-EM1 to the target system.

4.2 Characteristics of Target Interface

The target interface (signals connecting the in-circuit emulator and the target system) functionally operates as if an actual device is connected, however, the characteristics may be different than those of the actual device. The target interface of the IE-703204-G1-EM1 is one of those shown in Figures 4-1 to 4-12. The target interface processing of each target device is shown in Tables 4-1 and 4-2.

Figure 4-1. Equivalent Circuit A

Figure 4-2. Equivalent Circuit B

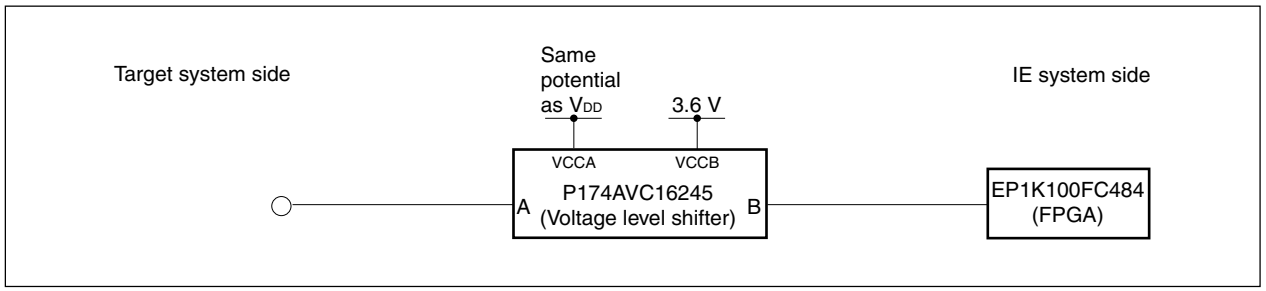


Figure 4-3. Equivalent Circuit C

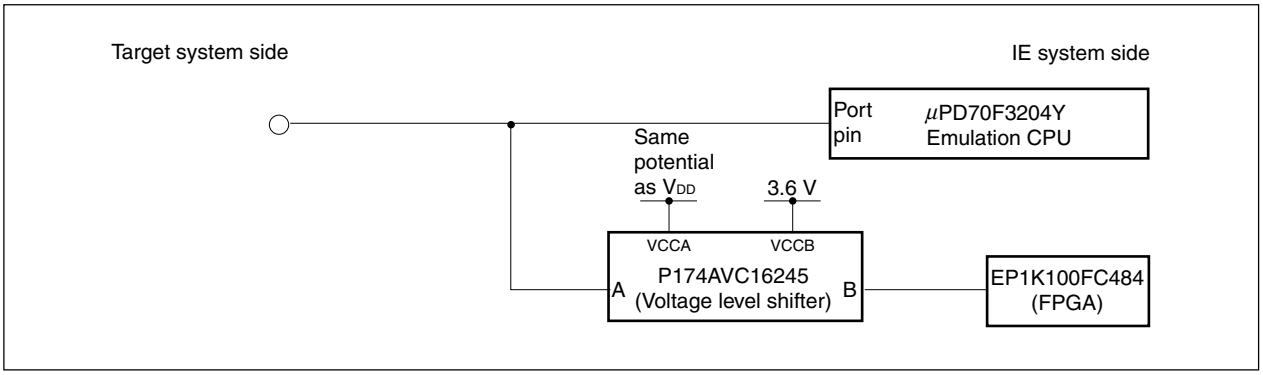


Figure 4-4. Equivalent Circuit D

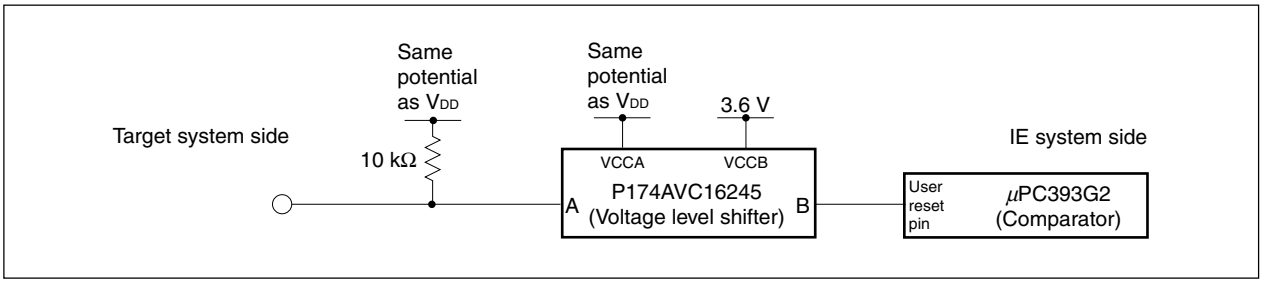
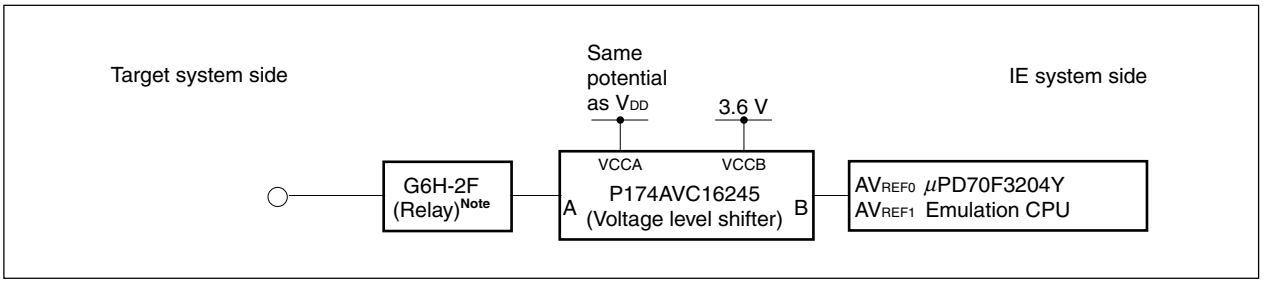


Figure 4-5. Equivalent Circuit E



Note Conducts only when the target system is connected.

Figure 4-6. Equivalent Circuit F

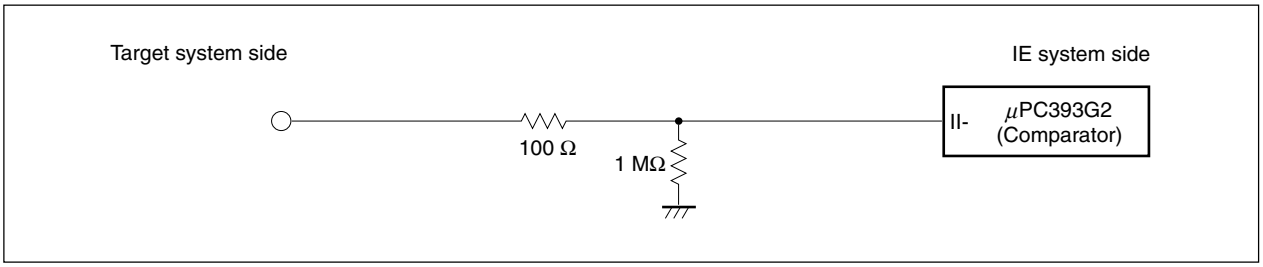
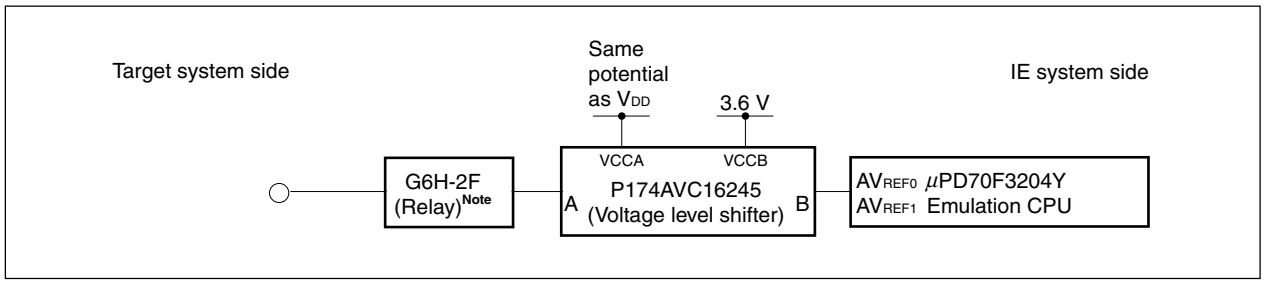


Figure 4-7. Equivalent Circuit G



Note Conducts only when the target system is connected.

Figure 4-8. Equivalent Circuit H

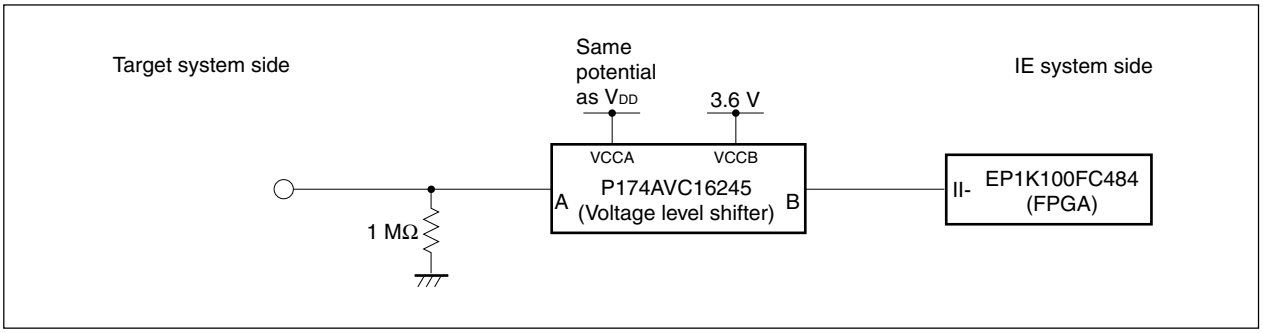


Figure 4-9. Equivalent Circuit I

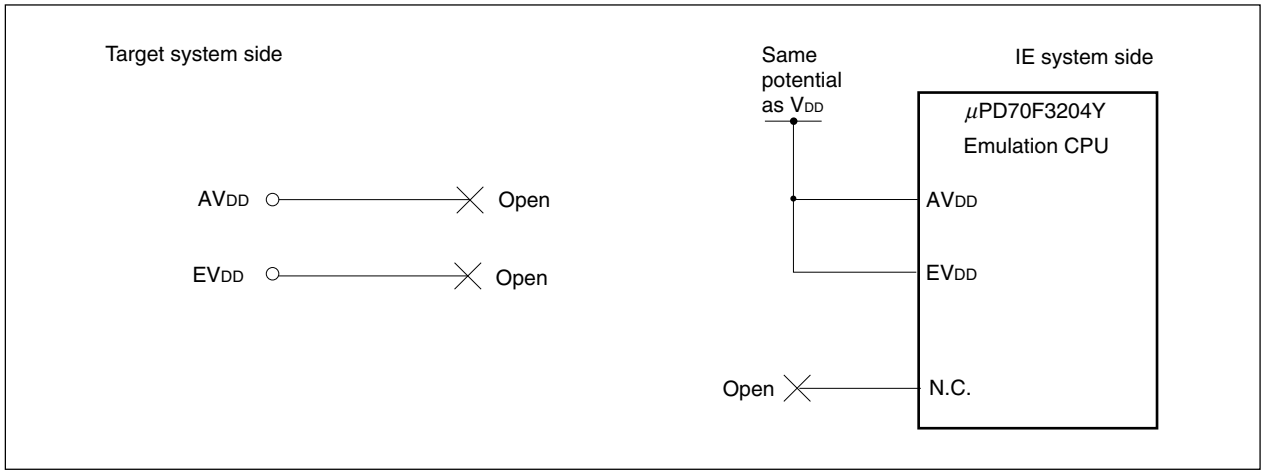


Figure 4-10. Equivalent Circuit J

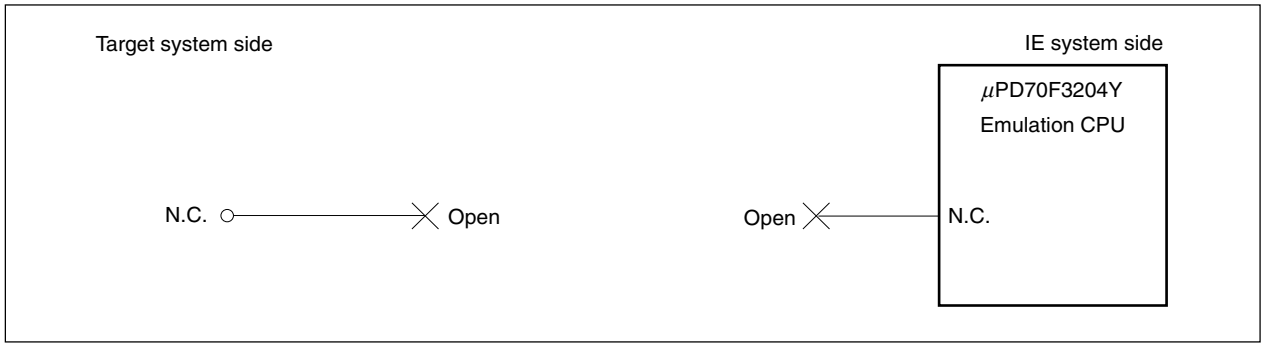


Figure 4-11. Equivalent Circuit K

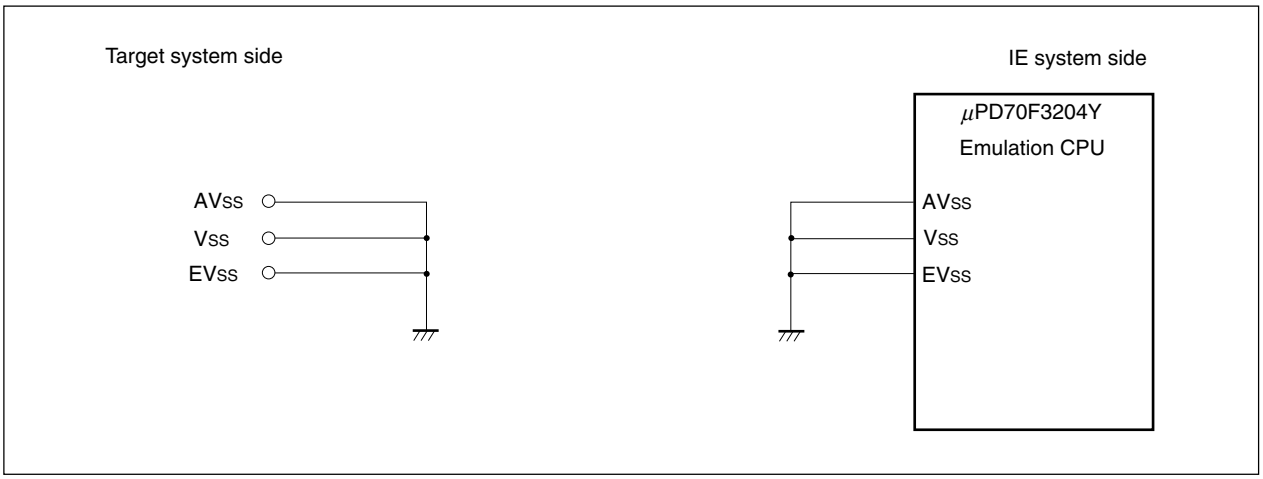


Figure 4-12. Equivalent Circuit L

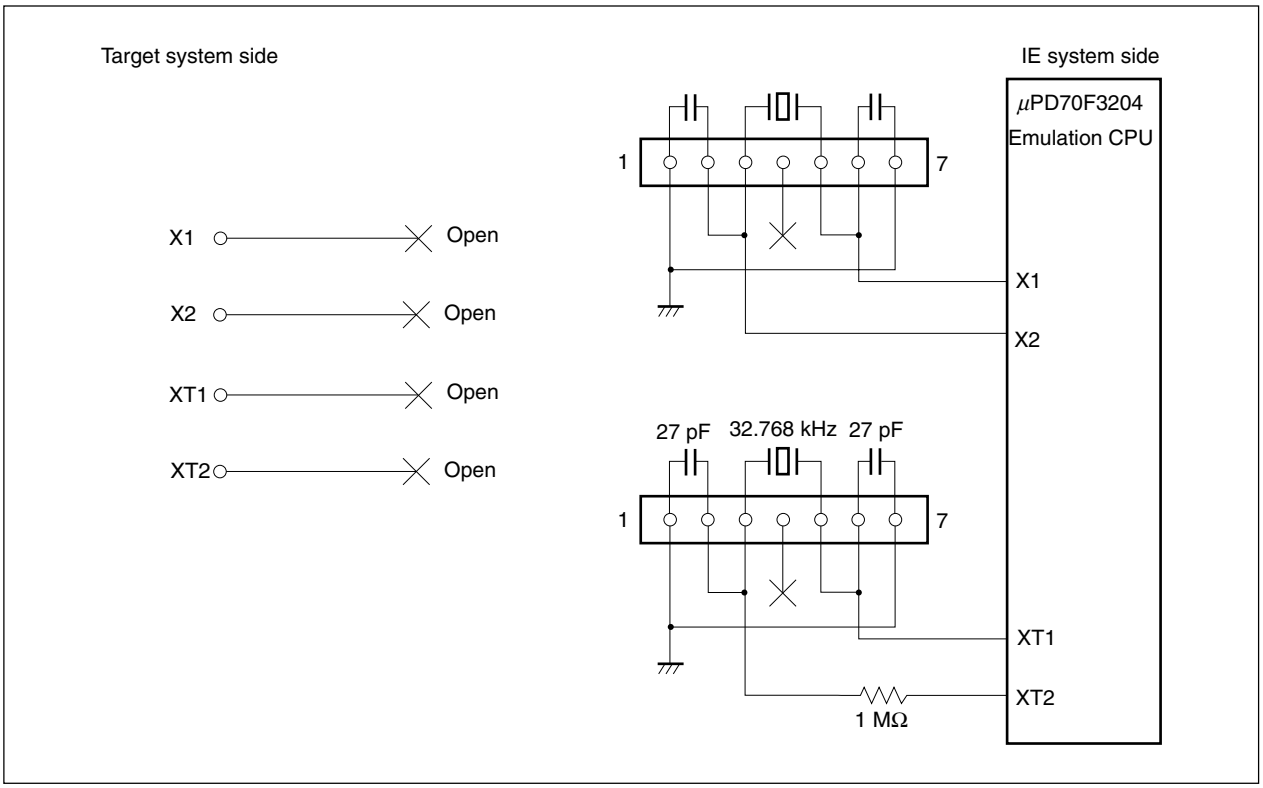


Table 4-1. Pin Correspondence List (V850ES/SA2 Pin Names) (1/3)

V850ES/SA2 Pin No.	Target Interface Name (V850ES/SA2 Pin Names)	Processing in In-Circuit Emulator
1	AV_{REF0}	Emulation circuit E
2	AV_{DD}	Emulation circuit I
3	AV_{SS}	Emulation circuit K
4	P80/ANO0	Emulation circuit A
5	P81/ANO1	Emulation circuit A
6	AV_{REF1}	Emulation circuit E
7	P00/NMI	Emulation circuit A
8	P30/SI1/RXD0	Emulation circuit A
9	P31/SO1/TXD0	Emulation circuit A
10	P32/$\overline{SCK1}$	Emulation circuit A
11	V_{DD}	Emulation circuit A
12	V_{SS}	Emulation circuit K
13	X1	Emulation circuit L
14	X2	Emulation circuit L
15	$\overline{RESET}$	Emulation circuit D
16	XT1	Emulation circuit L
17	XT2	Emulation circuit L
18	V_{DD}	Emulation circuit G
19	V_{SS}	Emulation circuit K
20	P90/A0	Emulation circuit C
21	P91/A1	Emulation circuit C
22	P92/A2/INTP5	Emulation circuit C
23	P93/A3/INTP6	Emulation circuit C
24	P94/A4/TO2	Emulation circuit C
25	P95/A5/TO3	Emulation circuit C
26	P96/A6/TO4	Emulation circuit C
27	P97/A7/TO5	Emulation circuit C
28	P98/A8/RXD1	Emulation circuit C
29	P99/A9/TXD1	Emulation circuit C
30	P910/A10/SI2	Emulation circuit C
31	P911/A11/SO2	Emulation circuit C
32	P912/A12/$\overline{SCK2}$	Emulation circuit C
33	P913/A13/SI3	Emulation circuit C
34	P914/A14/SO3	Emulation circuit C
35	P915/A15/$\overline{SCK3}$	Emulation circuit C
36	EV_{SS}	Emulation circuit K
37	EV_{DD}	Emulation circuit I
38	PCS0/$\overline{CS0}$	Emulation circuit B
39	PCS1/$\overline{CS1}$	Emulation circuit B
40	PCS2/$\overline{CS2}$	Emulation circuit B

Table 4-1. Pin Correspondence List (V850ES/SA2 Pin Names) (2/3)

V850ES/SA2 Pin No.	Target Interface Name (V850ES/SA2 Pin Names)	Processing in In-Circuit Emulator
41	PCS3/$\overline{CS3}$	Emulation circuit B
42	PCM0/$\overline{WAIT}$	Emulation circuit B
43	PCM1/CLKOUT	Emulation circuit B
44	PCM2/$\overline{HLDAK}$	Emulation circuit B
45	PCM3/$\overline{HLDRQ}$	Emulation circuit B
46	PCT0/$\overline{WR0}$	Emulation circuit B
47	PCT1/$\overline{WR1}$	Emulation circuit B
48	PCT4/$\overline{RD}$	Emulation circuit B
49	PCT5	Emulation circuit B
50	PCT6/ASTB	Emulation circuit B
51	PCT7	Emulation circuit B
52	PDL0/AD0	Emulation circuit B
53	PDL1/AD1	Emulation circuit B
54	PDL2/AD2	Emulation circuit B
55	PDL3/AD3	Emulation circuit B
56	PDL4/AD4	Emulation circuit B
57	PDL5/AD5/FLMD1	Emulation circuit B
58	PDL6/AD6	Emulation circuit B
59	PDL7/AD7	Emulation circuit B
60	PDL8/AD8	Emulation circuit B
61	PDL9/AD9	Emulation circuit B
62	IC/FLMD0	Emulation circuit B
63	EV_{SS}	Emulation circuit K
64	EV_{DD}	Emulation circuit I
65	PDL10/AD10	Emulation circuit B
66	PDL11/AD11	Emulation circuit B
67	PDL12/AD12	Emulation circuit B
68	PDL13/AD13	Emulation circuit B
69	PDL14/AD14	Emulation circuit B
70	PDL15/AD15	Emulation circuit B
71	PDH0/A16	Emulation circuit B
72	PDH1/A17	Emulation circuit B
73	PDH2/A18	Emulation circuit B
74	PDH3/A19	Emulation circuit B
75	PDH4/A20	Emulation circuit B
76	PDH5/A21	Emulation circuit B
77	P40/SI0	Emulation circuit A
78	P41/SO0/SDA	Emulation circuit A
79	P42/$\overline{SCK0}$/SCL	Emulation circuit A
80	P43/INTP00/TI0/TCLR0	Emulation circuit A

Table 4-1. Pin Correspondence List (V850ES/SA2 Pin Names) (3/3)

V850ES/SA2 Pin No.	Target Interface Name (V850ES/SA2 Pin Names)	Processing in In-Circuit Emulator
81	P44/INTP01/TO0	Emulation circuit A
82	P45/INTP10/TI1/TCLR1	Emulation circuit A
83	P46/INTP11/TO1	Emulation circuit A
84	P01/INTP0/TI2	Emulation circuit A
85	P02/INTP1/TI3	Emulation circuit A
86	P03/INTP2/TI4	Emulation circuit A
87	P04/INTP3/TI5	Emulation circuit A
88	P05/INTP4	Emulation circuit A
89	P711/ANI11	Emulation circuit A
90	P710/ANI10	Emulation circuit A
91	P79/ANI9	Emulation circuit A
92	P78/ANI8	Emulation circuit A
93	P77/ANI7	Emulation circuit A
94	P76/ANI6	Emulation circuit A
95	P75/ANI5	Emulation circuit A
96	P74/ANI4	Emulation circuit A
97	P73/ANI3	Emulation circuit A
98	P72/ANI2	Emulation circuit A
99	P71/ANI1	Emulation circuit A
100	P70/ANI0	Emulation circuit A

Table 4-2. Pin Correspondence List (V850ES/SA3 Pin Names) (1/3)

V850ES/SA3 Pin No.	Target Interface Name (V850ES/SA3 Pin Names)	Processing in In-Circuit Emulator
A1	P70/ANI0	Emulation circuit A
A2	P71/ANI1	Emulation circuit A
A3	P73/ANI3	Emulation circuit A
A4	P713/ANI13	Emulation circuit A
A5	P76/ANI6	Emulation circuit A
A6	P78/ANI8	Emulation circuit A
A7	P711/ANI11	Emulation circuit A
A8	P04/INTP3/TI5	Emulation circuit A
A9	PCD2	Emulation circuit B
A10	P45/INTP10/TI1/TCLR1	Emulation circuit A
A11	P43/INTP00/TI0/TCLR0	Emulation circuit A
A12	P41/SO0/SDA	Emulation circuit A
A13	PDH5/A21	Emulation circuit B
B1	AV_{DD}	Emulation circuit I
B2	AV_{REF0}	Emulation circuit E
B3	P72/ANI2	Emulation circuit A
B4	P712/ANI12	Emulation circuit A
B5	P75/ANI5	Emulation circuit A
B6	P77/ANI7	Emulation circuit A
B7	P710/ANI10	Emulation circuit A
B8	PCD3	Emulation circuit B
B9	P02/INTP1/TI3	Emulation circuit A
B10	P46/INTP11/TO1	Emulation circuit A
B11	P42/$\overline{SCK0}$/SCL	Emulation circuit A
B12	P40/SI0	Emulation circuit A
B13	PDH4/A20	Emulation circuit B
C1	P80/ANO0	Emulation circuit A
C2	AV_{SS}	Emulation circuit K
C3	P74/ANI4	Emulation circuit A
C4	P714/ANI14	Emulation circuit A
C5	P715/ANI15	Emulation circuit A
C6	P79/ANI9	Emulation circuit A
C7	P05/INTP4[/ADTRG]	Emulation circuit A
C8	P03/INTP2/TI4	Emulation circuit A
C9	PCD1	Emulation circuit B
C10	P01/INTP0/TI2	Emulation circuit A
C11	P44/INTP01/TO0	Emulation circuit A
C12	PDH3/A19	Emulation circuit B
C13	PDH7/A23	Emulation circuit H
D1	P81/ANO1	Emulation circuit A
D2	AV_{REF1}	Emulation circuit E

Table 4-2. Pin Correspondence List (V850ES/SA3 Pin Names) (2/3)

V850ES/SA3 Pin No.	Target Interface Name (V850ES/SA3 Pin Names)	Processing in In-Circuit Emulator
D3	P00/NMI	Emulation circuit A
D4	N.C.	Emulation circuit J
D11	PDH0/A16	Emulation circuit B
D12	PDH2/A18	Emulation circuit B
D13	PDH1/A17	Emulation circuit B
E1	P30/SI1/RXD0	Emulation circuit A
E2	P31/SO1/TXD0	Emulation circuit A
E3	P32/$\overline{\text{SCK1}}$	Emulation circuit A
E11	PDL14/AD14	Emulation circuit B
E12	PDH6/A22	Emulation circuit H
E13	PDL15/AD15	Emulation circuit B
F1	V_{SS}	Emulation circuit K
F2	X1	Emulation circuit L
F3	V_{DD}	Emulation circuit F
F11	PDL11/AD11	Emulation circuit B
F12	PDL13/AD13	Emulation circuit B
F13	PDL12/AD12	Emulation circuit B
G1	$\overline{\text{RESET}}$	Emulation circuit D
G2	XT1	Emulation circuit L
G3	X2	Emulation circuit L
G11	EV_{SS}	Emulation circuit K
G12	PDL10/AD10	Emulation circuit B
G13	EV_{DD}	Emulation circuit I
H1	V_{SS}	Emulation circuit K
H2	V_{DD}	Emulation circuit G
H3	XT2	Emulation circuit L
H11	PDL8/AD8	Emulation circuit B
H12	MODE/FLMD0	Emulation circuit B
H13	PDL9/AD9	Emulation circuit B
J1	P20/SI4	Emulation circuit A
J2	P91/A1	Emulation circuit C
J3	P90/A0	Emulation circuit C
J11	PDL5/AD5/FLMD1	Emulation circuit B
J12	PDL7/AD7	Emulation circuit B
J13	PDL6/AD6	Emulation circuit B
K1	P22/$\overline{\text{SCK4}}$	Emulation circuit A
K2	P92/A2/INTP5	Emulation circuit C
K3	P21/SO4	Emulation circuit A
K11	PCM1/CLKOUT	Emulation circuit B
K12	PDL4/AD4	Emulation circuit B

Table 4-2. Pin Correspondence List (V850ES/SA3 Pin Names) (3/3)

V850ES/SA3 Pin No.	Target Interface Name (V850ES/SA3 Pin Names)	Processing in In-Circuit Emulator
K13	PDL3/AD3	Emulation circuit B
L1	P93/A3/INTP6	Emulation circuit C
L2	P94/A4/TO2	Emulation circuit C
L3	P911/A11/SO2	Emulation circuit C
L4	P914/A14/SO3	Emulation circuit C
L5	P915/A15/$\overline{\text{SCK3}}$	Emulation circuit C
L6	EV_{DD}	Emulation circuit I
L7	PCS0/$\overline{\text{CS0}}$	Emulation circuit B
L8	PCS2/$\overline{\text{CS2}}$	Emulation circuit B
L9	PCM4	Emulation circuit H
L10	PCT2	Emulation circuit H
L11	PCT0/$\overline{\text{WR0}}$	Emulation circuit B
L12	PDL1/AD1	Emulation circuit B
L13	PDL2/AD2	Emulation circuit B
M1	P95/A5/TO3	Emulation circuit C
M2	P97/A7/TO5	Emulation circuit C
M3	P99/A9/TXD1	Emulation circuit C
M4	P913/A13/SI3	Emulation circuit C
M5	EV_{SS}	Emulation circuit K
M6	PCS5	Emulation circuit H
M7	PCS4	Emulation circuit H
M8	PCM0/$\overline{\text{WAIT}}$	Emulation circuit B
M9	PCM2/$\overline{\text{HLDAK}}$	Emulation circuit B
M10	PCT3	Emulation circuit H
M11	PCT4/$\overline{\text{RD}}$	Emulation circuit B
M12	PCT7	Emulation circuit B
M13	PDL0/AD0	Emulation circuit B
N1	P96/A6/TO4	Emulation circuit C
N2	P98/A8/RXD1	Emulation circuit C
N3	P910/A10/SI2	Emulation circuit C
N4	P912/A12/$\overline{\text{SCK2}}$	Emulation circuit C
N5	PCS7	Emulation circuit H
N6	PCS6	Emulation circuit H
N7	PCS1/$\overline{\text{CS1}}$	Emulation circuit B
N8	PCS3/$\overline{\text{CS3}}$	Emulation circuit B
N9	PCM5	Emulation circuit H
N10	PCM3/$\overline{\text{HLDRQ}}$	Emulation circuit B
N11	PCT1/$\overline{\text{WR1}}$	Emulation circuit B
N12	PCT5	Emulation circuit B
N13	PCT6/ASTB	Emulation circuit B

CHAPTER 5 RESTRICTIONS

The IE-703204-G1-EM1 has the following restrictions.

5.1 Clock Generator

(1) Resonator to be connected
Oscillation by the resonator on the target system is not supported. Therefore, clock oscillation operation on the target system cannot be emulated with the in-circuit emulator.

(2) Emulation of oscillation stabilization time after reset has been released
In the target device for emulation, oscillation stabilization time is inserted after reset has been released; however, it is not inserted in the in-circuit emulator.

(3) Operation clock after reset
In the target device for emulation, the operation clock after reset is $f_{XX}/8$; however, there may be a period in which the clock is not initialized to $f_{XX}/8$ with the in-circuit emulator (depending on the timing of reset release).

5.2 Timing of Setting/Releasing Standby Mode

The timing of setting/releasing the standby mode is different between the target device and the in-circuit emulator.
The difference is within 1 clock when standby mode is set, and 2 or 3 clocks when it is released.

5.3 DMA

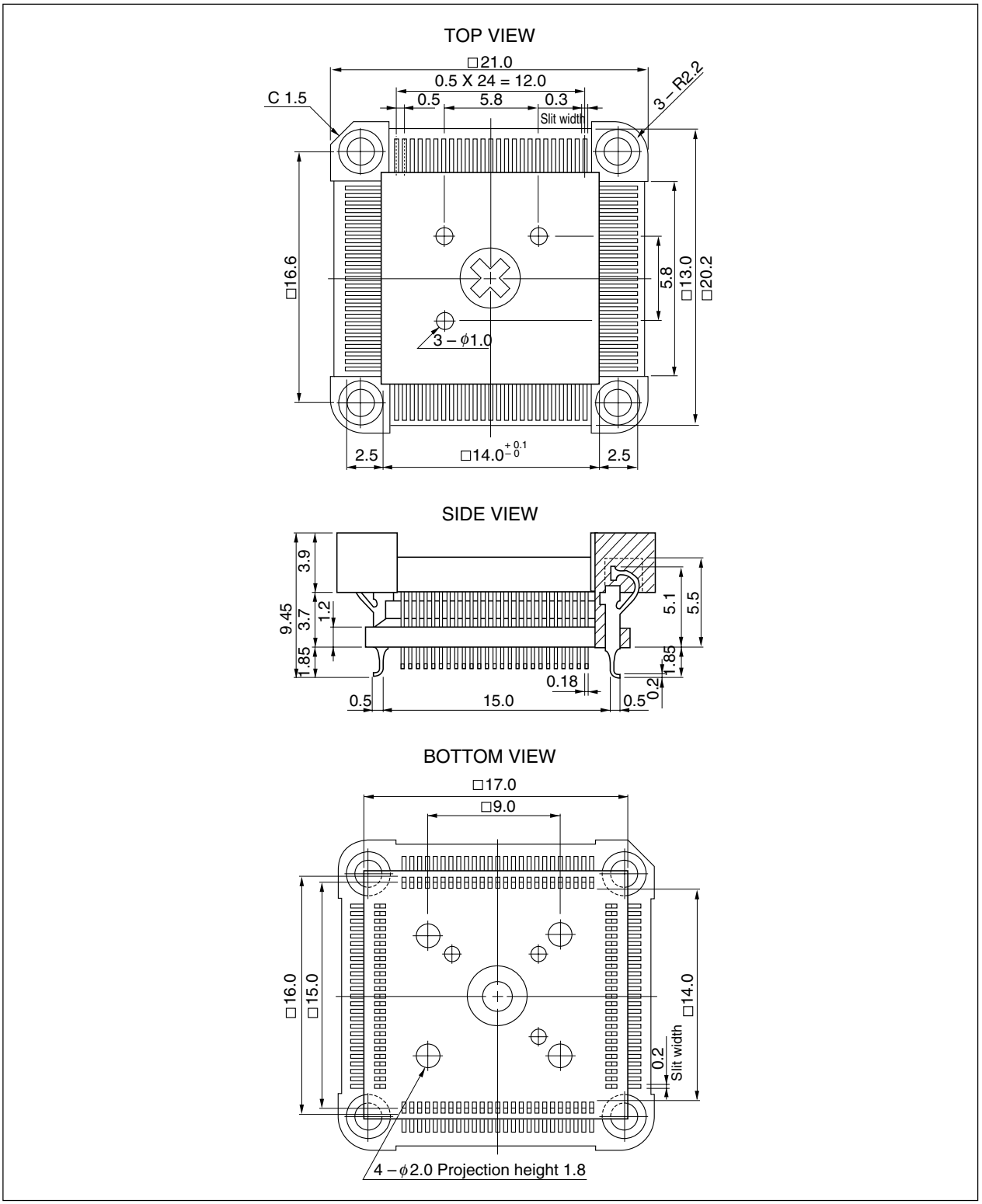
The status of the DCHC0 to DCHC3 registers of the DMA function vary when read; however, these registers cannot be displayed by the I/O register browser of the debugger.

5.4 Operation During Break

In the in-circuit emulator, peripheral functions operate during a break, so there may be a difference between the operations of the in-circuit emulator and target device.
(However, while the in-circuit emulator is in the break status, the counter of the watchdog timer stops.)

APPENDIX A PACKAGE DRAWINGS

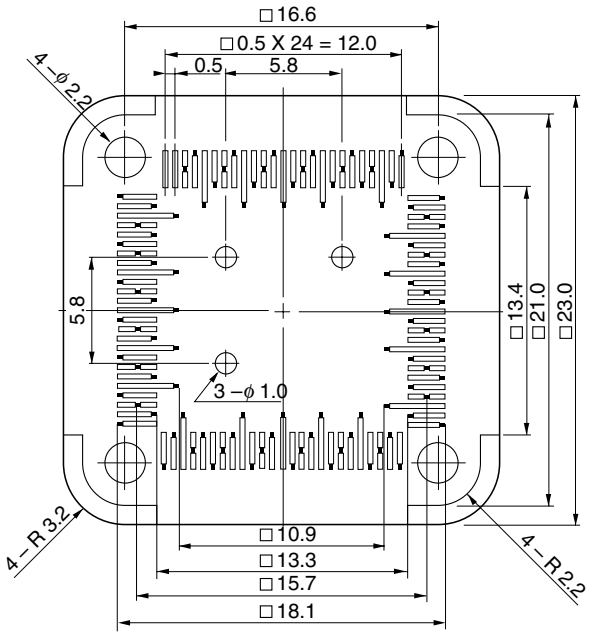
(1) NQPACK100SD (unit: mm)



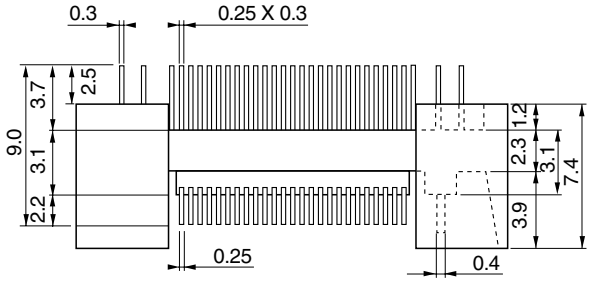
Remark NQPACK100SD is a product of TOKYO ELETECH CORPORATION.

(2) YQPACK100SD (unit: mm)

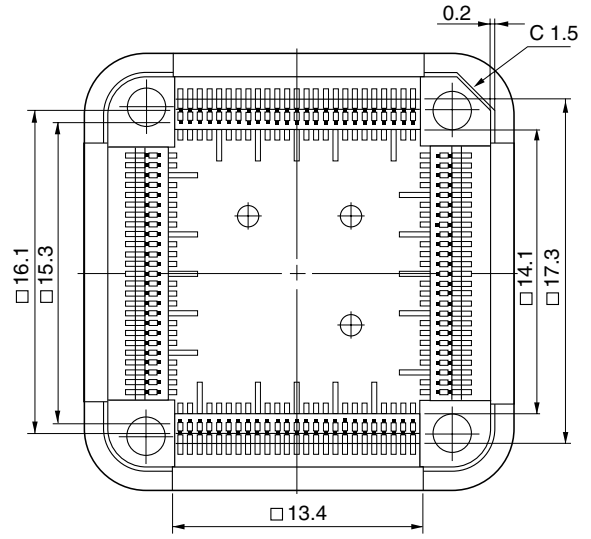
TOP VIEW



SIDE VIEW

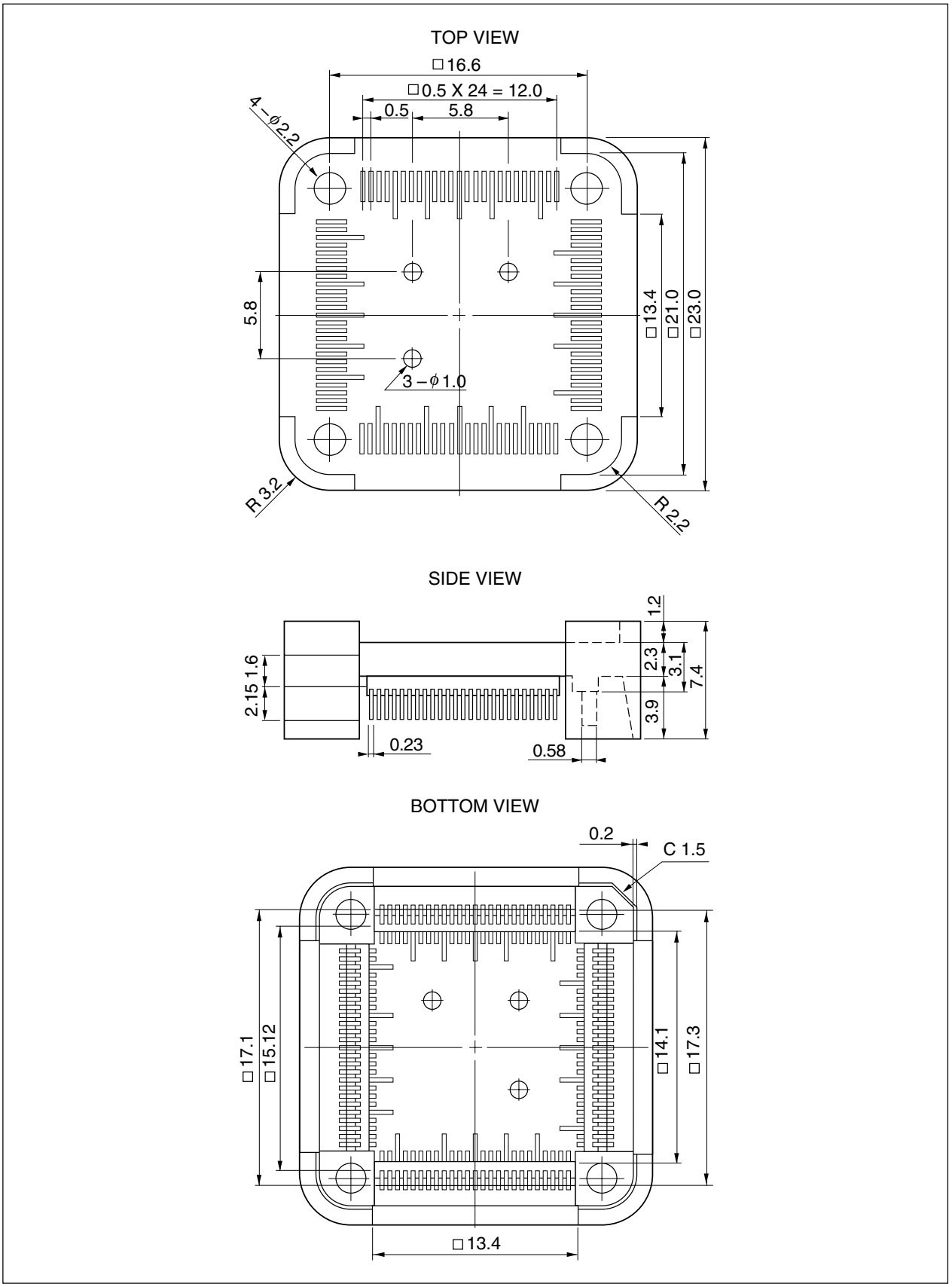


BOTTOM VIEW



Remark YQPACK100SD is a product of TOKYO ELETECH CORPORATION.

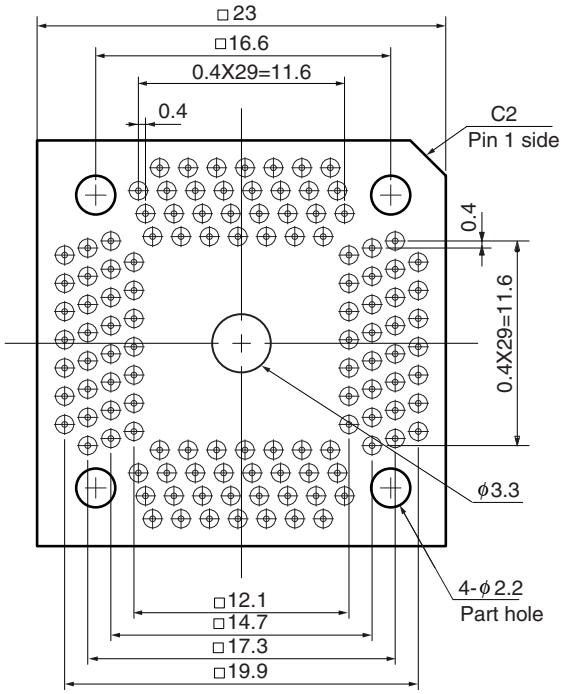
(3) HQPACK100SD (unit: mm)



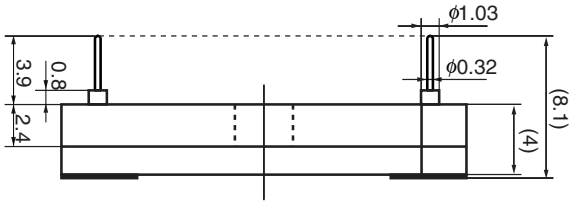
Remark HQPACK100SD is a product of TOKYO ELETECH CORPORATION.

(4) CSICE121A1312N03 (unit: mm)

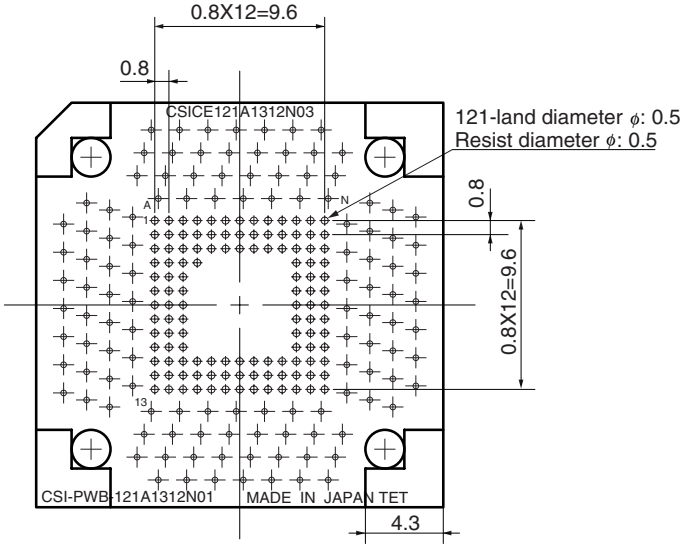
TOP VIEW



SIDE VIEW

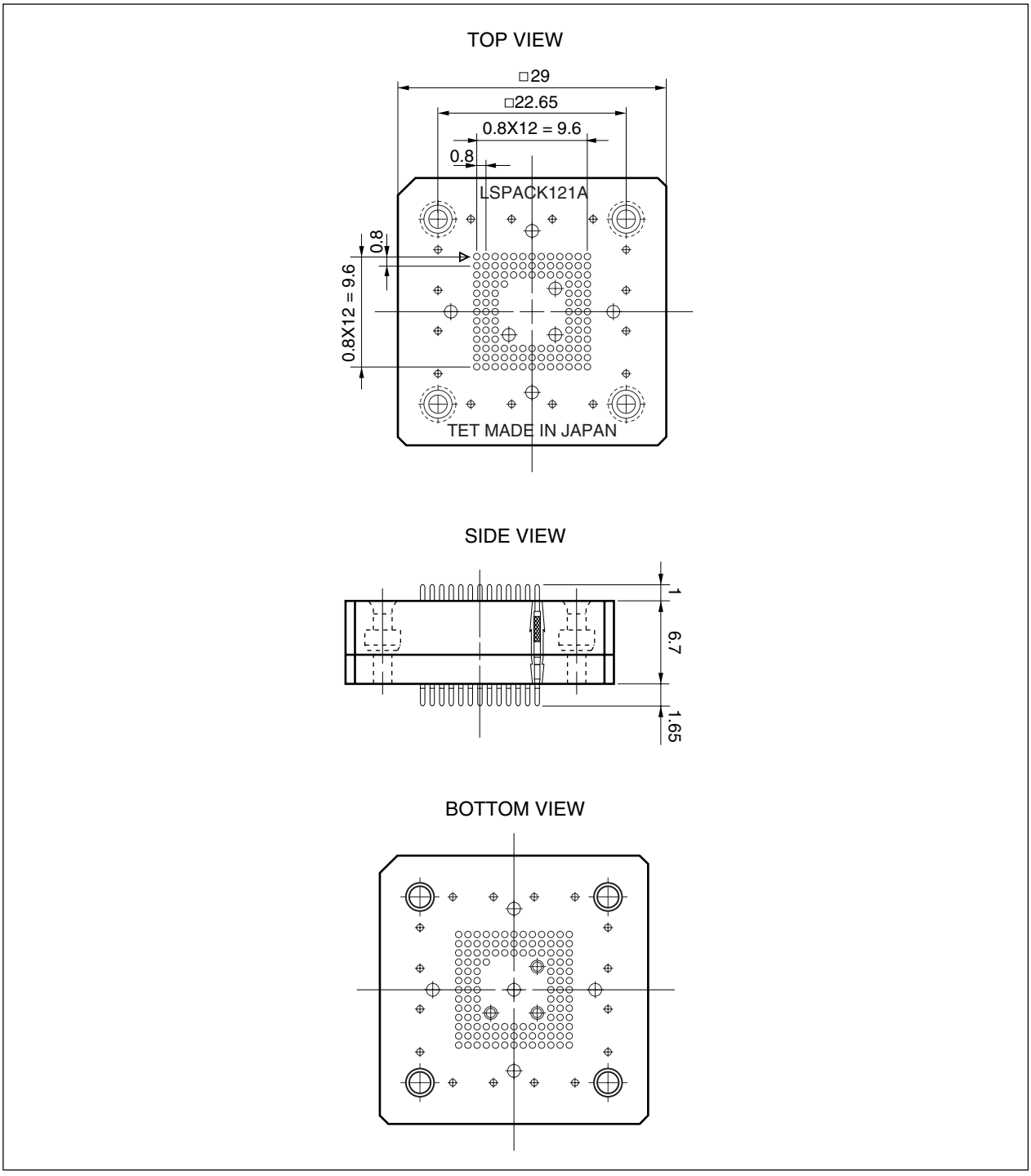


BOTTOM VIEW



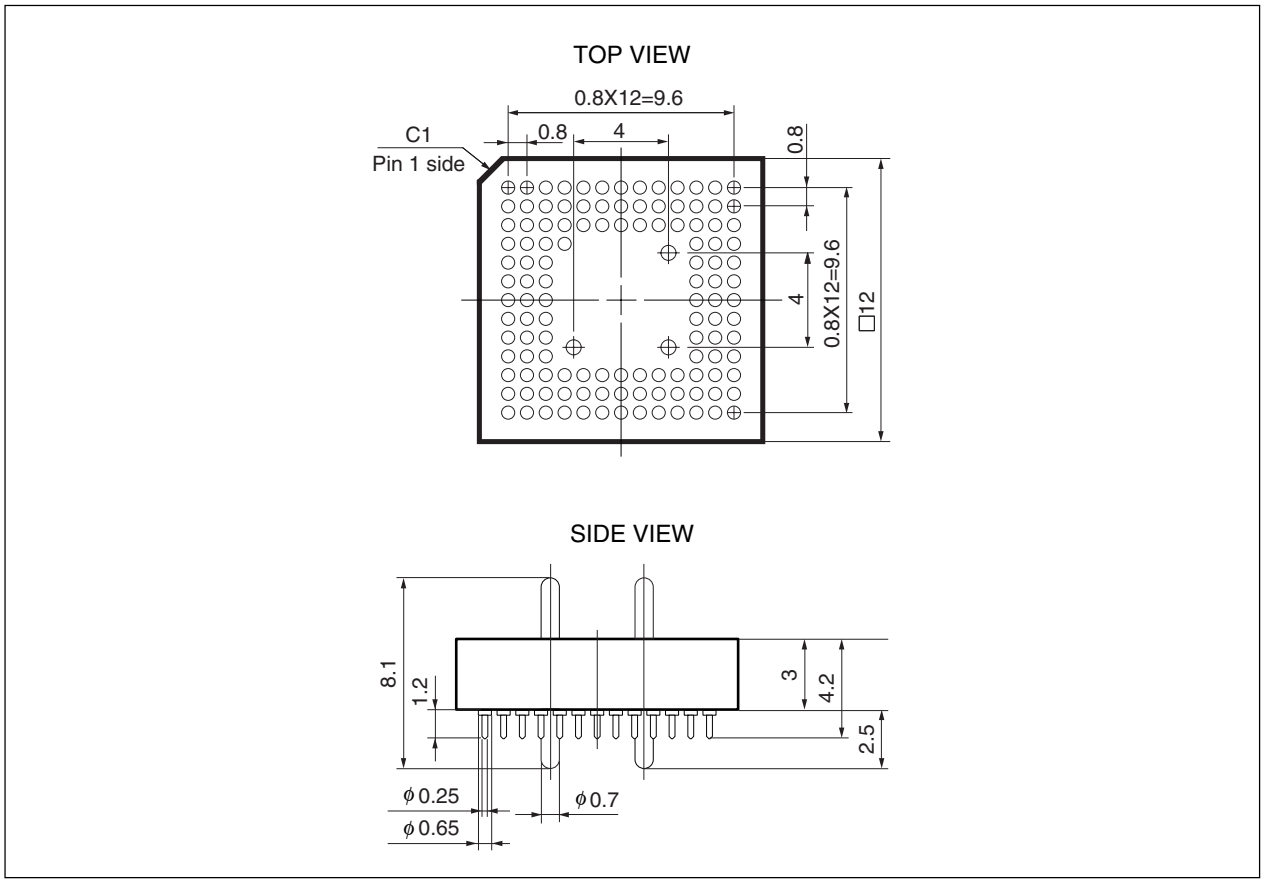
Remark CSICE121A1312N03 is a product of TOKYO ELETECH CORPORATION.

(5) LSPACK121A1312N01 (unit: mm)



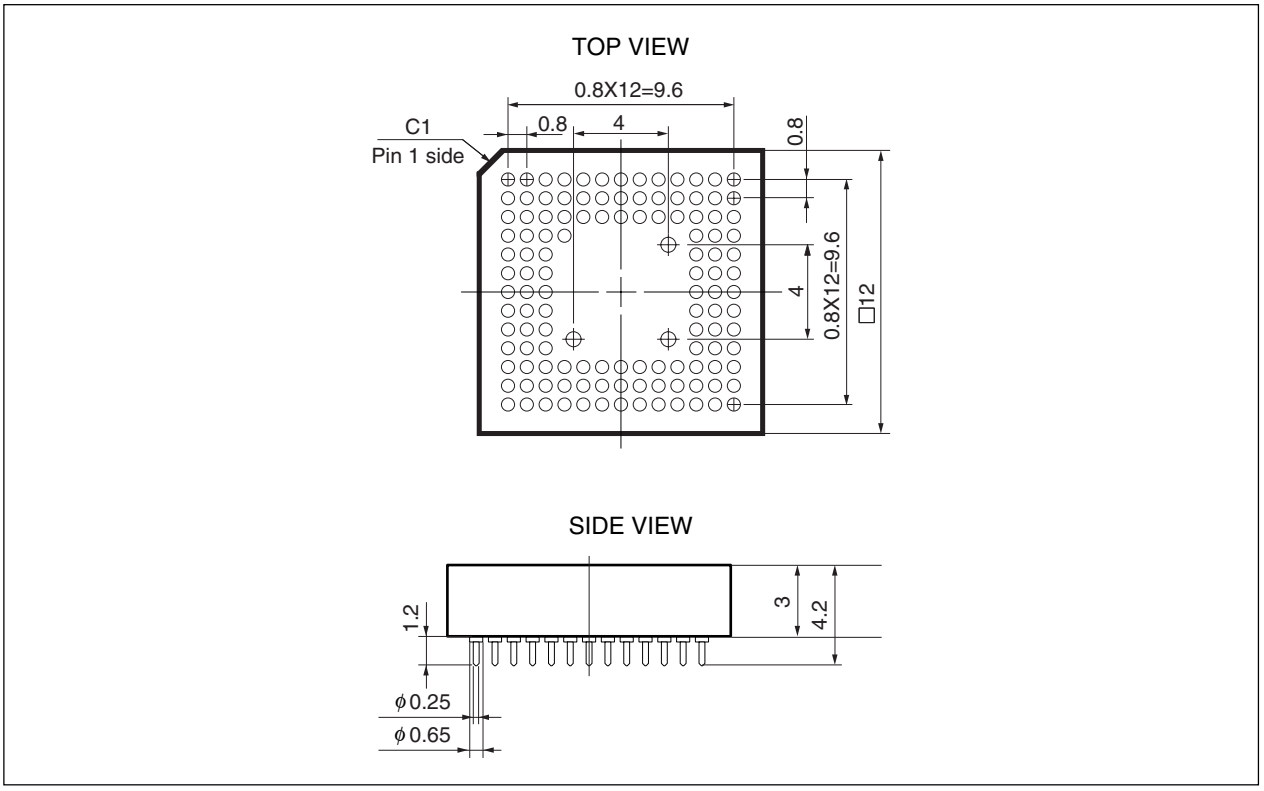
Remark LSPACK121A1312N01 is a product of TOKYO ELETECH CORPORATION.

(6) CSSOCKET121A1312N01 (unit: mm)



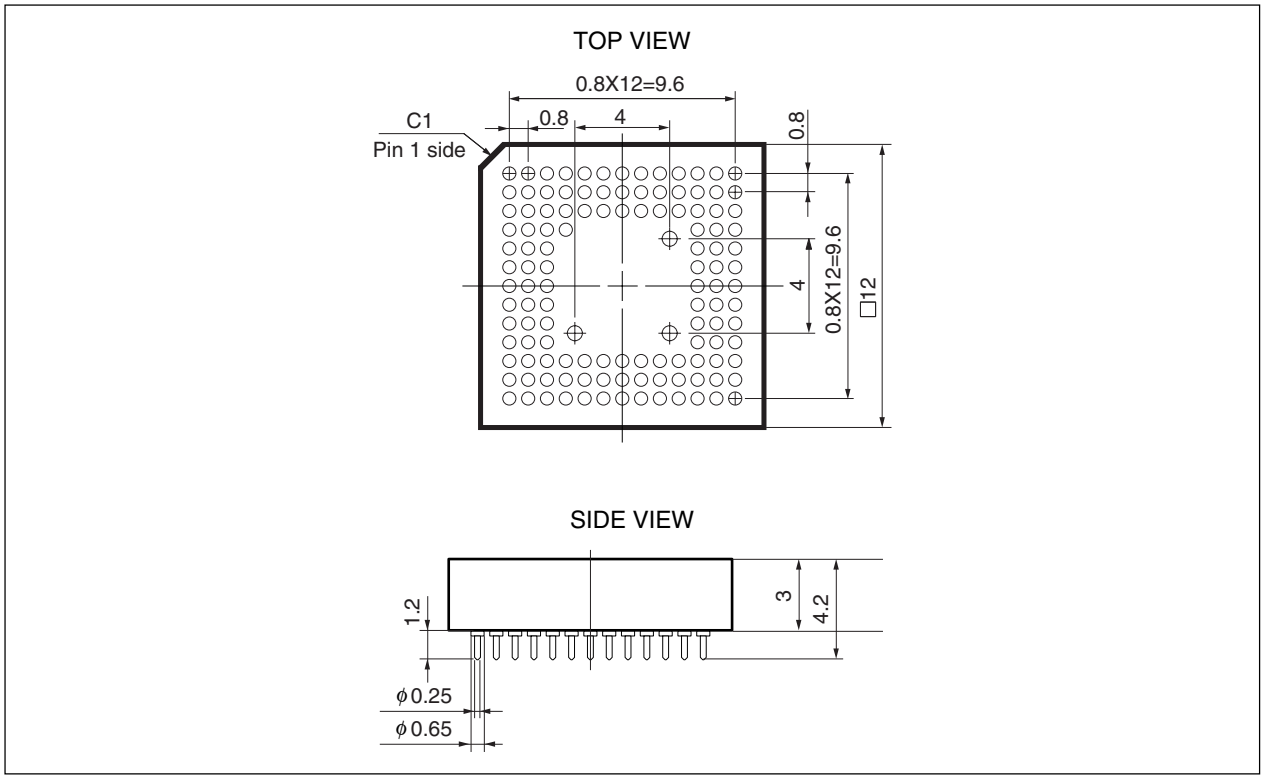
Remark CSSOCKET121A1312N01 is a product of TOKYO ELETECH CORPORATION.

(7) CSSOCKET121A1312N01N (unit: mm)



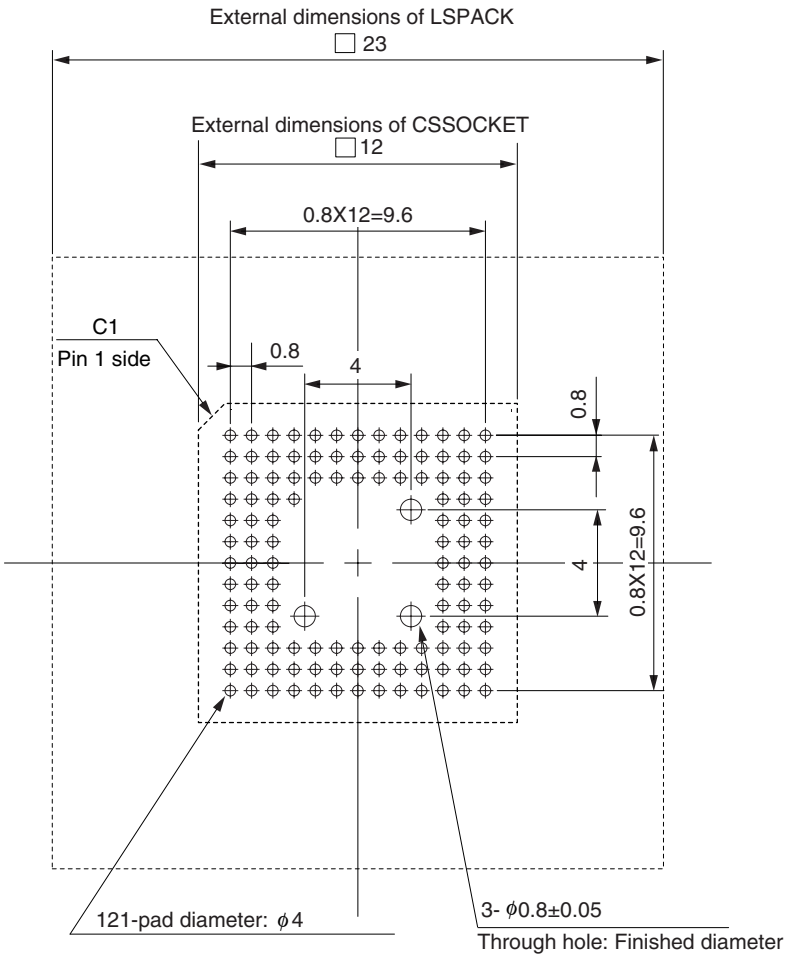
Remark CSSOCKET121A1312N01N is a product of TOKYO ELETECH CORPORATION.

(8) CSSOCKET121A1312N01S1 (unit: mm)



Remark CSSOCKET121A1312N01S1 is a product of TOKYO ELETECH CORPORATION.

(9) CSSOCKET121A1312N01 (foot pattern) (unit: mm)

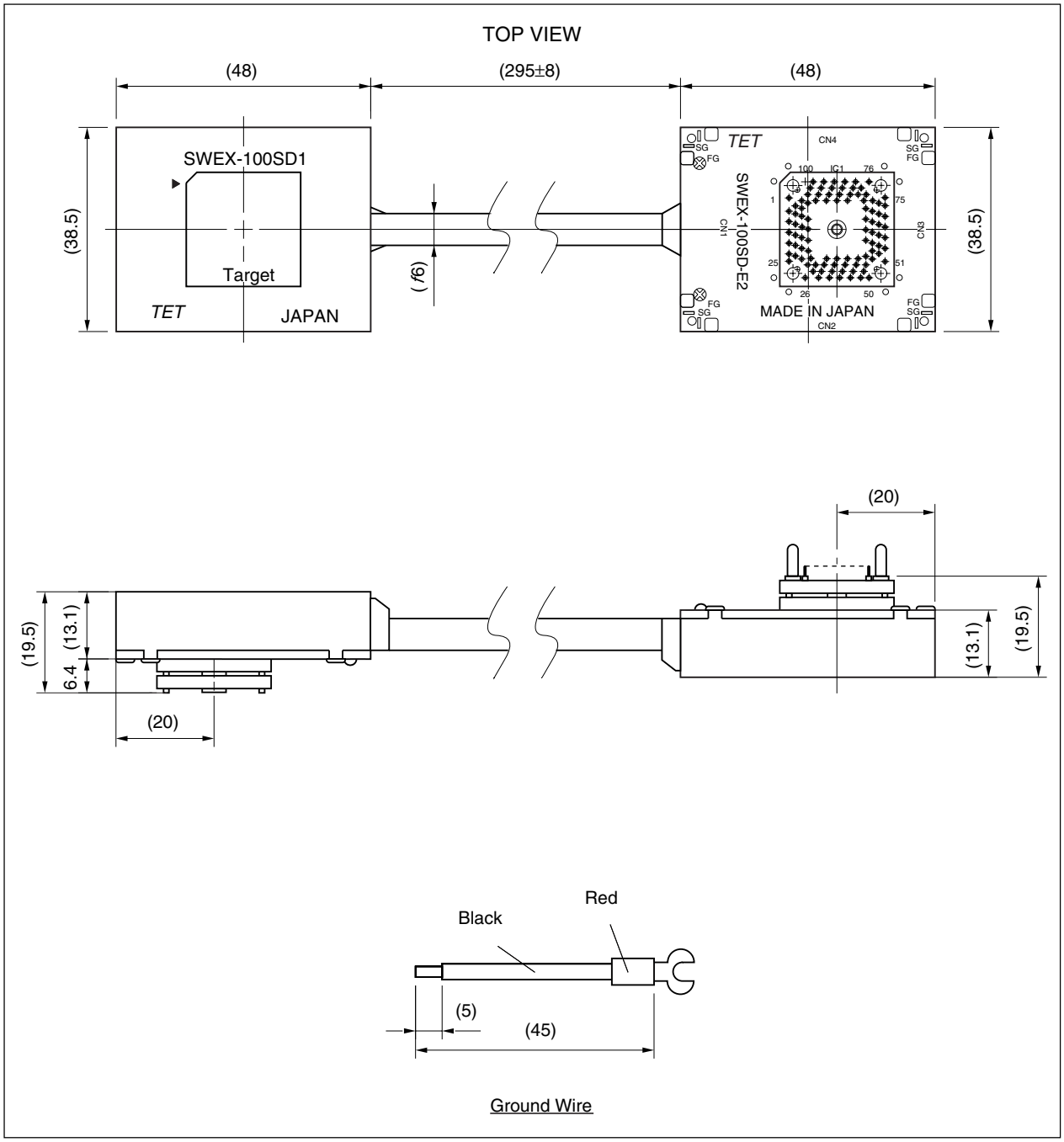


Remarks 1. After CSSOCKET has been fixed on the board by soldering, it is recommended to solder the guide pin of the connector from the lower side of the board or to fix the portion around the connector with resin for reinforcement.

2. The soldering reflow conditions are the same as for the CSPACK.

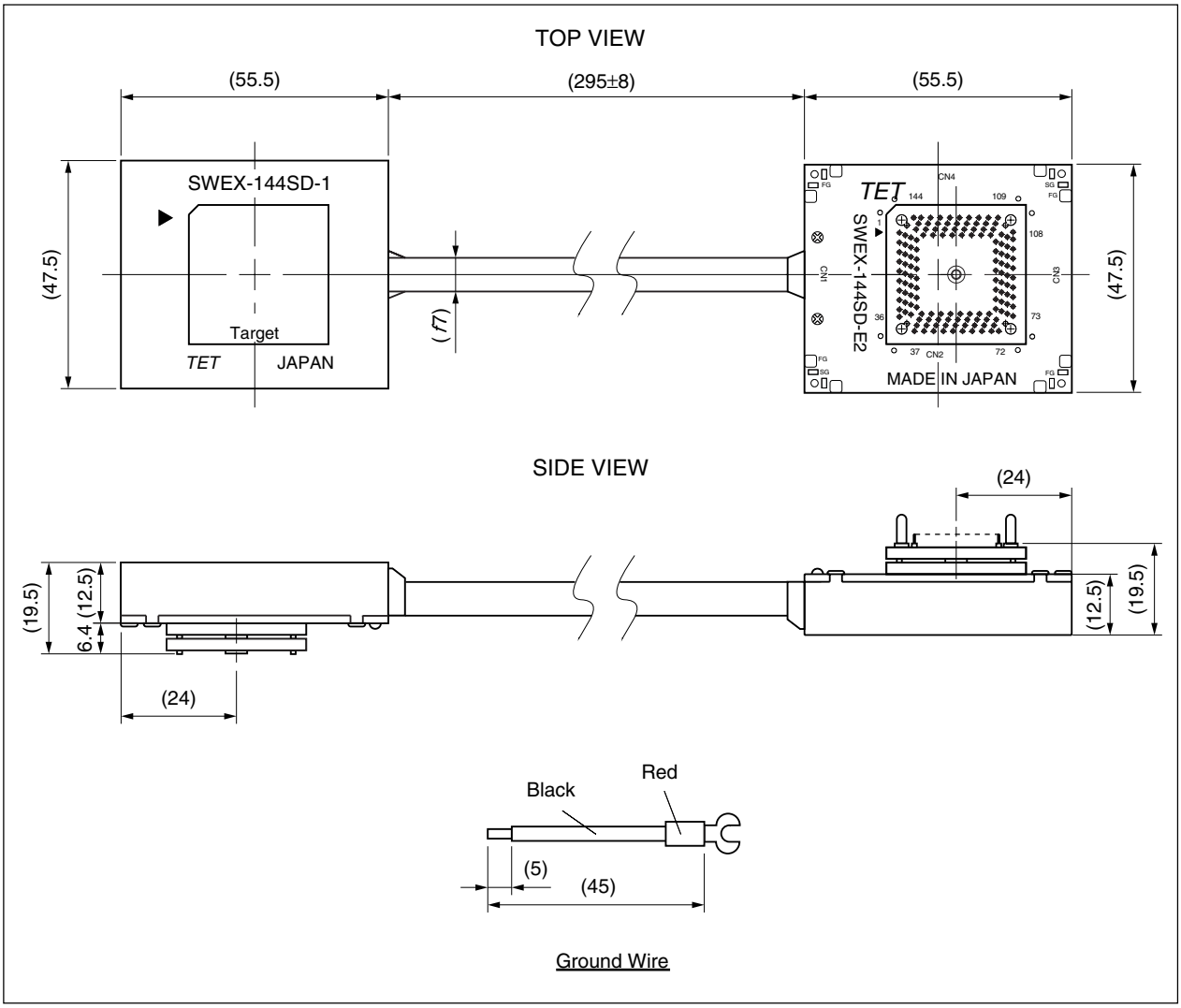
Remark CSSOCKET121A1312N01 is a product of TOKYO ELETECH CORPORATION.

(10) SWEX-100SD-1 (unit: mm)



Remark SWEX-100SD-1 is a product of TOKYO ELETECH CORPORATION.

(11) SWEX-120SE-1 (unit: mm)



Remark SWEX-120SE-1 is a product of TOKYO ELETECH CORPORATION.