

## 128K x 8 Static RAM

### Features

- High speed
  - $t_{AA} = 12$  ns
- Low active power
  - 495 mW (max.)
- Low CMOS standby power
  - 11 mW (max.) (L Version)
- 2.0V Data Retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{OE}$  options
- CY7C109B is available in standard 400-mil-wide SOJ and 32-pin TSOP type I packages. The CY7C1009B is available in a 300-mil-wide SOJ package

### Functional Description<sup>[1]</sup>

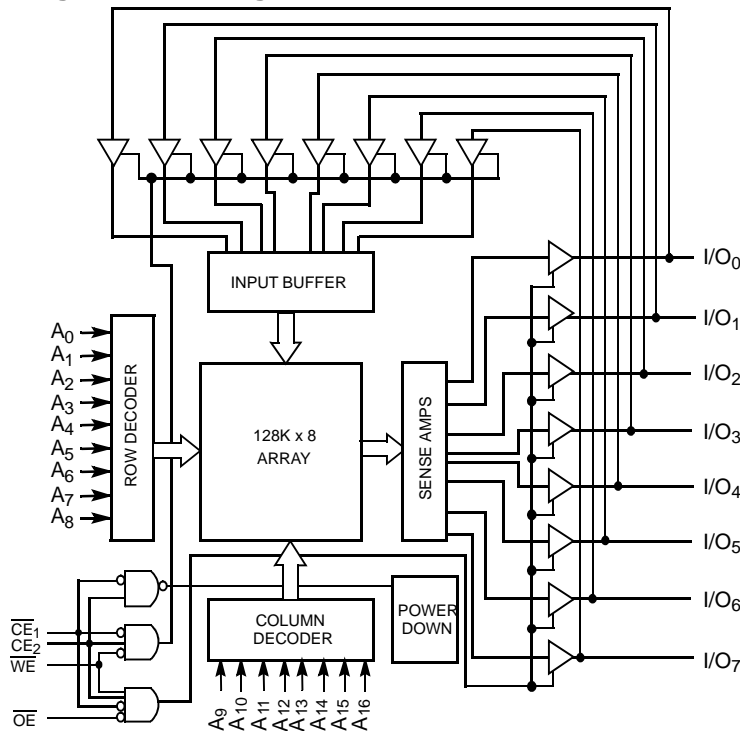
The CY7C109B/CY7C1009B is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}_1$ ), an active HIGH Chip Enable ( $CE_2$ ), an active LOW Output Enable ( $\overline{OE}$ ), and tri-state drivers. Writing to the device is accomplished by taking Chip Enable One ( $\overline{CE}_1$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW and Chip Enable Two ( $CE_2$ ) input HIGH. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ).

Reading from the device is accomplished by taking Chip Enable One ( $\overline{CE}_1$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) and Chip Enable Two ( $CE_2$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

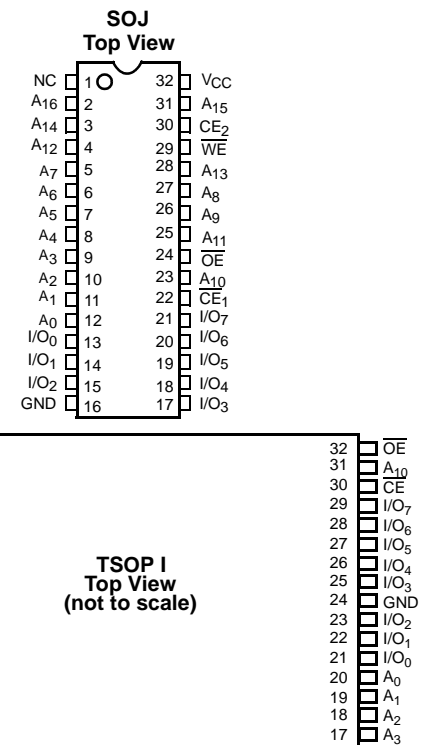
The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW).

CY7C109B is available in standard 400-mil-wide SOJ and 32-pin TSOP type I packages. The CY7C1009B is available in a 300-mil-wide SOJ package. The CY7C109B and CY7C1009B are functionally equivalent in all other respects

### Logic Block Diagram



### Pin Configurations<sup>[2]</sup>



#### Note:

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).
2. NC pins are not connected on the die.

**Selection Guide**

	7C109B-12 7C1009B-12	7C109B-15 7C1009B-15	7C109B-20 7C1009B-20	Unit
Maximum Access Time	12	15	20	ns
Maximum Operating Current	90	80	75	mA
Maximum CMOS Standby Current	10	10	10	mA
Maximum CMOS Standby Current (L)		2		mA

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature ..... -65°C to +150°C
- Ambient Temperature with Power Applied ..... -55°C to +125°C
- Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[3]</sup> .... -0.5V to +7.0V
- DC Voltage Applied to Outputs in High Z State<sup>[3]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V
- DC Input Voltage<sup>[3]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

- Current into Outputs (LOW)..... 20 mA
- Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)
- Latch-Up Current..... >200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	7C109B-12 7C1009B-12		7C109B-15 7C1009B-15		7C109B-20 7C1009B-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[3]</sup>		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	-1	+1	-1	+1	µA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	-5	+5	µA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		90		80		75	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	Max. V <sub>CC</sub> ; CE <sub>1</sub> ≥ V <sub>IH</sub> or CE <sub>2</sub> ≤ V <sub>IL</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		45		40		30	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> ; CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.3V, or CE <sub>2</sub> ≤ 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0		10		10		10	mA
			L				2		

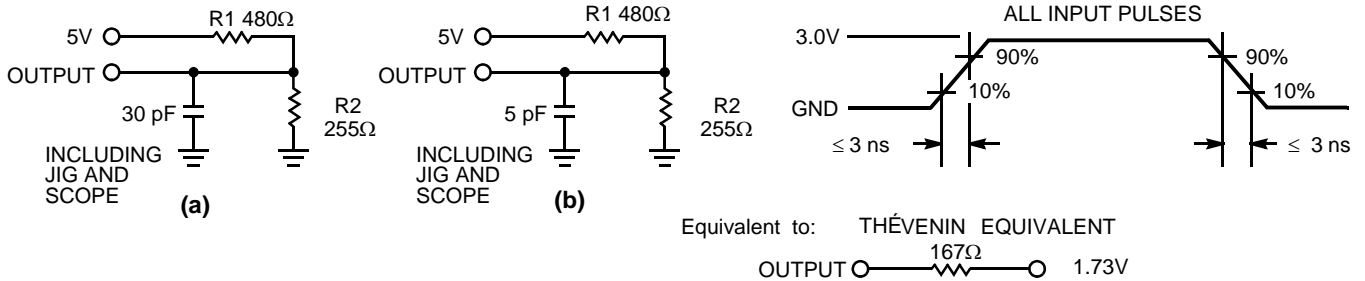
**Capacitance<sup>[4]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	9	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**Notes:**

- 3. Minimum voltage is -2.0V for pulse durations of less than 20 ns.
- 4. Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**



**Switching Characteristics<sup>[5]</sup>**

Parameter	Description	7C109B-12 7C1009B-12		7C109B-15 7C1009B-15		7C109B-20 7C1009B-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>								
$t_{RC}$	Read Cycle Time	12		15		20		ns
$t_{AA}$	Address to Data Valid		12		15		20	ns
$t_{OHA}$	Data Hold from Address Change	3		3		3		ns
$t_{ACE}$	$\overline{CE}_1$ LOW to Data Valid, $CE_2$ HIGH to Data Valid		12		15		20	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		6		7		8	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	0		0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		6		7		8	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW to Low Z, $CE_2$ HIGH to Low Z <sup>[7]</sup>	3		3		3		ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH to High Z, $CE_2$ LOW to High Z <sup>[6, 7]</sup>		6		7		8	ns
$t_{PU}$	$\overline{CE}_1$ LOW to Power-Up, $CE_2$ HIGH to Power-Up	0		0		0		ns
$t_{PD}$	$\overline{CE}_1$ HIGH to Power-Down, $CE_2$ LOW to Power-Down		12		15		20	ns
<b>Write Cycle<sup>[8]</sup></b>								
$t_{WC}$	Write Cycle Time <sup>[9]</sup>	12		15		20		ns
$t_{SCE}$	$\overline{CE}_1$ LOW to Write End, $CE_2$ HIGH to Write End	10		12		15		ns
$t_{AW}$	Address Set-Up to Write End	10		12		15		ns
$t_{HA}$	Address Hold from Write End	0		0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	10		12		12		ns
$t_{SD}$	Data Set-Up to Write End	7		8		10		ns
$t_{HD}$	Data Hold from Write End	0		0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	3		3		3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		6		7		8	ns

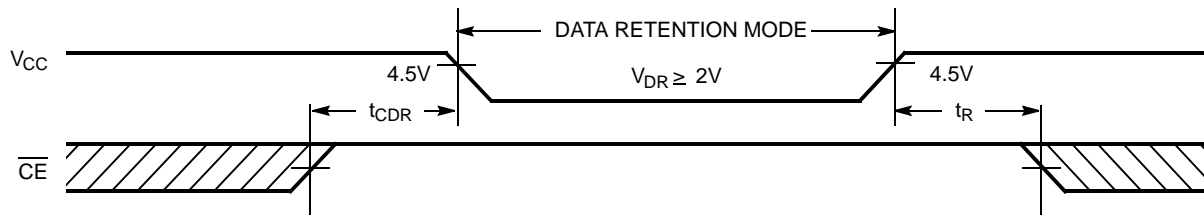
**Notes:**

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW.  $\overline{CE}_1$  and  $\overline{WE}$  must be LOW and  $CE_2$  HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Data Retention Characteristics** Over the Operating Range (Low Power version only)

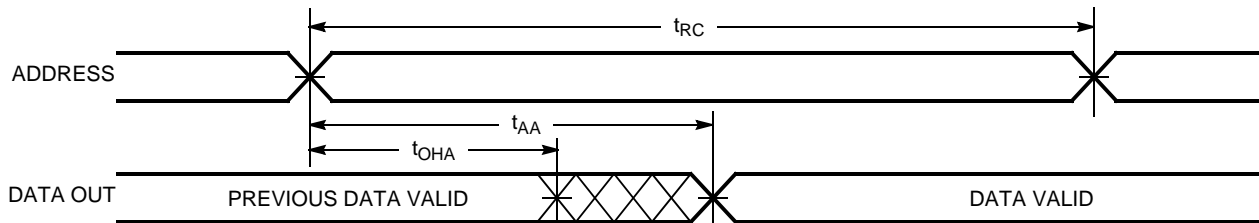
Parameter	Description	Conditions	Min.	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention	No input may exceed $V_{CC} + 0.5V$	2.0		V
$I_{CCDR}$	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$ , $CE_1 \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$ ,		150	$\mu A$
$t_{CDR}$	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	0		ns
$t_R$	Operation Recovery Time		200		$\mu s$

**Data Retention Waveform**

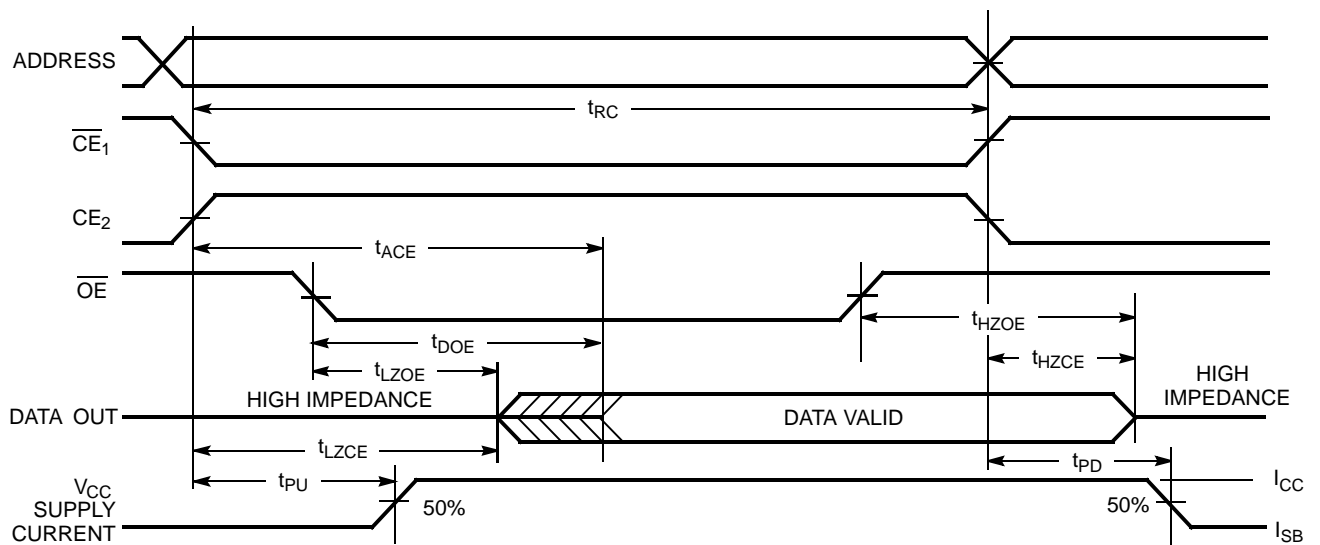


**Switching Waveforms**

**Read Cycle No. 1**<sup>[10, 11]</sup>



**Read Cycle No. 2 (OE Controlled)**<sup>[11, 12]</sup>

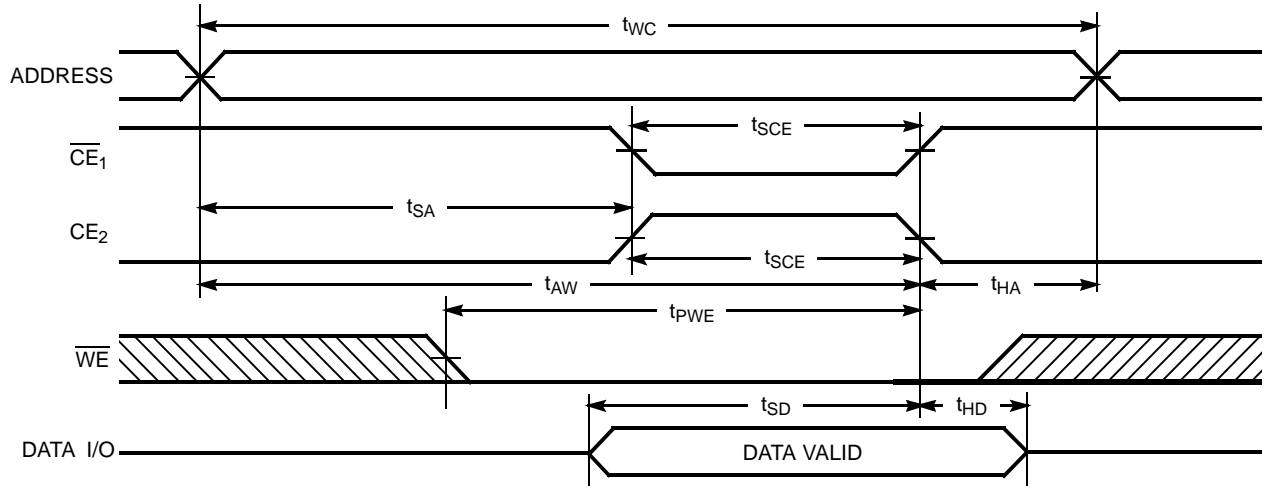


**Notes:**

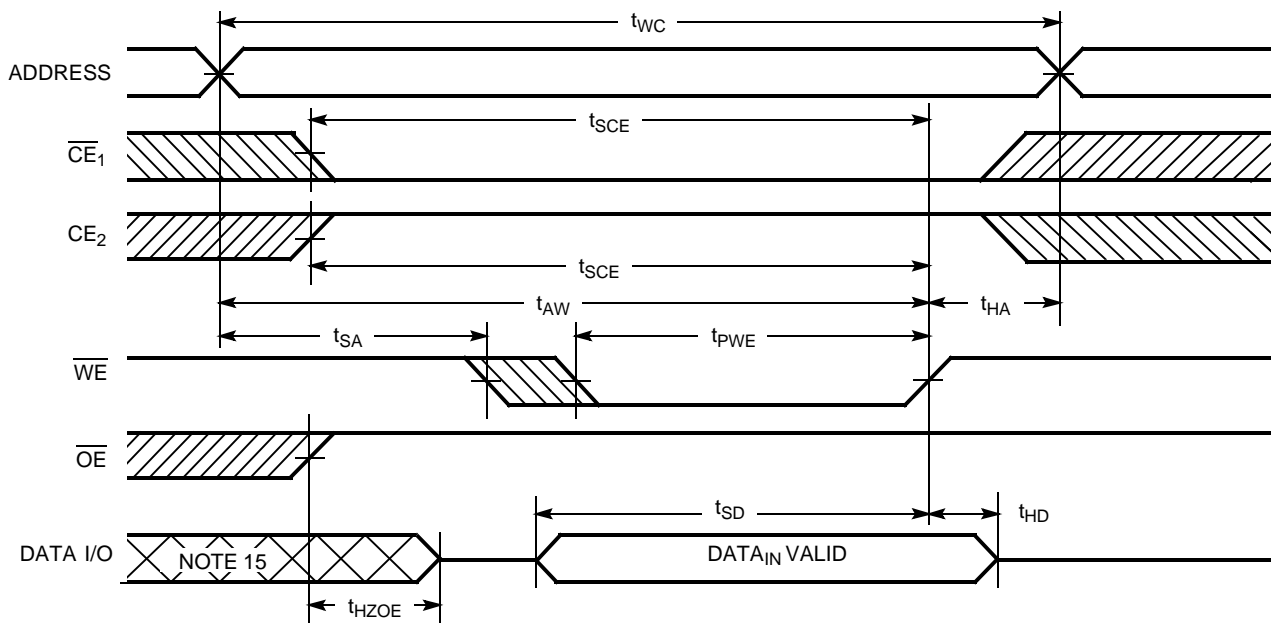
- 10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
- 11.  $\overline{WE}$  is HIGH for read cycle.
- 12. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.

**Switching Waveforms** (continued)

**Write Cycle No. 1 ( $\overline{CE}_1$  or  $CE_2$  Controlled)**<sup>[13, 14]</sup>



**Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)**<sup>[13, 14]</sup>

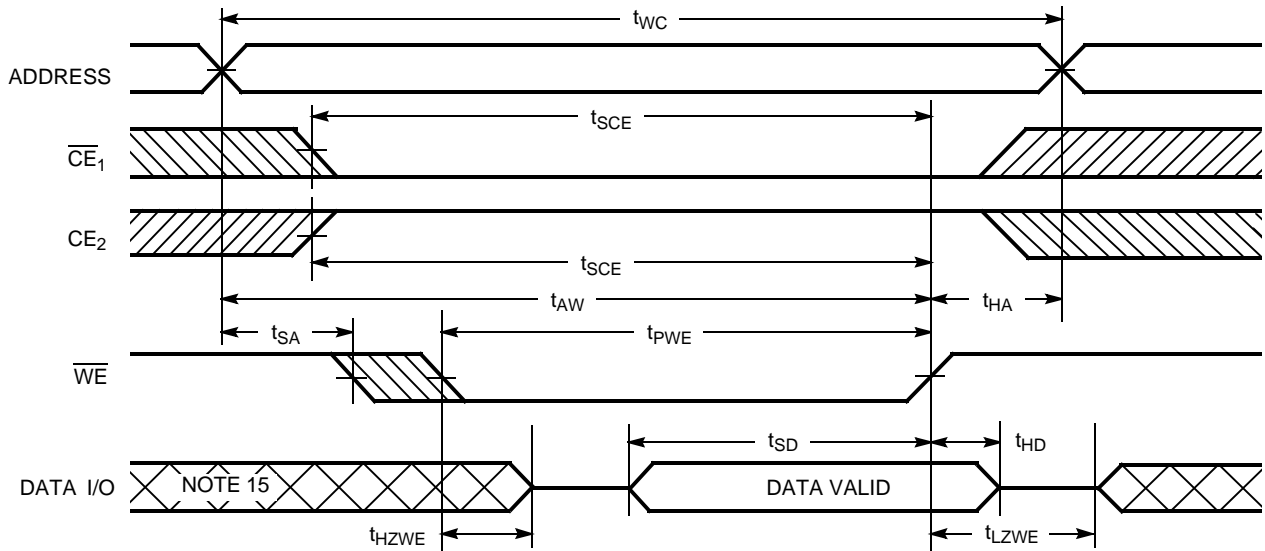


**Notes:**

- 13. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 14. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
- 15. During this period the I/Os are in the output state and input signals should not be applied.

**Switching Waveforms** (continued)

**Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[14]</sup>**



**Truth Table**

$\overline{\text{CE}}_1$	$\overline{\text{CE}}_2$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O <sub>0</sub> -I/O <sub>7</sub>	Mode	Power
H	X	X	X	High Z	Power-Down	Standby ( $I_{\text{SB}}$ )
X	L	X	X	High Z	Power-Down	Standby ( $I_{\text{SB}}$ )
L	H	L	H	Data Out	Read	Active ( $I_{\text{CC}}$ )
L	H	X	L	Data In	Write	Active ( $I_{\text{CC}}$ )
L	H	H	H	High Z	Selected, Outputs Disabled	Active ( $I_{\text{CC}}$ )

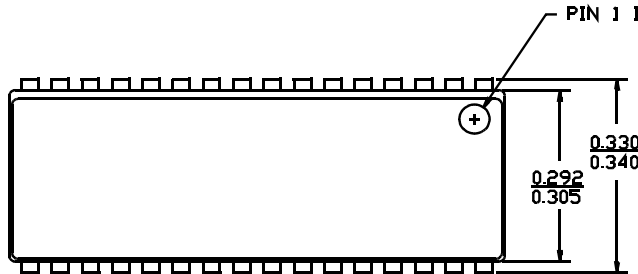
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C109B-12VC	51-85033	32-pin (400-Mil) Molded SOJ	Commercial
	CY7C1009B-12VC	51-85041	32-pin (300-Mil) Molded SOJ	
	CY7C109B-12ZC	51-85056	32-pin TSOP Type I	
	CY7C109B-12ZXC		32-pin TSOP Type I (Pb-Free)	
15	CY7C109BL-15VC	51-85033	32-pin (400-Mil) Molded SOJ	Commercial
	CY7C109B-15VC		32-pin (400-Mil) Molded SOJ	
	CY7C109B-15VXC		32-pin (400-Mil) Molded SOJ (Pb-Free)	
	CY7C1009B-15VC	51-85041	32-pin (300-Mil) Molded SOJ	
	CY7C1009B-15VXC		32-pin (300-Mil) Molded SOJ (Pb-Free)	
	CY7C109B-15ZC	51-85056	32-pin TSOP Type I	
	CY7C109B-15ZXC		32-pin TSOP Type I (Pb-Free)	
	CY7C109B-15VI	51-85033	32-pin (400-Mil) Molded SOJ	Industrial
	CY7C1009B-15VI	51-85041	32-pin (300-Mil) Molded SOJ	
20	CY7C109B-20ZC	51-85056	32-pin TSOP Type I	Commercial
	CY7C1009B-20VC	51-85041	32-pin (300-Mil) Molded SOJ	
	CY7C109B-20VI	51-85033	32-pin (400-Mil) Molded SOJ	Industrial

Please contact local sales representative regarding availability of parts

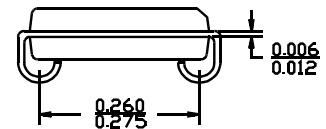
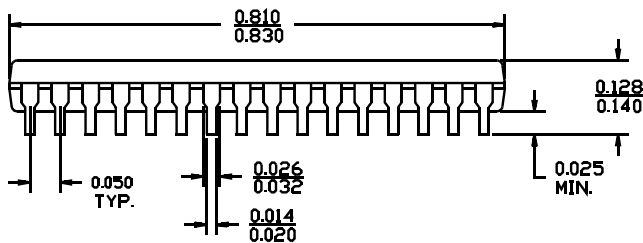
**Package Diagrams**

**32-pin (300-Mil) Molded (51-85041)**



DIMENSIONS IN INCHES MIN.  
MAX.

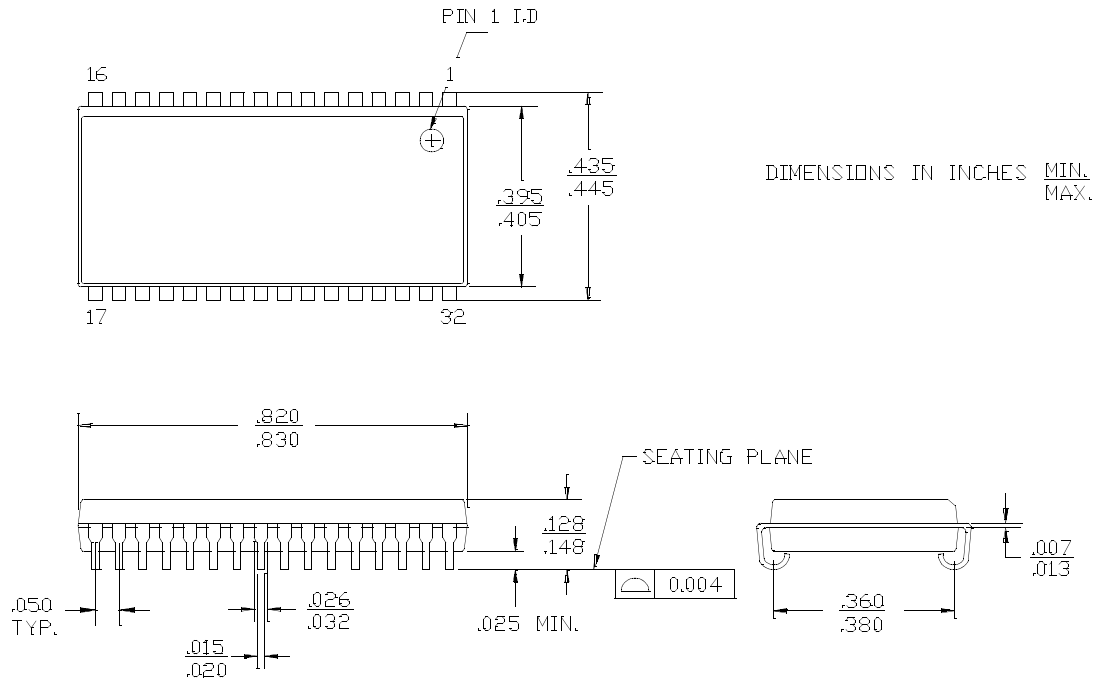
LEAD COPLANARITY 0.004 MAX.



51-85041-\*A

**Package Diagrams** (continued)

**32-pin (400-Mil) Molded SOJ (51-85033)**

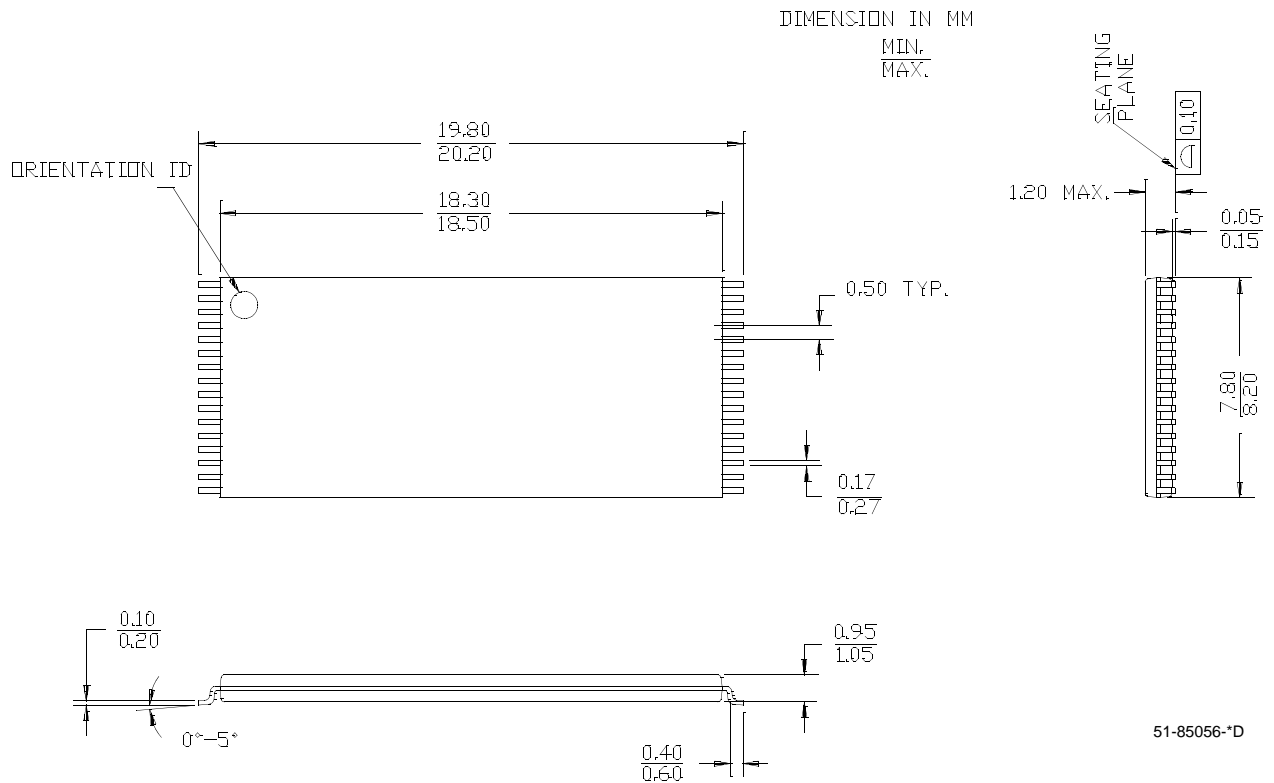


51-85033-B



Package Diagrams (continued)

**32-pin TSOP Type I (8 x 20 mm) (51-85056)**



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**Document History Page**

<b>Document Title: CY7C109B/CY7C1009B 128K x 8 Static RAM</b>				
<b>Document Number: 38-05038</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	106832	09/22/01	SZV	Change from Spec number: 38-00971 to 38-05038
*A	116467	09/16/02	CEA	Added applications foot note to data sheet, page 1
*B	397875	See ECN	NXR	Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Updated the Ordering Information Table on page 7
*C	493543	See ECN	NXR	Removed 25 ns and 35 ns speed bin from product offering Added note# 2 on page# 1 Changed the description of $I_{IX}$ from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed $I_{OS}$ parameter from DC Electrical Characteristics table Updated the Ordering Information Table