Electrical Specifications

Absolute Maximum Ratings*

DC Supply Voltage, V_{CC} ..... -0.5V to +7.0V

DC Programming Voltages, V_{PP}, V_{PB} ..... -0.5 to +10.5V

DC Input Voltage, V_I ..... -0.5V to Vcc +0.5V

DC Input Clamp Current, I_{IK} (V_I<0 or V_I>V_{DD}) ..... ± 20mA

DC Output Current Per Pin (V_O = 0 to V_{CC}) ..... ± 25mA

Storage Temperature, T_{STG}

Ceramic Packages ..... -65°C to +150°C

Plastic Packages ..... -40°C to +125°C

* Stresses beyond these ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* section of this specification is not implied. Exposure to conditions exceeding the absolute maximum ratings for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	Commercial Industrial & Military	4.75 4.5	5.25 5.5	V
V_I	Input Voltage		0	V_{CC}	V
V_O	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature	Commercial Industrial Military	0 -40 -55	+70 +85 +125	°C
$t_{R,F}$	Input Rise & Fall Times	Normal Inputs Clock Inputs		250 100	ns

Timing

Propagation delays in the CP20K FPGAs depend upon the physical implementation of the circuit. After a design has gone through the layout process, the Crosspoint Design System uses layout and cell library data to model circuit timing and provide information necessary to accurately model both propagation delay and timing constraint parameters.

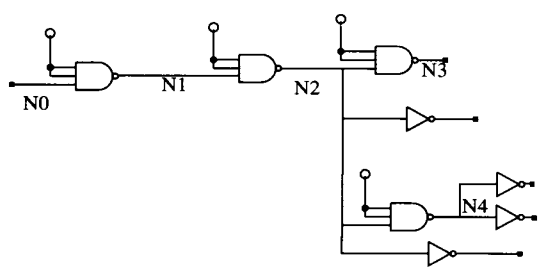
Prior to layout, data provided in this manual can be used to estimate what these timing parameters will be in the completed circuit. This section provides the information needed to correctly interpret timing data and to apply it to the estimation and analysis of circuit timing performance.

Timing Behavior of FPGA Circuits

In order to properly analyze the timing behavior of a circuit implemented in a CP20K array it is necessary to account for the effects of routing interconnect load capacitance and resistance and the intrinsic delay of signals through library components in the design.

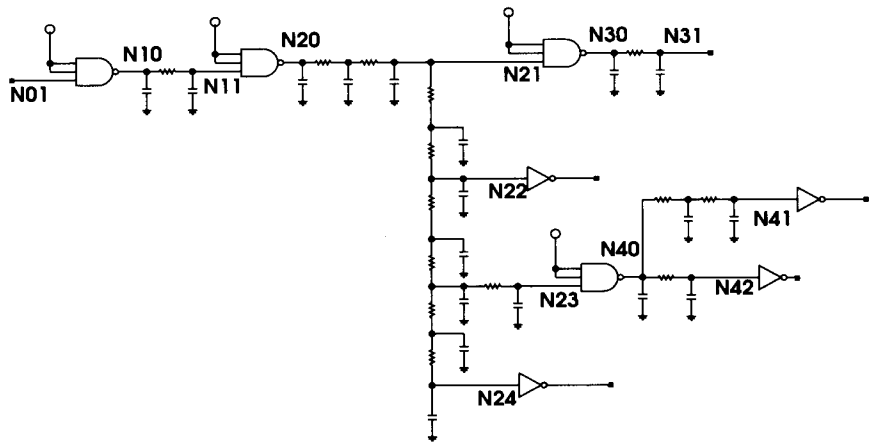
To understand the effect of resistance on a digital circuit, consider the circuit shown in Figure 1-20.

Figure 1-20
Logical schematic



The effect of resistance in the interconnect is to split a single logical net in the digital design into a number of sub-nets, as illustrated in Figure 1-21.

Figure 1-21
Splitting logical nets into physical nets

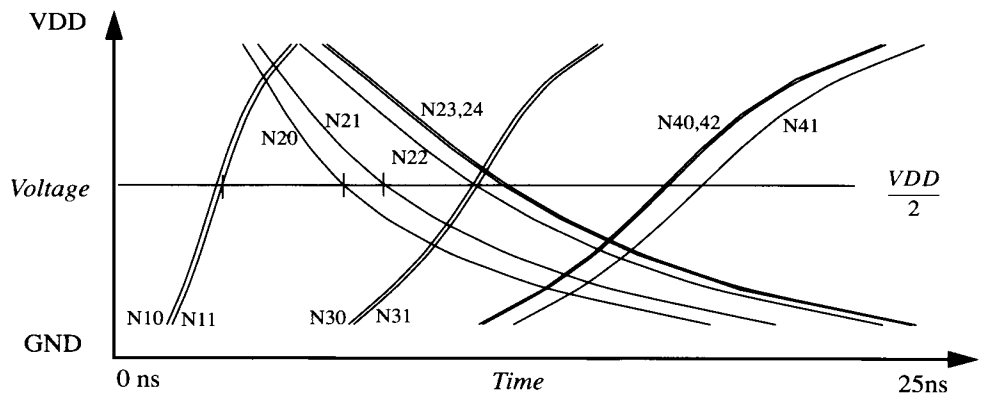


In Figure 1-20, net *N10* and *N11* are subnets formed from a single net (corresponding to the logical net *N1*) by the introduction of a resistor. Similarly, logical nets *N2*, *N3* and *N4* are split into the subnets indicated in Figure 1-21 by the introduction of resistors.

In a CP20K circuit, the principal cause of resistance in interconnect is the presence of antifuses. Except for very long routing segments, wire resistance may be ignored in the interconnect model. Thus, most nets split into interconnect networks with resistors representing antifuses and capacitors representing wire segments.

A SPICE simulation of the above circuit reveals that there is a delay between the signals arriving at each point on an interconnect network. The signal waveforms are plotted (between 10% and 90% of V_{DD}) for each node labeled in Figure 1-22.

Figure 1-22
Actual signal waveforms



Delays are measured by taking the difference between the times when the waveforms of interest cross the voltage $V_{DD}/2$. The delay of the 3-input **NAND** gate between the gate input at node *N11* and the gate output at node *N20* as well as the net delay between nodes *N20* and *N21* illustrate this point.

In summary, the delay through a stage of logic essentially consists of four components:

- The *intrinsic delay* from the cell input pin to the cell output pin that would be observed if the loading or capacitance on both input and output pins were zero.
- The *output transition time* or additional delay through the cell (from input pin to output pin) which is due to the effects of loading on the output pin. This is modeled as the product of an output drive resistance and the output net capacitance.
- The *input slew time* or change in delay through the cell which is due to the effects of loading on the input pin. Essentially, this is the difference between the time at which the signal on the input pin crosses 50% of V_{DD} (the reference point for delay measurement) and the time at which the signal reaches the voltage which physically initiates a transition of the gate (logic threshold voltage). The slew time can be either positive or negative. This is modeled as the product of a slew-rate

factor and a time-constant which is characteristic of the signal on the input pin. The time-constant is approximately the sum of the transition time of the previous stage and the net delay associated with the input net.

- The *net delay* is the time it takes a signal to propagate from a cell output pin, through interconnect wiring, to the next stage input pin. This is modeled by analyzing the RC network representing the interconnect associated with each logical net as described below.

Estimating Delay Prior to Layout

While timing is not determined until after layout, reasonable estimates can be made prior to layout using the *macrocell datasheets*. A much simplified model is used based upon some carefully chosen assumptions and statistical analysis of post-layout timing obtained from several completed FPGA designs.

The key features of the pre-layout timing estimation model are:

- Propagation delay is modeled as the sum of an intrinsic component and a load dependent component. Datasheets list values for intrinsic delay and for the drive factor for each macrocell timing arc (see Equation 1-1).

$$Delay = Intrinsic + (Drive \cdot Load) \qquad \text{(EQ1- 1)}$$

- Capacitance is given in units of standard loads. Each datasheet lists the load for each pin. (A standard load is approximately that of a unit strength inverter.)
- A *wire load* model which lists expected interconnect capacitance, in units of standard load, as a function of net fanout is given in Table 1-7. Add the wire load to that of each pin on the cell's fan-out to obtain the total load for Equation 1-1.
- Net delays, time constants and slew rate effects are accounted for, on a statistical basis only, by modification of cell intrinsic and drive factors and of wire load values. Since these modifications have already been applied to the appropriate tables, they are transparent to the user.
- Derating factors are applied after delays are computed at nominal conditions. Derating factors are either the same for all cells or are given different values for I/O buffers than for internal cells.

Interconnect Wire Load

Table 1-7 tabulates estimated wire capacitance as a function of fanout in standard load units (1 standard load = 0.488 pF) for place and route of typical designs and for optimized layout of critical portions of a design.

Table 1-7 Wire Load per Fanout*

Fanout	Optimized Layout (std load units)	Typical (std load units)
1	2.5	3.6
2	3.5	5.9
3	4.6	8.2
4	5.8	10.5
5	7.2	12.8
6	8.8	15.1
7	10.6	17.4
8	13	19.7
9	16	22.0
10	20	24.2
11	-	26.5
12	-	28.8
13	-	31.1
14	-	33.4
15	-	35.7
16	-	38.0
17	-	40.3
18	-	42.6
19	-	44.9
20	-	47.2
21	-	49.5
22	-	51.8
23	-	54.1
24	-	56.4
25	-	58.7

* Use zero wireload for clock buffers.

It is statistically derived from the analysis of a variety of circuits. Actual wire load may vary significantly from that listed.

Loading for clock distribution networks is included in clock buffer intrinsic timing. For clock buffers, zero wire-load must be used regardless of fanout.

Derating Timing for Best Case/Worst Case Analysis

The timing data in the macrocell datasheets in this manual is for *nominal* conditions. Nominal is defined as worst-case process conditions for -1 speed grade parts (see the following section for a description of speed bins), nominal power supply voltage (5.0 V) and junction temperature of 25 °C. This section describes how to modify estimated delay for other than *nominal* conditions.

Derating timing after it is determined at nominal conditions by using Equation 1-2.

$$delay = (f_{temp} \cdot f_{process} \cdot f_{voltage}) \cdot (delay)_{nominal} \qquad \text{(EQ1- 2)}$$

Temperature Derating

The junction temperature will typically be 10 to 40 °C above ambient temperature, depending upon package properties and chip power dissipation. Table 1-8 may be used in most cases as a reasonable guide to the highest and lowest junction temperatures that should be expected when designing to commercial and military specifications:

Table 1-8 Junction Temperatures Ranges for Commercial and Military Specifications

Specification Type	Junction Temperature
Commercial	0° C to 115 °C
Industrial	-40° C to 125 °C
Military	-55° C to 150 °C

The derating factor is determined using Equation 1-3.

$$f_{temp} = 1 + k_T (T_J - 25°C) \qquad \text{(EQ1- 3)}$$

where:

Table 1-9 Temperature K-Factors *(Preliminary)*

Cell Type	k_T
Internal Cells	0.0022 per °C
Pad Buffers	0.0022 per °C

Supply Voltage Derating

The voltage derating factors depend upon cell type and, for pad buffers, the transition type. They are listed in Table 1-10 for nominal (5.0V), commercial (4.75 to 5.25) and military (4.5 to 5.5) voltages.

Table 1-10 Voltage Derating Factors *(Preliminary)*

Cell Type	4.5 V_{CC}	4.75 V_{CC}	5.0 V_{CC}	5.25 V_{CC}	5.5 V_{CC}
Internal Cell	1.03	1.02	1.0	0.97	0.97
Output Buffer	1.08	1.04	1.0	0.96	0.93
Input Buffer, Falling Transition	1.05	1.02	1.0	0.98	0.95
Input Buffer, Rising Transition	1.02	1.01	1.0	0.99	0.98
Clock Buffer	1.04	1.02	1.0	0.98	0.96

Process Derating—Speed Bins and Worst/Best Case

Delay depends upon several process factors including transistor drive strength, capacitance and antifuse on-resistance which are fixed when a part is manufactured or, in the case of antifuse resistance, when the part is programmed. A Crosspoint customer may purchase parts which have been tested and qualified according to defined *speed-bins*. For each speed-bin, the FPGA designer may analyze timing under either *worst-case* or *best-case* process conditions.

The derating factors for best and worst case process conditions for each bin are listed in Table 1-11.

Table 1-11 Process Derating Factors *(Preliminary)*

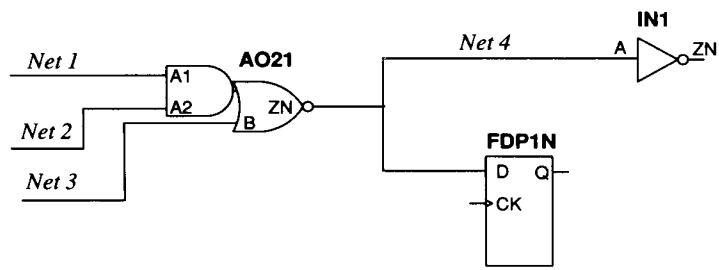
Speed Grade	Worst Case	Best Case
-0	1.4	0.9
-1	1.0	0.7

Estimating Delay Using the Macrocell Datasheets—An Example

The procedure to estimate delay is illustrated using the example in Figure 1-23. Estimation is made for the following conditions:

- 0 degrees C junction temperature
- 5.5 V supply voltage
- -0 speed grade, best case process.

Figure 1-23
Delay calculation example



Use the following steps to find delay:

1. Select a path in the design for analysis, noting all the *hard* macrocells and the fanout of each net in the path. (Soft macros must be decomposed into their hard-macro components.) The example requires the delay between *Net 1* and *Net 4* for the transition *Net 1* rising and *Net 4* falling.

2. Use Table 1-7 to determine the wire load for each net in the path. For clock nets use zero wire load. For output buffers the expected load capacitance should be known and there is no wire load. In this case the fan-out on *Net 4* is 2 and Table 1-7 gives a wire load of 5.9.

3. Use the *macrocell datasheets* to determine the pin loads for each input pin and add to the wire load to arrive at a total load for each net in the path. The example has a load of 1.0 for the IN1 and a load of 0.5 for pin D of FDP1N. Total load on *Net 4* is $5.9 + 1.0 + 0.5 = 7.4$ standard loads.

4. Use the *macrocell datasheets* to determine the delay for each macrocell in the path, given the net loads. For example, refer to the *macrocell datasheet for AO21* and find the entries in the Timing Parameter Table for the transition "A1(↑) to ZN(↓)". The delay may be determined in one of two ways:

   - Use the appropriate value found under the table heading *Delay Given Standard Load.* Either round-off the calculated load (7.4) to the nearest table entry (8.0) or interpolate. The example has a delay of 2.7 ns for a load of 8.
   - Calculate the delay using the intrinsic and drive values given in the table using Equation 1-1. In this case, the delay is $1.42 + 0.165 \times 7.4 = 2.64$ nano-seconds.

   Repeat this procedure for each macrocell in the path of interest and sum the delays. In this example, only a single-stage path is illustrated; the total path delay is 2.6 ns (0.1 ns precision is sufficient).

5. Use Equation 1-3 and Table 1-9 to find the temperature derating factor. Note that the same derating factor is applied to all timing values for a given temperature. The example shows $f_T = 1 + 0.0022 \times (0 - 25) = 0.945$.

6. Use Table 1-10 to find the supply voltage derating. In this case $VCC = 5.5$, the example shows $f_V = 0.97$.

7. Use Table 1-11 to find the process derating. In the case of speed grade -0, best case is $f_P = 0.9$.

8. Multiply the timing values found in step 4 by the derating factors to find the final values. In this case, $2.64 \times 0.945 \times 0.97 \times 0.9 = 2.2$ nano-seconds.

The estimated delay sums the propagation times from cell input-pin to cell input-pin.

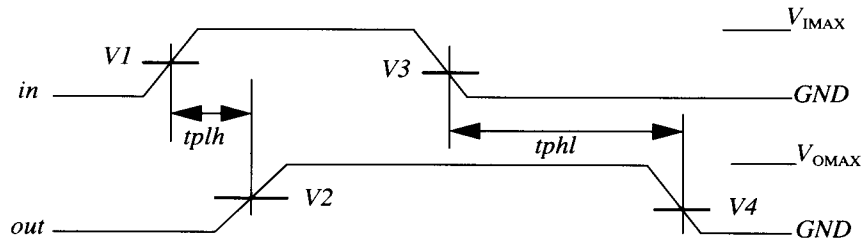
NOTE: In comparing estimated timing to post-layout delay calculator timing the delay calculator sums delays from output-pin to output-pin.

Pad Buffer Delay Measurement Conditions

Delay to and from internal pins of macrocells is measured at 50% of the internal supply voltage. Delay to and from the PAD pin of Pad Buffers and External Clock Buffers is measured as described in this section.

Figure 1-24 shows the propagation of a signal through a buffer from a buffer input to buffer output. The voltage levels *V1*, *V2*, *V3* and *V4* are reference points for timing measurement and the levels V_{IMAX} and V_{OMAX} represent the maximum high voltage level in the logic one state.

Figure 1-24
Signal propagation through a buffer from a buffer input to buffer output



The reference voltage levels for each buffer type are tabulated in Table 1-12 below.

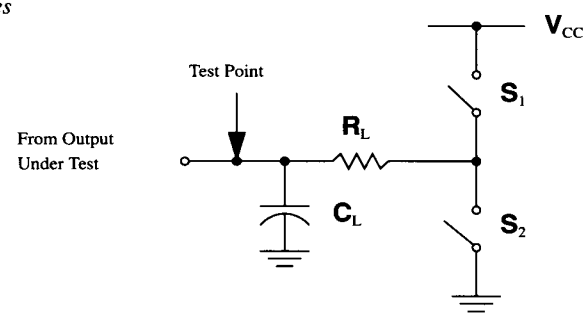
Table 1-12 Buffer Reference Voltages for Delay Measurement*

Buffer Type	V1	V2	V3	V4	VIH	VOH
CMOS Input	50% V_{CC}	50% V_{CCD}	50% V_{CC}	50% V_{CCD}	V_{CC}	V_{CCD}
TTL Input	1.5V	50% V_{CCD}	1.5V	50% V_{CCD}	3.0 V	V_{CCD}
Clock Buffers	50% V_{CC}	50% V_{CCD}	50% V_{CC}	50% V_{CCD}	V_{CC}	V_{CCD}
Driven Output	50% V_{CCD}	1.5 V	50% V_{CCD}	1.5 V	V_{CCD}	V_{CC}
Three-State Output	50% V_{CCD}	10% V_{CC}	50% V_{CCD}	90% V_{CC}	V_{CCD}	V_{CC}

* V_{CCD} is the regulated internal supply voltage.

In the case of buffers with non-driving states, which include three-state, open drain and bidirectional buffers, the load circuit shown in Figure 1-25 is added to the PAD output pin for a timing measurement in which the PAD makes a transition either to or from the undriven "Z" state:

Figure 1-25
Buffers with non-driving states



C_L is the (variable) load capacitance and R_L is fixed at 1 kΩ. The switches are set as illustrated in Table 1-13.

Table 1-13 Switch Setting

Parameter	S1	S2
t_{PZH}	open	closed
t_{PZL}	closed	open
t_{PHZ}	open	closed
t_{PLZ}	closed	open
t_{PLH}	open	open
t_{PHL}	open	open

NOTE: For open drain buffers, S_1 is always closed and S_2 is always open.