



Quad 2-Input NOR Gate

ELECTRICALLY TESTED PER:
5962-8755701

The 10H502 is a quad 2-input **NOR** gate. The 10H502 provides one gate with **OR/NOR** outputs. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increases in power-supply current.

- Propagation Delay, 1.0 ns Typical
- 40 mW Max/Gate (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
VCC1	1	5	2	GND
AOUT	2	6	3	51 Ω to V _{TT}
BOUT	3	7	4	51 Ω to V _{TT}
A _{IN}	4	8	5	51 Ω to V _{TT}
A _{IN}	5	9	7	OPEN
B _{IN}	6	10	8	51 Ω to V _{TT}
B _{IN}	7	11	9	OPEN
V _{EE}	8	12	10	V _{EE}
D _{OUT}	9	13	12	51 Ω to V _{TT}
C _{IN}	10	14	13	51 Ω to V _{TT}
C _{IN}	11	15	14	OPEN
D _{IN}	12	16	15	51 Ω to V _{TT}
D _{IN}	13	1	17	OPEN
C _{OUT}	14	2	18	51 Ω to V _{TT}
D _{OUT}	15	3	19	51 Ω to V _{TT}
VCC2	16	4	20	GND

BURN - IN CONDITIONS:

V_{TT} = -2.0 V MAX/ -2.2 V MIN

V_{EE} = -5.7 V MAX/ -5.2 V MIN

Military 10H502

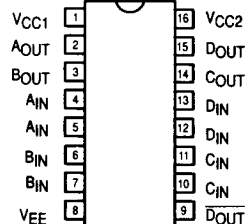


AVAILABLE AS

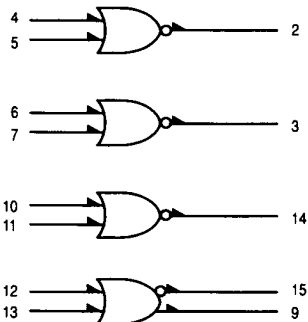
- 1) JAN: N/A
 - 2) SMD: 5962-8755701
 - 3) 883: 10H502/BXAJC
- X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before
the slash on LCC.

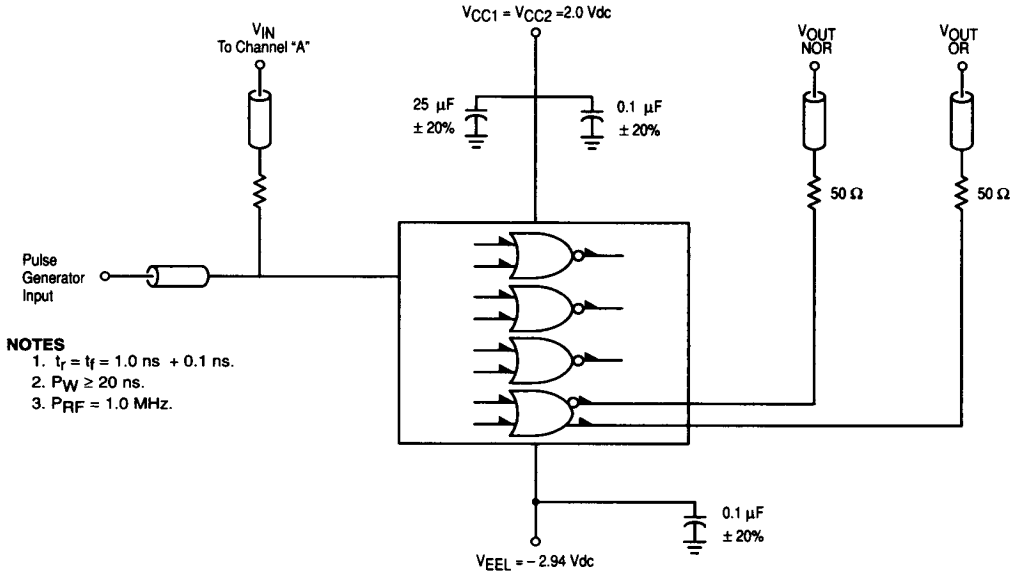


LOGIC DIAGRAM



10H502

2



NOTES

1. All input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be ≤ 0.250 inches (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
2. Outputs not under test should be connected to a 100Ω resistor to ground.

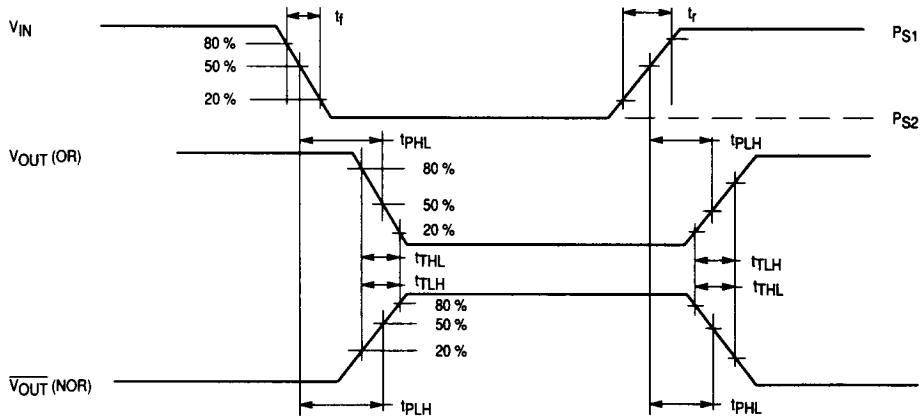


Figure 1. Switching Test Circuit and Waveforms

10H502 QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)									
	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	P _{S1}	P _{S2}	VEE1	VEE2	VEEL	VEEL
T _A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94	-2.94
T _A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94	-2.94
T _A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V _{CC} = 0 V, Output Load = 100 Ω to - 2.0 V									
		Subgroup 1		Subgroup 2		Subgroup 3												
		Min	Max	Min	Max	Min	Max											
V _{OH}	High Output Voltage	- 1.01	- 0.78	- 0.86	- 0.65	- 1.06	- 0.84	V	12, 13	4-7 12, 13			8		1, 16	2, 3, 9, 14, 15		
V _{OL}	Low Output Voltage	- 1.95	- 1.58	- 1.95	- 1.565	- 1.95	- 1.61	V	5-7 10-13	10-13			8		1, 16	2, 3, 9, 14, 15		
V _{OH1}	High Output Voltage	- 1.01	- 0.78	- 0.86	- 0.65	- 1.06	- 0.84	V			12, 13	4, 6 10-13	8	8	1, 16	2, 9, 15		
V _{OL1}	Low Output Voltage	- 1.95	- 1.58	- 1.95	- 1.565	- 1.95	- 1.61	V			4-7 10-13	12, 13	8	8	1, 16	2, 9, 15		
I _{EE}	Power Supply Current	- 26		- 29		- 29		mA					8		1, 16	8		
I _{IH1}	Input Current High		265		425		425	μA	4, 7 10-13				8		1, 16	4, 7, 10-13		
I _{IL}	Input Current Low	0.5		0.3		0.5		μA		4-5 10-13			8		1, 16	4, 7, 10-13		

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T _A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94	
T _A = - 55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94	

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max							
t _{TLH}	Rise Time	0.5	1.6	0.55	1.7	0.5	1.5	ns	V _{IN}	V _{OUT}	V _{CC}	VEEL	P.U.T.	
t _{THL}	Fall time	0.5	1.6	0.55	1.7	0.5	1.5	ns	5, 7, 11, 13	2, 3, 14, 9, 15	1, 16	8	2, 3, 9, 14, 15	
t _{PLH}	Propagation Delay Low to High	0.4	1.25	0.4	1.5	0.4	1.25	ns	5, 7, 11, 13	2, 3, 14, 15	1, 16	8	2, 3, 9, 14, 15	
t _{PHL}	Propagation Delay High to Low	0.4	1.25	0.4	1.5	0.4	1.25	ns	5, 7, 11, 13	2, 3, 14, 15	1, 16	8	2, 3, 9, 14, 15	