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μPD17P104**4-BIT SINGLE-CHIP MICROCONTROLLER****2**

The μPD17P104 is a tiny microcontroller consisting of a 1K-byte ROM, 16-word RAM, and 16 input/output ports. It is a one-time PROM version of the μPD17104, whose internal mask ROM is replaced with a one-time PROM.

Two μPD17P104 models are available: μPD17P104CS and μPD17P104GS, which allow a program to be written only once. They are suitable for evaluation of μPD17104 and for small-scale production.

The μPD17000 architecture of the CPU uses general registers so that data memory can be manipulated directly for effective programming. Every instruction is 1 word long, consisting of 16 bits.

FEATURES

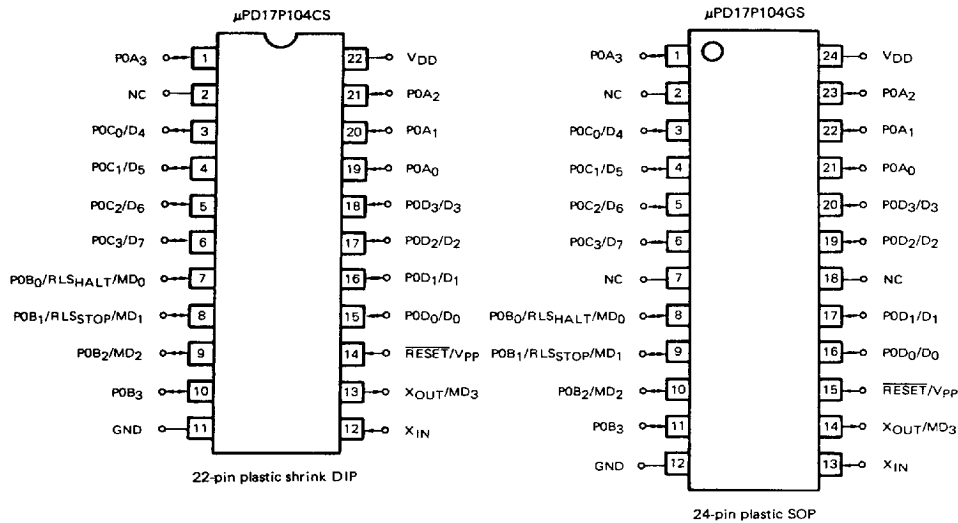
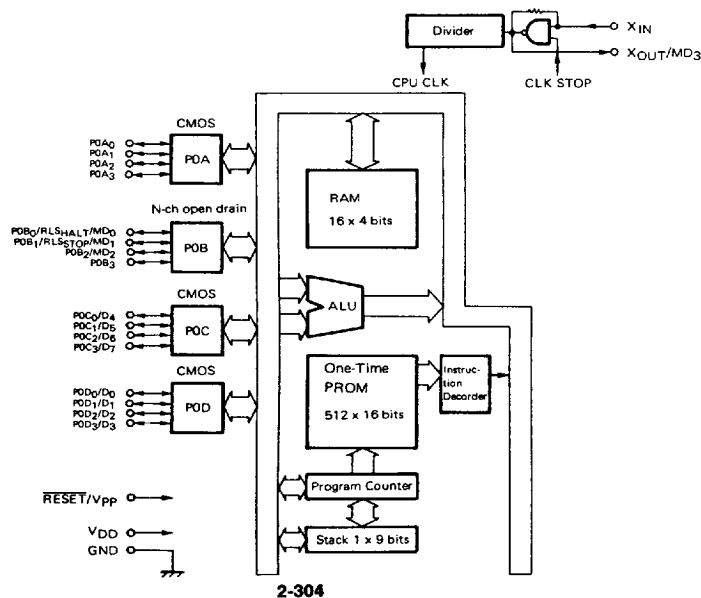
- Compatible with the μPD17104
- Program memory (one-time PROM): 1K bytes (512 words x 16 bits)
- Data memory (RAM): 16 words x 4 bits
- Input/output ports: 16 ports (including four N-ch open-drain outputs)
- Instruction execution time: 2 μs (with 8 MHz crystal or ceramic resonator connected)
- Number of instructions: 24 (Each instruction is 1 word long.)
- Stack level: 1
- A standby function is supported (with the STOP and HALT instructions).
- Data memory can retain data on low voltage (2.0 V at minimum).
- An oscillator is included for the system clock (for crystal or ceramic resonator).
- Operating supply voltage: 2.7 to 6.0 V (at 2 MHz)
4.5 to 6.0 V (at 8 MHz)

APPLICATIONS

- Controlling electric appliances or toys
- Providing general-purpose logic ICs in one chip

ORDERING INFORMATION

Order Code	Package
μPD17P104CS	22-pin plastic shrink DIP (300 mil)
μPD17P104GS	24-pin plastic SOP (300 mil)

μPD17P104**PIN CONFIGURATION (Top View)****BLOCK DIAGRAM**

PIN FUNCTIONS

● Port pins

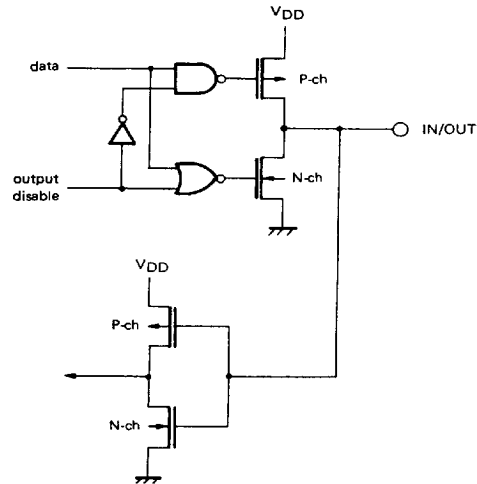
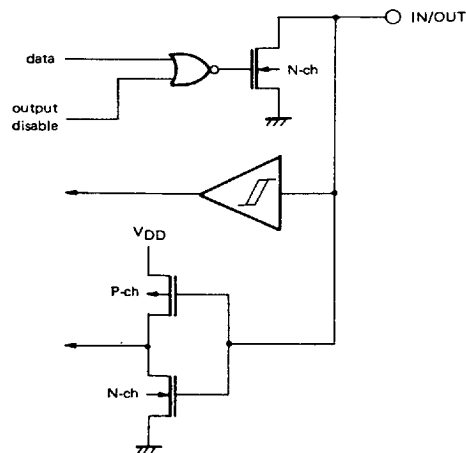
PIN NAME	INPUT/ OUTPUT	DUAL FUNCTION PIN		FUNCTION		When writing to program memory or verifying its contents	WHEN RESET
POA ₀	Input/output			• CMOS (push-pull) 4-bit input/ output port (port 0A)		Pull down	High impedance (input mode)
POA ₁							
POA ₂							
POA ₃							
POB ₀	Input/output	RLSHALT	MD ₀	• N-ch open-drain 4-bit input/ output port (port 0B)	For the HALT mode releasing	Mode selection pin	High impedance (input mode)
POB ₁		RLSTOP	MD ₁		For the STOP mode releasing		
POB ₂		MD ₂					
POB ₃					Pull down		
POC ₀	Input/output	D ₄		• CMOS (push-pull) 4-bit input/ output port (port 0C)	8-bit data input/output pin (high-order 4 bits)	High impedance (input mode)	
POC ₁		D ₅					
POC ₂		D ₆					
POC ₃		D ₇					
POD ₀	Input/output	D ₀		• CMOS (push-pull) 4-bit input/ output port (port 0D)	8-bit data input/output pin (low-order 4-bits)	High Impedance (input mode)	
POD ₁		D ₁					
POD ₂		D ₂					
POD ₃		D ₃					

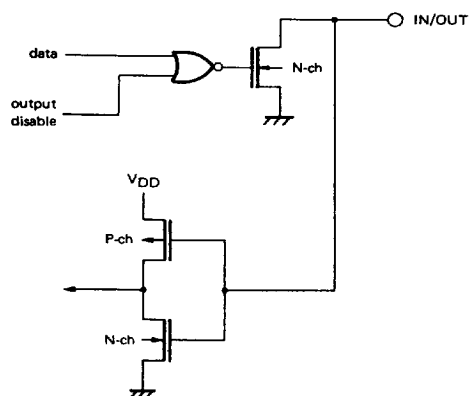
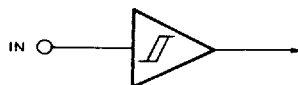
● Non-port pins

PIN NAME	INPUT/OUTPUT	DUAL FUNCTION PIN	FUNCTION	When writing to program memory or verifying its contents
RESET	Input	V _{pp}	System reset input pin	Voltage is applied to this pin (+12.5 V)
VDD			Positive power supply pin	Positive power supply pin (+6.0 V)
GND			GND pin	GND pin
XIN			Pins to be connected to the system clock resonator	Program memory address update
XOUT		MD ₃	Pins to be connected to the system clock resonator	Mode selection pin
NC			NC pin is not connected internally.	

μPD17P104**PIN INPUT/OUTPUT CIRCUITS**

Following are schematics of the input/output circuits of the pins of the μPD17P104.

(1) POC and POD**(2) POB₀ and POB₁**

(3) $P0B_2$ and $P0B_3$ (4) $\overline{\text{RESET}}$ 

9. DIFFERENCES BETWEEN THE μPD17P104 AND μPD17104

The μPD17P104 is a one-time PROM version of the μPD17104, in which the internal mask ROM is replaced with a one-time PROM. The μPD17P104 has the same CPU functions and internal hardwares as those of μPD17104 except for its program memory and mask option. Table 9-1 lists the differences between them.

Table 9-1 Differences between μPD17P104 and μPD17104

ITEM	μPD17P104	μPD17104
ROM	One-time PROM 512 x 16 bits	Mask ROM 512 x 16 bits
Pull-up resistors of pins POB ₀ to POB ₃	None	Mask option
Pull-up resistors of RESET pin	None	Mask option
Connection pin	V _{PP} pin and operation mode selection pins are provided.	V _{PP} pin and operation mode selection pins are not provided.
Power supply	2.7 to 6.0 V (at 2 MHz) 4.5 to 6.0 V (at 8 MHz)	
Package	22-pin plastic shrink DIP 24-pin plastic SOP	
Waiting time for the operation mode	16 clock pulses	8 clock pulses

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μPD17P104**10. WRITING TO AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)**

The μPD17P104's internal program memory consists of a 512 x 16 bit one-time PROM.

Writing to the one-time PROM or verifying the contents of the PROM is accomplished using the pins shown in the table below. Note that address inputs are not used; instead, the address is updated using the clock input from the X_{IN} pin.

PIN NAME	FUNCTION
V_{PP}	Voltage is applied to this pin when writing to program memory or verifying its contents.
X_{IN}	Input pin for address update clock used when writing to program memory or verifying its contents
MD_0 to MD_3	Pins that turn to input pins and are used as operation mode selection pins when writing to program memory or verifying its contents
D_0 to D_7	Input/output pins for 8-bit data used when writing to program memory or verifying its contents

10.1 PROGRAM MEMORY WRITE/VERIFY MODES

If +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after a certain duration of reset status ($V_{DD} = 5$ V, $RESET = 0$ V), the μPD17P104 enters program memory write/verify mode. A specific operating mode is then selected by setting the MD_0 through MD_3 pins as follows. Set the other unused pins to GND level by means of pull-down resistors.

OPERATING MODE SPECIFICATION						OPERATING MODE
V_{PP}	V_{DD}	MD_0	MD_1	MD_2	MD_3	
+12.5 V	+6 V	H	L	H	L	Program memory address clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	X	H	H	Program inhibit mode

X: L (low) or H (high)

10.2 WRITING TO PROGRAM MEMORY

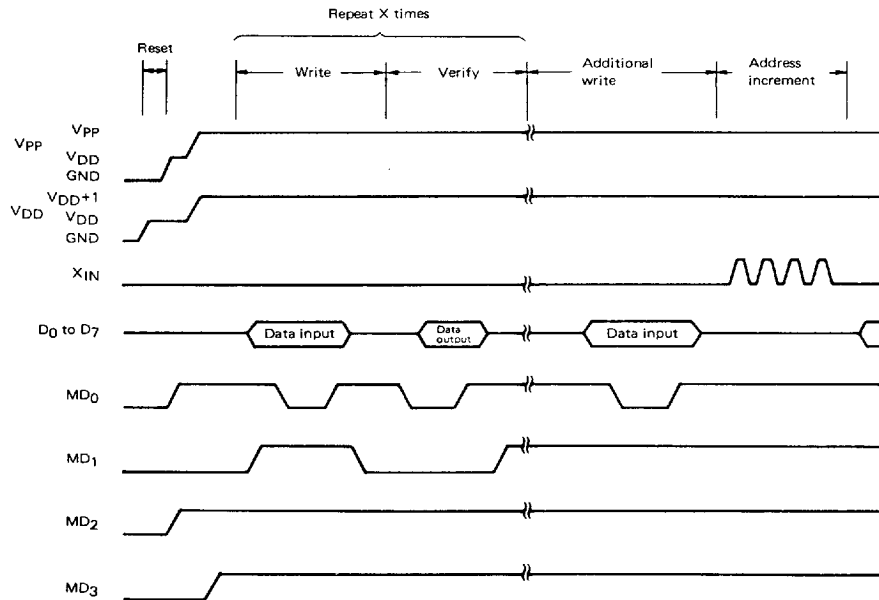
The procedure for writing to program memory is described below; high-speed write is possible.

- (1) Pull low the levels on all unused pins to GND by means of resistors. Bring X_{IN} to low level.
- (2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
- (3) Wait 10 μs. Then apply 5 V to V_{PP} .
- (4) Set the mode selection pins to program memory address clear mode.
- (5) Apply 6 V to V_{DD} and 12.5 V to V_{PP} .
- (6) Select program inhibit mode.
- (7) Write data in 1 ms write mode.
- (8) Select program inhibit mode.
- (9) Select verify mode. If the write operation is found successful, proceed to step (10). If the operation is found unsuccessful, repeat steps (7) to (9).
- (10) Perform additional write for (number of repetitions of steps (7) to (9)) x 1 ms.
- (11) Select program inhibit mode.

μPD17P104

- (12) Increment the program memory address by one on reception of four pulses on the X_{IN} pin.
- (13) Repeat steps (7) to (12) until the last address is reached.
- (14) Select program memory address clear mode.
- (15) Apply 5 V to the V_{DD} and V_{PP} pins.
- (16) Turn power off.

The timing for steps (2) to (12) is shown below.

**10.3 READING PROGRAM MEMORY**

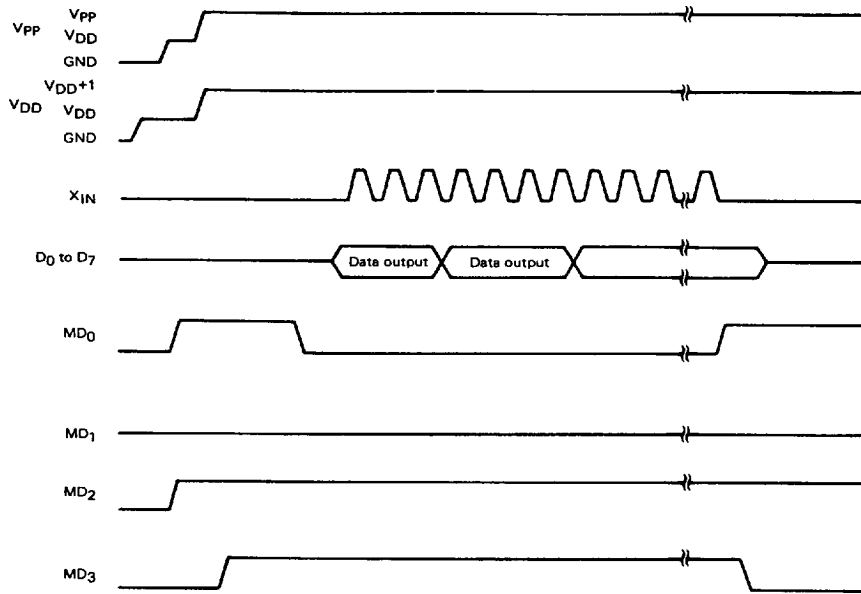
- (1) Pull low the levels of all unused pins to GND by means of resistors. Bring X_{IN} to low level.
- (2) Apply 5 V to V_{DD} and bring V_{PP} to low level.
- (3) Wait 10 μ s. Then apply 5 V to V_{PP} .
- (4) Set the mode selection pins to program memory address clear mode.
- (5) Apply 6 V to V_{DD} and 12.5 V to V_{PP} .
- (6) Select program inhibit mode.
- (7) Select verify mode. Data is output sequentially one address at a time for each cycle of four clock pulses on the X_{IN} pin.
- (8) Select program inhibit mode.
- (9) Select program memory address clear mode.
- (10) Apply 5 V to the V_{DD} and V_{PP} pins.
- (11) Turn power off.

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μPD17P104

The timing for steps (2) to (9) is shown below.



11. ASSEMBLER RESERVED WORDS

Table 11-1 lists the reserved words defined in the μPD17P104 device file (AS17104).

Table 11-1 Reserved Words

Name	Attribute	Value	Read/write	Description
P0A0	FLG	0.70H.0	Read/write	Bit 0 of port 0A
P0A1	FLG	0.70H.1	Read/write	Bit 1 of port 0A
P0A2	FLG	0.70H.2	Read/write	Bit 2 of port 0A
P0A3	FLG	0.70H.3	Read/write	Bit 3 of port 0A
P0B0	FLG	0.71H.0	Read/write	Bit 0 of port 0B
P0B1	FLG	0.71H.1	Read/write	Bit 1 of port 0B
P0B2	FLG	0.71H.2	Read/write	Bit 2 of port 0B
P0B3	FLG	0.71H.3	Read/write	Bit 3 of port 0B
P0C0	FLG	0.72H.0	Read/write	Bit 0 of port 0C
P0C1	FLG	0.72H.1	Read/write	Bit 1 of port 0C
P0C2	FLG	0.72H.2	Read/write	Bit 2 of port 0C
P0C3	FLG	0.72H.3	Read/write	Bit 3 of port 0C
P0D0	FLG	0.73H.0	Read/write	Bit 0 of port 0D
P0D1	FLG	0.73H.1	Read/write	Bit 1 of port 0D
P0D2	FLG	0.73H.2	Read/write	Bit 2 of port 0D
P0D3	FLG	0.73H.3	Read/write	Bit 3 of port 0D
BCD	FLG	0.7EH.0	Read/write	BCD arithmetic flag
PSW	MEM	0.7FH	Read/write	Program status word
Z	FLG	0.7FH.1	Read/write	Zero flag
CY	FLG	0.7FH.2	Read/write	Carry flag
CMP	FLG	0.7FH.3	Read/write	Compare flag

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μPD17P104**12. INSTRUCTION SET****12.1 INSTRUCTION SET LIST**

b ₁₄ to b ₁₁ \ b ₁₅				0	1
BIN	HEX				
0 0 0 0	0	ADD	r, m	ADD	m, #i
0 0 0 1	1	SUB	r, m	SUB	m, #i
0 0 1 0	2	ADDC	r, m	ADDC	m, #i
0 0 1 1	3	SUBC	r, m	SUBC	m, #i
0 1 0 0	4	AND	r, m	AND	m, #i
0 1 0 1	5	XOR	r, m	XOR	m, #i
0 1 1 0	6	OR	r, m	OR	m, #i
0 1 1 1	7	RET			
		RETSK			
		RORC	r		
		STOP	s		
		HALT	h		
		NOP			
1 0 0 0	8	LD	r, m	ST	m, r
1 0 0 1	9	SKE	m, #i	SKGE	m, #i
1 0 1 0	A				
1 0 1 1	B	SKNE	m, #i	SKLT	m, #i
1 1 0 0	C	BR	addr	CALL	addr
1 1 0 1	D			MOV	m, #i
1 1 1 0	E			SKT	m, #n
1 1 1 1	F			SKF	m, #n

μPD17P104

12.2 INSTRUCTIONS

Legend:

M	: One of data memory	n	: Bit position : 4 bits
m	: Data memory address specified by $\{m_H, m_L\}$ of each bank	addr	: One of program memory address : 11 bits
m_H	: Data memory address high (row address) : 3 bits	a_H	: Program memory address high : 3 bits
m_L	: Data memory address low (column address) : 4 bits	a_M	: Program memory address middle : 4 bits
R	: One of general register specified by $\{(RP), r\}$	a_L	: Program memory address low : 4 bits
r	: General register address low (column address) : 4 bits	CY	: Carry flag
RP	: General register pointer	CMP	: Compare flag
PC	: Program counter	s	: Stop release condition
SP	: Stack pointer	h	: Halt release condition
STACK	: Stack specified by (SP)	[]	: Address of M,R
i	: Immediate data : 4 bits	()	: Contents of M,R

Type	Mnemonic	Operand	Function	Operation	Machine code			
					Op code	3 bits	4 bits	4 bits
Add	ADD	r,m	Add memory to register	$R \leftarrow (R) + (M)$	0000	m_H	m_L	r
		m, #i	Add immediate data to memory	$M \leftarrow (M) + i$	1000	m_H	m_L	i
	ADDC	r,m	Add memory to register with carry	$R \leftarrow (R) + (M) + (CY)$	0010	m_H	m_L	r
		m, #i	Add immediate data to memory with carry	$R \leftarrow (M) + i + (CY)$	1010	m_H	m_L	i
Subtract	SUB	r,m	Subtract memory from register	$R \leftarrow (R) - (M)$	0001	m_H	m_L	r
		m, #i	Subtract immediate data from memory	$M \leftarrow (M) - i$	1001	m_H	m_L	i
	SUBC	r,m	Subtract memory from register with borrow	$R \leftarrow (R) - (M) - (CY)$	0011	m_H	m_L	r
		m, #i	Subtract immediate data from memory with borrow	$M \leftarrow (M) - i - (CY)$	1011	m_H	m_L	i
Compare	SKE	m, #i	Skip if memory equal to immediate data	$M - i$, skip if zero	0100	m_H	m_L	i
	SKGE	m, #i	Skip if memory greater than or equal to immediate data	$M - i$, skip if not borrow	1100	m_H	m_L	i
	SKLT	m, #i	Skip if memory less than immediate data	$M - i$, skip if borrow	1101	m_H	m_L	i
	SKNE	m, #i	Skip if memory not equal to immediate data	$M - i$, skip if not zero	0101	m_H	m_L	i
Logical operation	AND	m, #i	Logical AND of memory and immediate data	$M \leftarrow (M) \text{ AND } i$	1010	m_H	m_L	i
		r,m	Logical AND of register and memory	$R \leftarrow (R) \text{ AND } (M)$	0010	m_H	m_L	r
	OR	m, #i	Logical OR of memory and immediate data	$M \leftarrow (M) \text{ OR } i$	1011	m_H	m_L	i
		r,m	Logical OR of register and memory	$R \leftarrow (R) \text{ OR } (M)$	0011	m_H	m_L	r
	XOR	m, #i	Logical XOR of memory and immediate data	$M \leftarrow (M) \text{ XOR } i$	1010	m_H	m_L	i
		r,m	Logical XOR of register and memory	$R \leftarrow (R) \text{ XOR } (M)$	0010	m_H	m_L	r
Transfer	LD	r,m	Load memory of register	$R \leftarrow (M)$	0100	m_H	m_L	r
	ST	m,r	Store register to memory	$(M) \leftarrow R$	1100	m_H	m_L	r
	MOV	m, #i	Move immediate data to memory	$M \leftarrow i$	1110	m_H	m_L	i
Test	SKT	m, #n	Test memory bits, then skip if all bits specified are true	$CMP \leftarrow 0$ skip if $M_n = \text{all "1"}$	1110	m_H	m_L	n
	SKF	m, #n	Test memory bits, then skip if all bits specified are false	$CMP \leftarrow 0$ skip if $M_n = \text{all "0"}$	1111	m_H	m_L	n

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	Type	Mnemonic	Operand	Function	Operation	Machine code			
						Op code	3 bits	4 bits	4 bits
Branch	HR	addr		Jump to the address	PC←ADDR	01100	a _H	a _H	a _L
Shift	RORC	r		Rotate register right with carry	(CY)→(R)→CY	00111	000	0111	r
Subroutine	CALL	addr		Call subroutine	SP←(SP) - 1 STACK←((PC) + 1), PC←ADDR	11100	a _H	a _H	a _L
	RET			Return to main routine from subroutine	PC←(STACK), SP←(SP) + 1	00111	000	1110	0000
	RETSK			Return to main routine from subroutine, then skip unconditionary	PC←(STACK), SP←(SP) + 1 and skip	00111	001	1110	0000
Miscellaneous	STOP	s		Stop clock	STOP	00111	010	1111	s
	HALT	h		Halt the CPU, restart by condition h	HALT	00111	011	1111	h
	NOP			No operation	No Operation	00111	100	1111	0000

μPD17P104**13. ELECTRICAL CHARACTERISTICS (PRELIMINARY)****ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)**

Supply Voltage	V_{DD}		-0.3 to +7.0	V
Supply Voltage	V_{PP}		-0.3 to +13.5	V
Input Voltage	V_I	P0A, P0C, P0D	-0.3 to $V_{DD} + 0.3$	V
		P0B	-0.3 to +11	V
Output Voltage	V_O	P0A, P0C, P0D	-0.3 to $V_{DD} + 0.3$	V
		P0B	-0.3 to +11	V
High-Level Output Current	I_{OH}	Each of P0A, P0B, P0C, P0D	-5	mA
		Total of all pins	-15	mA
Low-Level Output Current	I_{OL}	Each of P0A, P0B, P0C, P0D	30	mA
		Total of all pins	100	mA
Operating Temperature	T_{opt}		-40 to +85	$^\circ\text{C}$
Storage Temperature	T_{stg}		-65 to +150	$^\circ\text{C}$
Power Consumption	P_d	$T_a = 85^\circ\text{C}$	22-pin shrink DIP	400
			24-pin SOP	250

CAPACITANCE ($T_a = 25^\circ\text{C}$, $V_{DD} = 0\text{ V}$)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Capacitance	C_{IN}			15	pF	$f = 1\text{ MHz}$
I/O(*) Capacitance	C_{IO}			15	pF	0 V for pins other than pins to be measured

* Input/output

DC CHARACTERISTICS ($T_a = -40$ to $+85$ °C, $V_{DD} = 2.7$ to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
High-Level Input Voltage	V_{IH1}	$0.7 V_{DD}$		V_{DD}	V	Other than the following pins and port	
	V_{IH2}	$0.8 V_{DD}$		V_{DD}	V	P0B and RESET	
	V_{IH3}	$0.8 V_{DD}$		9	V	P0B (*)	
	V_{IH4}	$V_{DD}-0.5$		V_{DD}	V	X_{IN}	
Low-Level Input Voltage	V_{IL1}	0		$0.3 V_{DD}$	V	Other than the following pins and port	
	V_{IL2}	0		$0.2 V_{DD}$	V	P0B and RESET	
	V_{IL3}	0		0.5	V	X_{IN}	
High-Level Output Voltage on P0A, P0C, and P0D	V_{OH}	$V_{DD}-2.0$			V	$V_{DD} = 4.5$ to 6.0 V, $I_{OH} = -2$ mA	
		$V_{DD}-1.0$			V	$I_{OH} = -200$ μA	
Low-Level Output Voltage on P0A, P0B, P0C, and P0D	V_{OL}			2.0	V	$V_{DD} = 4.5$ to 6.0 V, $I_{OL} = 15$ mA	
				0.5	V	$I_{OL} = 600$ μA	
High-Level Input Leakage Current on P0A to P0D	I_{LIH1}			5	μA	$V_{IN} = V_{DD}$	
	I_{LIH2}			10	μA	$V_{IN} = 9$ V (*)	
Low-Level Input Leakage Current on P0A to P0D	I_{LIL}			-5	μA	$V_{IN} = 0$ V	
High-Level Output Leakage Current on P0A to P0D	I_{LOH1}			5	μA	$V_{OUT} = V_{DD}$	
	I_{LOH2}			10	μA	$V_{OUT} = 9$ V (*)	
Low-Level Output Leakage Current on P0A to P0D	I_{LOL}			-5	μA	$V_{OUT} = 0$ V	
Power Supply Current	I_{DD1}		1.5	4.5	mA	Operation mode	$V_{DD} = 5$ V ± 10 %, $f_{CC} = 8.0$ MHz
			250	750	μA		$V_{DD} = 3$ V ± 10 %, $f_{CC} = 2.0$ MHz
	I_{DD2}		1.0	3.0	mA	HALT mode	$V_{DD} = 5$ V ± 10 %, $f_{CC} = 8.0$ MHz
			200	600	μA		$V_{DD} = 3$ V ± 10 %, $f_{CC} = 2.0$ MHz
	I_{DD3}		0.1	10	μA	STOP mode	$V_{DD} = 5$ V ± 10 %
			0.1	5	μA		$V_{DD} = 3$ V ± 10 %

* When N-ch open-drain input/output is selected

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**CHARACTERISTICS OF DATA MEMORY FOR HOLDING DATA ON LOW SUPPLY VOLTAGE
IN THE STOP MODE ($T_a = -40$ to $+85$ °C)**

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Data Hold Supply Voltage	V_{DDDR}	2.0		6.0	V	
Data Hold Supply Current	I_{DDDR}		0.1	5.0	μA	$V_{DDDR} = 2.0$ V
Release Signal Set Time	t_{SREL}	0			μs	

AC CHARACTERISTICS ($T_a = -40$ to $+85$ °C, $V_{DD} = 2.7$ to 6.0 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Internal Clock Cycle Time	T_{CY}	1.9		33	μs	$V_{DD} = 4.5$ to 6.0 V
		7.6		33	μs	
High/Low Level Width on POB_0 and POB_1	T_{PBH} T_{PBL}	10			μs	
High/Low Level Width on $\overline{RESET}$	T_{RSH} T_{RSL}	10			μs	

DC PROGRAMING CHARACTERISTICS ($T_a = 25$ °C, $V_{DD} = 6.0 \pm 0.25$ V, $V_{pp} = 12.5 \pm 0.5$ V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Voltage High	V_{IH1}	$0.7 V_{DD}$		V_{DD}	V	Except X_{1N}
	V_{IH2}	$V_{DD} - 0.5$		V_{DD}	V	X_{1N}
Input Voltage Low	V_{IL1}	0		$0.3 V_{DD}$	V	Except X_{1N}
	V_{IL2}	0		0.4	V	X_{1N}
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
Output Voltage High	V_{OH}	$V_{DD} - 1.0$			V	$I_{OH} = -1$ mA
Output Voltage Low	V_{OL}			0.4	V	$I_{OL} = 1.6$ mA
V_{DD} Power Supply Current	I_{DD}			30	mA	
V_{pp} Power Supply Current	I_{pp}			30	mA	$MD0 = V_{IL}$, $MD1 = V_{IH}$

Notes 1. V_{pp} must be under +13.5 V including overshoot.

2. V_{DD} must be applied before V_{pp} on and must be off after V_{pp} off.

AC CHARACTERISTICS ($T_a = 25^\circ\text{C}$, $V_{DD} = 6.0 \pm 0.25\text{ V}$, $V_{PP} = 12.5 \pm 0.5\text{ V}$)

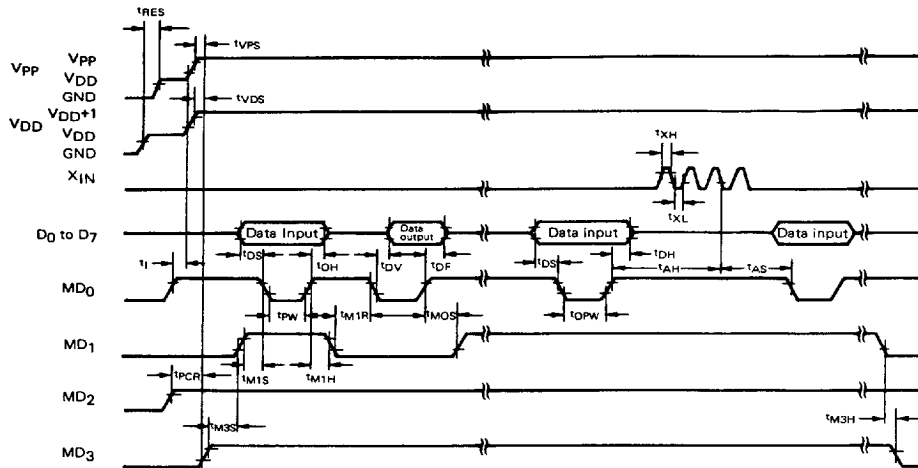
CHARACTERISTICS	SYMBOL	(*1)	MIN.	TYP.	MAX.	UNIT	CONDITION
Address Set Up Time(*2) to MD0↓	t _{AS}	t _{AS}	2			μs	
MD1 Setup Time to MD0↓	t _{M1S}	t _{OES}	2			μs	
Data Setup Time to MD0↓	t _{DS}	t _{DS}	2			μs	
Address Hold Time(*2) to MD0↑	t _{AH}	t _{AH}	2			μs	
Data Hold Time to MD0↑	t _{DH}	t _{DH}	2			μs	
Data Output Float Delay Time from MD0↑→	t _{DF}	t _{DF}	0		130	ns	
V _{PP} Setup Time to MD3↑	t _{VPS}	t _{VPS}	2			μs	
V _{DD} Setup Time to MD3↑	t _{VDS}	t _{VCS}	2			μs	
Initial Program Pulse Width	t _{PW}	t _{PW}	0.95	1.0	1.05	ms	
Additional Program Pulse Width	t _{OPW}	t _{OPW}	0.95		21.0	ms	
MD0 Setup Time to MD1↑	t _{MOS}	t _{CES}	2			μs	
Data Output Delay Time from MD0↑→	t _{DV}	t _{DV}			1	μs	MD0 = MD1 = V _{IL}
MD1 Hold Time to MD0↑	t _{M1H}	t _{OEH}	2			μs	t _{M1H} + t _{M1R} ≥ 50 μs
MD1 Recovery Time to MD0↓	t _{M1R}	t _{OR}	2			μs	
Program Counter Reset Time	t _{PCR}	—	10			μs	
X _{IN} Input High, Low Level Range	t _{XH} , t _{XL}	—	0.063			μs	
X _{IN} Input Frequency	f _X	—			8	MHz	
Initial Mode Set Time	t _I	—	2			μs	
MD3 Setup Time to MD1↑	t _{M3S}	—	2			μs	
MD3 Hold Time to MD1↓	t _{M3H}	—	2			μs	
MD3 Setup Time to MD0↓	t _{M3SR}	—	2			μs	Read program memory
Data Output Delay Time from Address(*2)	t _{DAD}	t _{ACC}	2			μs	Read program memory
Data Output Hold Time from Address(*2)	t _{HAD}	t _{OH}	0		130	ns	Read program memory
MD3 Hold Time to MD0↑	t _{M3HR}	—	2			μs	Read program memory
Data Output Float Delay Time from MD3↑→	t _{DFR}	—	2			μs	Read program memory
Reset Setup Time	t _{RES}		10			μs	

*1 Symbols for corresponding μPD27C256.

*2 Internal address signal is incremented by one at the falling edge of the third X_{IN} input, and it is not connected to the pin.

μ PD17P104

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NEC**WRITE PROGRAM MEMORY TIMING****READ PROGRAM MEMORY TIMING**