S-121 000979 T979 LSC

LSI LOGIC CORPORATION

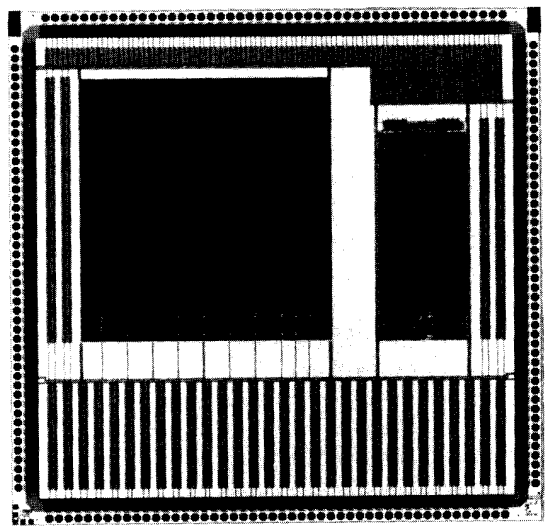
LSA2010 Two Micron HCMOS Structured Array™

General Description

The LSA2010 is a member of the 2-micron drawn, (1.4-micron effective) HCMOS family of Structured Arrays offered by LSI LOGIC Corporation. These very high performance, Application Specific Integrated Circuits (ASICs) combine special purpose silicon structures, optimized for performance with general purpose logic arrays on a single chip. Structured Arrays provide a high density of logic functionality while maintaining the flexibility of design and fast turn-around of metal mask programmable logic-arrays. The use of dual layer metal interconnect technology provides high speed, high packing density, ease of layout and the ability to configure megacell architectures at the interconnect level.

Contains The Following Structures:

- 3200 gate LL7000 Series type 2-micron drawn (1.4-micron effective) gate length HCMOS logic array
- 65,536-bit Read Only Memory (ROM)
  - –Metal mask programmable
  - –Metal mask configurable as either one or two ROMs
  - –Fully static
  - –ROM widths up to 128 bits
  - –Built-in scan testability
  - –Programmable output buffers
- 2304-bit Random Access Memory (RAM)
  - –Configurable as a single RAM
  - –Fully static
  - –Word width can be ×4, ×9, ×18 or ×36
  - –Latches on all data and address pins
  - –Low power standby mode
  - –Built-in scan testability
  - –Programmable output buffers



LSA2010 Pad Statistics

Max Pads[1]		Max I/O Pads[1]		Max Package Pins[2]	
Plastic or Ceramic	Ceramic	Plastic or Ceramic	Ceramic	Plastic or Ceramic	Ceramic
144	192	132	180	136	184

Notes:

1. The difference between the maximum number of pads and I/Os is the number of dedicated V_{DD} or V_{SS} pads. It may be necessary to configure additional I/O pads for V_{DD}/V_{SS}, depending on the number and drive of the output buffers.

2. LSI LOGIC recommends that all LSA2010 designs be configured for use in plastic packages, thus permitting upward compatibility to ceramic packages, where required. Does not apply to military designs.

RAM AC Switching Characteristics

Parameter	Typical	Worst-Case Commercial	Worst-Case Military
Read Cycle Time	27.4ns	47.7ns	60.8ns
Write Cycle Time	16.0ns	27.9ns	35.5ns

Representative 512 × 4 configuration.

AC Characteristics will vary slightly as a function of configuration.

ROM AC Switching Characteristics

Parameter	Typical	Worst-Case Commercial	Worst-Case Military
Read Cycle Time	35.1ns	61.1ns	77.9ns

Representative 1K × 64 configuration.

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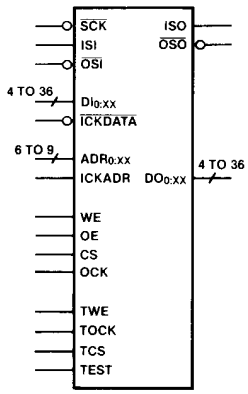
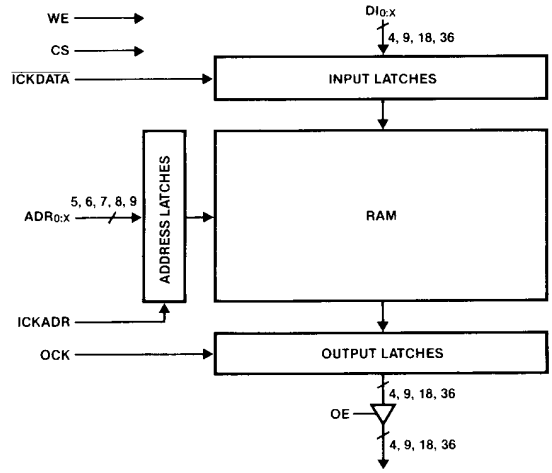
November 1985
Order No. 002010

RAM Block Diagram



RAM Logic Diagram — Normal Operation



RAM Configuration Table

	RAM Configuration Words × Bits
2304-Bit RAM	512 × 4 256 × 9 128 × 18 64 × 36

Allowable ROM Combinations

Single ROM	64K		
Dual ROM	ROM A	ROM B	Total
	60K + 4K = 64K		
	56K + 8K = 64K		
	48K + 16K = 64K		
	32K + 32K = 64K		

Note: Above sizes listed represent maximum allowable. Smaller ROMs (i.e., large ROMs not fully utilized) can be used.

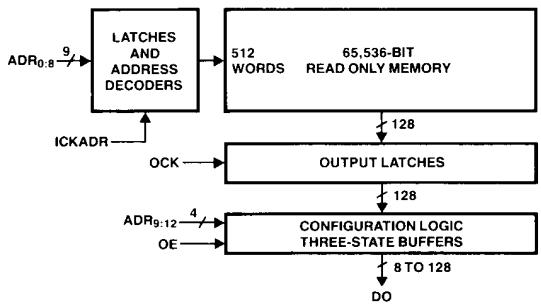
ROM Configuration Table

ROM Size / Address Lines Used	Single ROM	Dual ROM						
		ROM A			ROM A or ROM B	ROM B		
	64K	60K	56K	48K	32K	16K	8K	4K
$A_{0:8}$	512 × 128	512 × 120	512 × 112	512 × 96	512 × 64	512 × 32	512 × 16	512 × 8
$A_{0:9}$	1K × 64	1K × 60	1K × 56	1K × 48	1K × 32	1K × 16	1K × 8	1K × 4
$A_{0:10}$	2K × 32	2K × 30	2K × 28	2K × 24	2K × 16	2K × 8	2K × 4	2K × 2
$A_{0:11}$	4K × 16	4K × 15	4K × 14	4K × 12	4K × 8	4K × 4	4K × 2	4K × 1
$A_{0:12}$	8K × 8	—	—	—	—	—	—	—

ROM Block Diagrams

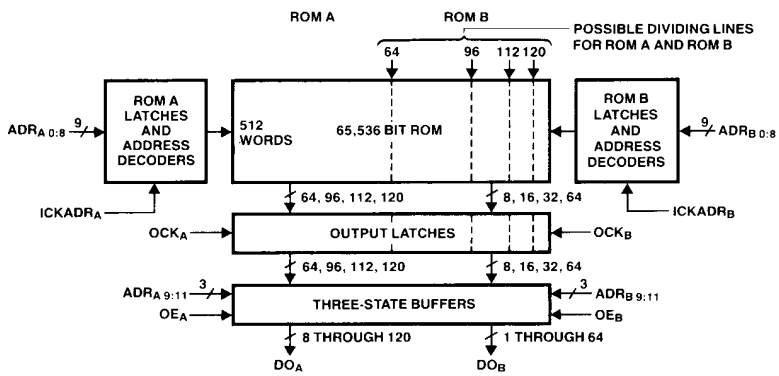
Single ROM

Normal Operation (TEST = LOW)



Dual ROM

Normal Operation (TEST = LOW)



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