HB52RD168GB-F

128 MB Unbuffered SDRAM Micro DIMM
16-Mword × 64-bit, 100 MHz Memory Bus, 1-Bank Module
(16 pcs of 16 M × 4 components)
PC100 SDRAM

ELPIDA

E0009H10 (1st edition)
(Previous ADE-203-1153A (Z))
Jan. 19, 2001

Description

The HB52RD168GB is a 16M × 64 × 1 bank Synchronous Dynamic RAM Micro Dual In-line Memory Module (Micro DIMM), mounted 16 pieces of 64-Mbit SDRAM (HM5264405FTB) sealed in TCP package and 1 piece of serial EEPROM (2-kbit EEPROM) for Presence Detect (PD). An outline of the product is 144-pin Zig Zag Dual tabs socket type compact and thin package. Therefore, it makes high density mounting possible without surface mount technology. It provides common data inputs and outputs. Decoupling capacitors are mounted beside TCP on the module board.

Note: Do not push the cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

Features

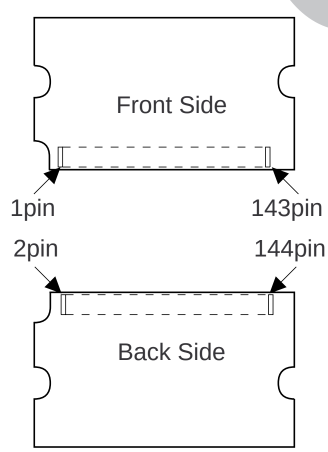
- 144-pin Zig Zag Dual tabs socket type
  - Outline: 38.00 mm (Length) × 30.00 mm (Height) × 3.80 mm (Thickness)
  - Lead pitch: 0.50 mm
- 3.3 V power supply
- Clock frequency: 100 MHz (max)
- LVTTL interface
- Data bus width: × 64 Non parity
- Single pulsed $\overline{\text{RAS}}$
- 4 Banks can operates simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length : 1/2/4/8/full page

- 2 variations of burst sequence
  - Sequential (BL = 1/2/4/8/full page)
  - Interleave (BL = 1/2/4/8)
- Programmable $\overline{\text{CE}}$ latency : 2/3 (HB52RD168GB-A6F/A6FL)
  : 3 (HB52RD168GB-B6F/B6FL)
- Byte control by DQMB
- Refresh cycles: 4096 refresh cycles/64 ms
- 2 variations of refresh
  - Auto refresh
  - Self refresh
- Low self refresh current: HB52RD168GB-A6FL/B6FL (L-version)
- Full page burst length capability
  - Sequential burst
  - Burst stop capability

Ordering Information

Type No.	Frequency	$\overline{\text{CE}}$ latency	Package	Contact pad
HB52RD168GB-A6F	100 MHz	2/3	Micro DIMM (144-pin)	Gold
HB52RD168GB-B6F	100 MHz	3		
HB52RD168GB-A6FL	100 MHz	2/3		
HB52RD168GB-B6FL	100 MHz	3		

Pin Arrangement



Pin Arrangement (cont.)

Front side				Back side			
Pin No.	**Signal name**	**Pin No.**	**Signal name**	**Pin No.**	**Signal name**	**Pin No.**	**Signal name**
1	V_{SS}	73	NC	2	V_{SS}	74	CK1
3	DQ0	75	V_{SS}	4	DQ32	76	V_{SS}
5	DQ1	77	NC	6	DQ33	78	NC
7	DQ2	79	NC	8	DQ34	80	NC
9	DQ3	81	V_{CC}	10	DQ35	82	V_{CC}
11	V_{CC}	83	DQ16	12	V_{CC}	84	DQ48
13	DQ4	85	DQ17	14	DQ36	86	DQ49
15	DQ5	87	DQ18	16	DQ37	88	DQ50
17	DQ6	89	DQ19	18	DQ38	90	DQ51
19	DQ7	91	V_{SS}	20	DQ39	92	V_{SS}
21	V_{SS}	93	DQ20	22	V_{SS}	94	DQ52
23	DQMB0	95	DQ21	24	DQMB4	96	DQ53
25	DQMB1	97	DQ22	26	DQMB5	98	DQ54
27	V_{CC}	99	DQ23	28	V_{CC}	100	DQ55
29	A0	101	V_{CC}	30	A3	102	V_{CC}
31	A1	103	A6	32	A4	104	A7
33	A2	105	A8	34	A5	106	A13 (BA0)
35	V_{SS}	107	V_{SS}	36	V_{SS}	108	V_{SS}
37	DQ8	109	A9	38	DQ40	110	A12 (BA1)
39	DQ9	111	A10 (AP)	40	DQ41	112	A11
41	DQ10	113	V_{CC}	42	DQ42	114	V_{CC}
43	DQ11	115	DQMB2	44	DQ43	116	DQMB6
45	V_{CC}	117	DQMB3	46	V_{CC}	118	DQMB7
47	DQ12	119	V_{SS}	48	DQ44	120	V_{SS}
49	DQ13	121	DQ24	50	DQ45	122	DQ56
51	DQ14	123	DQ25	52	DQ46	124	DQ57
53	DQ15	125	DQ26	54	DQ47	126	DQ58
55	V_{SS}	127	DQ27	56	V_{SS}	128	DQ59
57	NC	129	V_{CC}	58	NC	130	V_{CC}
59	NC	131	DQ28	60	NC	132	DQ60
61	CK0	133	DQ29	62	CKE0	134	DQ61
63	V_{CC}	135	DQ30	64	V_{CC}	136	DQ62
65	$\overline{RE}$	137	DQ31	66	$\overline{CE}$	138	DQ63

Front side				Back side			
Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
67	$\overline{W}$	139	V_{SS}	68	NC	140	V_{SS}
69	$\overline{S0}$	141	SDA	70	NC	142	SCL
71	NC	143	V_{CC}	72	NC	144	V_{CC}

Pin Description

Pin name	Function
A0 to A11	Address input — Row address A0 to A11 — Column address A0 to A9
A12/A13	Bank select address BA1, BA0
DQ0 to DQ63	Data-input/output
$\overline{S0}$	Chip select
$\overline{RE}$	Row address asserted bank enable
$\overline{CE}$	Column address asserted
$\overline{W}$	Write enable
DQMB0 to DQMB7	Byte input/output mask
CK0/CK1	Clock input
CKE0	Clock enable
SDA	Data-input/output for serial PD
SCL	Clock input for serial PD
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Serial PD Matrix*[1]

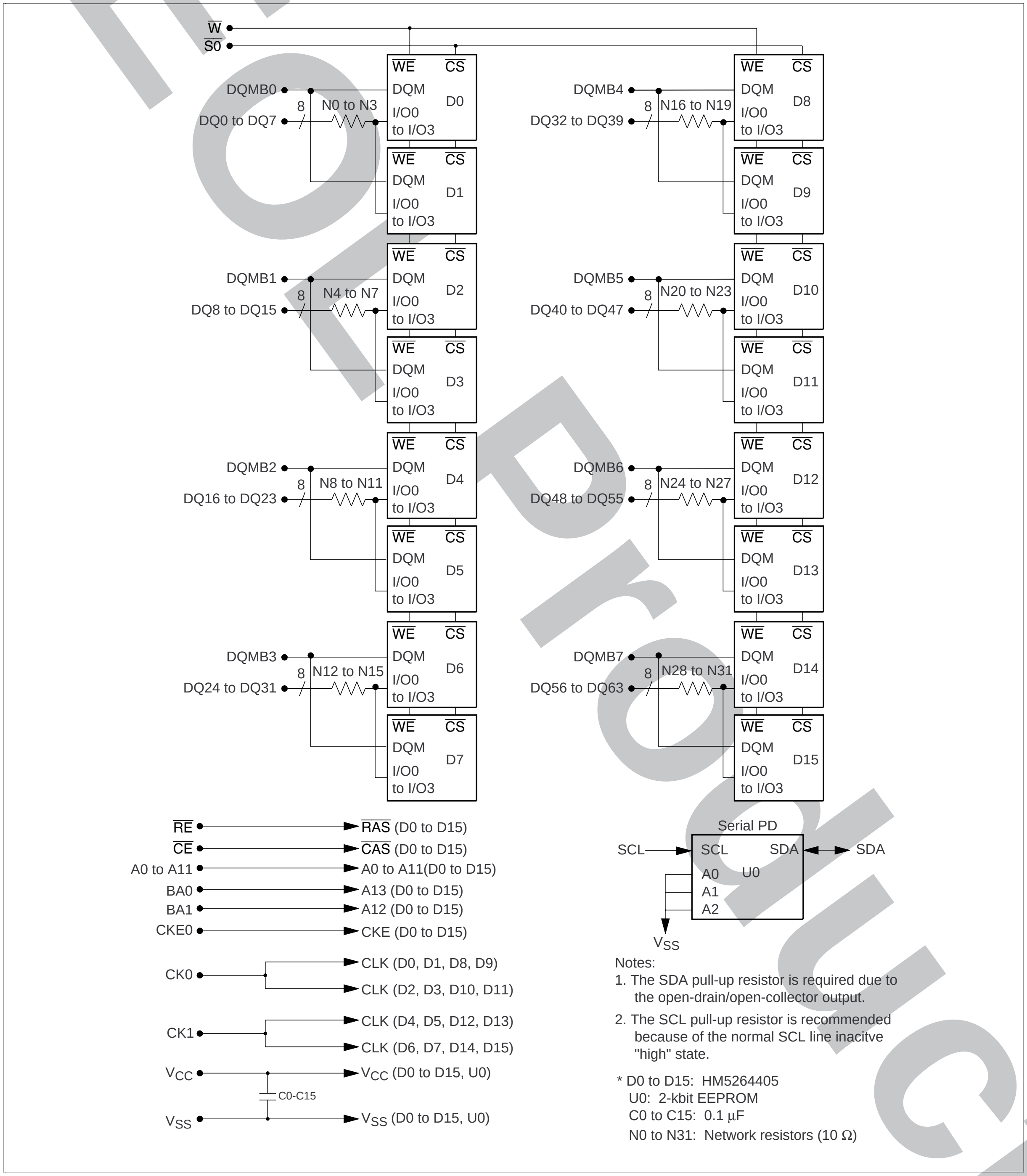
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes used by module manufacturer	1	0	0	0	0	0	0	0	80	128
1	Total SPD memory size	0	0	0	0	1	0	0	0	08	256 byte
2	Memory type	0	0	0	0	0	1	0	0	04	SDRAM
3	Number of row addresses bits	0	0	0	0	1	1	0	0	0C	12
4	Number of column addresses bits	0	0	0	0	1	0	1	0	0A	10
5	Number of banks	0	0	0	0	0	0	0	1	01	1
6	Module data width	0	1	0	0	0	0	0	0	40	64
7	Module data width (continued)	0	0	0	0	0	0	0	0	00	0 (+)
8	Module interface signal levels	0	0	0	0	0	0	0	1	01	LVTTL
9	SDRAM cycle time (highest $\overline{CE}$ latency) 10 ns	1	0	1	0	0	0	0	0	A0	CL = 3
10	SDRAM access from Clock (highest $\overline{CE}$ latency) 6 ns	0	1	1	0	0	0	0	0	60	CL = 3
11	Module configuration type	0	0	0	0	0	0	0	0	00	Non parity
12	Refresh rate/type	1	0	0	0	0	0	0	0	80	Normal (15.625 µs) Self refresh
13	SDRAM width	0	0	0	0	0	1	0	0	04	16M × 4
14	Error checking SDRAM width	0	0	0	0	0	0	0	0	00	—
15	SDRAM device attributes: minimum clock delay for back-to-back random column addresses	0	0	0	0	0	0	0	1	01	1 CLK
16	SDRAM device attributes: Burst lengths supported	1	0	0	0	1	1	1	1	8F	1, 2, 4, 8, full page
17	SDRAM device attributes: number of banks on SDRAM device	0	0	0	0	0	1	0	0	04	4
18	SDRAM device attributes: $\overline{CE}$ latency	0	0	0	0	0	1	1	0	06	2, 3
19	SDRAM device attributes: $\overline{S}$ latency	0	0	0	0	0	0	0	1	01	0
20	SDRAM device attributes: $\overline{W}$ latency	0	0	0	0	0	0	0	1	01	0
21	SDRAM module attributes	0	0	0	0	0	0	0	0	00	Unbuffer
22	SDRAM device attributes: General	0	0	0	0	1	1	1	0	0E	V_{CC} ± 10%

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
23	SDRAM cycle time (2nd highest $\overline{CE}$ latency) (-A6F/A6FL) 10 ns	1	0	1	0	0	0	0	0	A0	CL=2
	(-B6F/B6FL) 15 ns	1	1	1	1	0	0	0	0	F0	
24	SDRAM access from Clock (2nd highest $\overline{CE}$ latency) (-A6F/A6FL) 6 ns	0	1	1	0	0	0	0	0	60	CL=2
	(-B6F/B6FL) 8 ns	1	0	0	0	0	0	0	0	80	
25	SDRAM cycle time (3rd highest $\overline{CE}$ latency) Undefined	0	0	0	0	0	0	0	0	00	
26	SDRAM access from Clock (3rd highest $\overline{CE}$ latency) Undefined	0	0	0	0	0	0	0	0	00	
27	Minimum row precharge time	0	0	0	1	0	1	0	0	14	20 ns
28	Row active to row active min	0	0	0	1	0	1	0	0	14	20 ns
29	$\overline{RE}$ to $\overline{CE}$ delay min	0	0	0	1	0	1	0	0	14	20 ns
30	Minimum $\overline{RE}$ pulse width	0	0	1	1	0	0	1	0	32	50 ns
31	Density of each bank on module	0	0	1	0	0	0	0	0	20	128M byte
32	Address and command signal input setup time	0	0	1	0	0	0	0	0	20	2 ns
33	Address and command signal input hold time	0	0	0	1	0	0	0	0	10	1 ns
34	Data signal input setup time	0	0	1	0	0	0	0	0	20	2 ns
35	Data signal input hold time	0	0	0	1	0	0	0	0	10	1 ns
36 to 61	Superset information	0	0	0	0	0	0	0	0	00	Future use
62	SPD data revision code	0	0	0	1	0	0	1	0	12	Rev. 1.2A
63	Checksum for bytes 0 to 62 (-A6F/A6FL)	0	0	0	1	0	0	1	0	12	18
	(-B6F/B6FL)	1	0	0	0	0	0	1	0	82	130
64	Manufacturer's JEDEC ID code	0	0	0	0	0	1	1	1	07	HITACHI
65 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00	
72	Manufacturing location	×	×	×	×	×	×	×	×	××	*3 (ASCII-8bit code)
73	Manufacturer's part number	0	1	0	0	1	0	0	0	48	H
74	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
75	Manufacturer's part number	0	0	1	1	0	1	0	1	35	5
76	Manufacturer's part number	0	0	1	1	0	0	1	0	32	2
77	Manufacturer's part number	0	1	0	1	0	0	1	0	52	R

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
78	Manufacturer's part number	0	1	0	0	0	1	0	0	44	D
79	Manufacturer's part number	0	0	1	1	0	0	0	1	31	1
80	Manufacturer's part number	0	0	1	1	0	1	1	0	36	6
81	Manufacturer's part number	0	0	1	1	1	0	0	0	38	8
82	Manufacturer's part number	0	1	0	0	0	1	1	1	47	G
83	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
84	Manufacturer's part number	0	0	1	0	1	1	0	1	2D	—
85	Manufacturer's part number (-A6F/A6FL)	0	1	0	0	0	0	0	1	41	A
	(-B6F/B6FL)	0	1	0	0	0	0	1	0	42	B
86	Manufacturer's part number	0	0	1	1	0	1	1	0	36	6
87	Manufacturer's part number	0	1	0	0	0	1	1	0	46	F
88	Manufacturer's part number (L-version)	0	1	0	0	1	1	0	0	4C	L
	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
89	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
90	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30	Initial
92	Revision code	0	0	1	0	0	0	0	0	20	(Space)
93	Manufacturing date	×	×	×	×	×	×	×	×	××	Year code (BCD)*[4]
94	Manufacturing date	×	×	×	×	×	×	×	×	××	Week code (BCD)*[4]
95 to 98	Assembly serial number	*[6]									
99 to 125	Manufacturer specific data	—	—	—	—	—	—	—	—	—	*[5]
126	Intel specification frequency	0	1	1	0	0	1	0	0	64	100 MHz
127	Intel specification $\overline{\text{CE}}$# latency support (-A6F/A6FL)	1	1	0	0	0	1	1	1	C7	CL = 2, 3
	(-B6F/B6FL)	1	1	0	0	0	1	0	1	C5	CL = 3

Notes:
1. All serial PD data are not protected. 0: Serial data, "driven Low", 1: Serial data, "driven High" These SPD are based on Intel specification (Rev.1.2A).
2. Regarding byte32 to 35, based on JEDEC Committee Ballot JC42.5-97-119.
3. Byte72 is manufacturing location code. (ex: In case of Japan, byte72 is 4AH. 4AH shows "J" on ASCII code.)
4. Regarding byte93 and 94, based on JEDEC Committee Ballot JC42.5-97-135. BCD is "Binary Coded Decimal".
5. All bits of 99 through 125 are not defined ("1" or "0").
6. Bytes 95 through 98 are assembly serial number.

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	–0.5 to V_{CC} + 0.5 (≤ 4.6 (max))	V	1
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V	1
Short circuit output current	Iout	50	mA	
Power dissipation	P_T	16	W	
Operating temperature	Topr	0 to +65	°C	
Storage temperature	Tstg	–55 to +125	°C	

Note: 1. Respect to V_{SS}.

DC Operating Conditions (Ta = 0 to +65°C)

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage	V_{CC}	3.0	3.6	V	1, 2
	V_{SS}	0	0	V	3
Input high voltage	V_{IH}	2.0	V_{CC} + 0.3	V	1, 4, 5
Input low voltage	V_{IL}	–0.3	0.8	V	1, 6

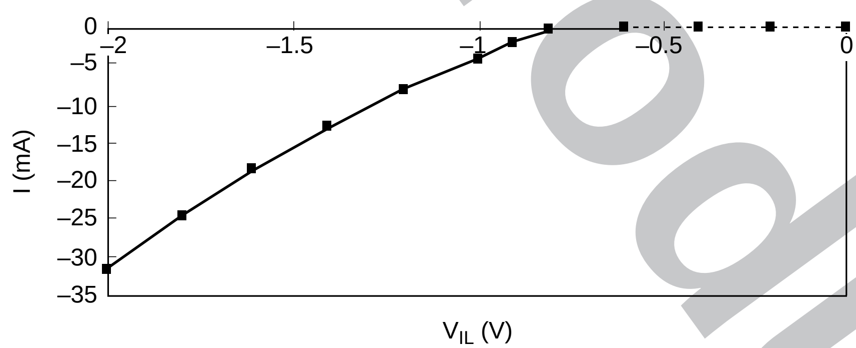
Notes: 1. All voltage referred to V_{SS}
2. The supply voltage with all V_{CC} pins must be on the same level.
3. The supply voltage with all V_{SS} pins must be on the same level.
4. CK, CKE, $\overline{S}$, DQMB, DQ pins: V_{IH} (max) = V_{CC} + 0.5 V for pulse width ≤ 5 ns at V_{CC}.
5. Others: V_{IH} (max) = 4.6 V for pulse width ≤ 5 ns at V_{CC}.
6. V_{IL} (min) = –1.0 V for pulse width ≤ 5 ns at V_{SS}.

V_{IL}/V_{IH} Clamp (Component characteristic)

This SDRAM component has V_{IL} and V_{IH} clamp for CK, CKE, $\overline{S}$, DQMB and DQ pins.

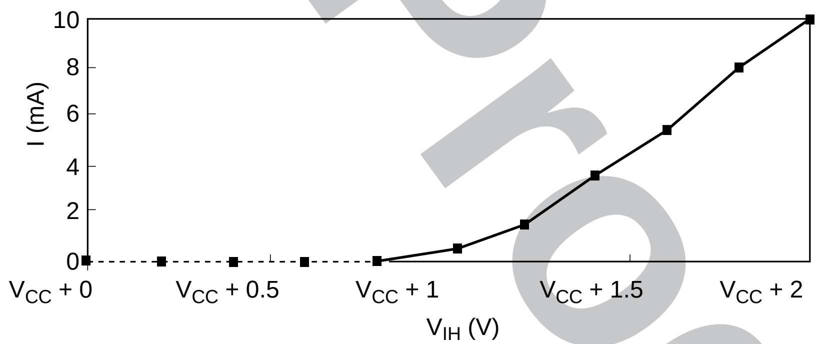
Minimum V_{IL} Clamp Current

V_{IL} (V)	I (mA)
–2	–32
–1.8	–25
–1.6	–19
–1.4	–13
–1.2	–8
–1	–4
–0.9	–2
–0.8	–0.6
–0.6	0
–0.4	0
–0.2	0
0	0



Minimum V_{IH} Clamp Current

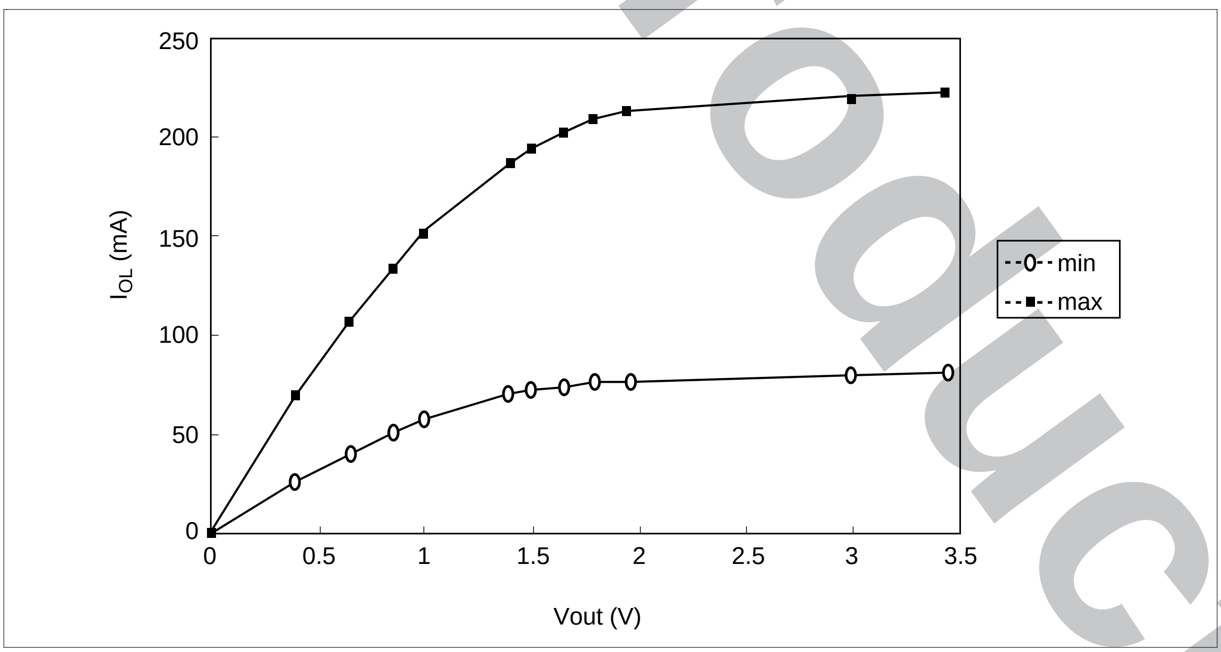
V_{IH} (V)	I (mA)
V_{CC} + 2	10
V_{CC} + 1.8	8
V_{CC} + 1.6	5.5
V_{CC} + 1.4	3.5
V_{CC} + 1.2	1.5
V_{CC} + 1	0.3
V_{CC} + 0.8	0
V_{CC} + 0.6	0
V_{CC} + 0.4	0
V_{CC} + 0.2	0
V_{CC} + 0	0



I_{OL}/I_{OH} Characteristics (Component characteristic)

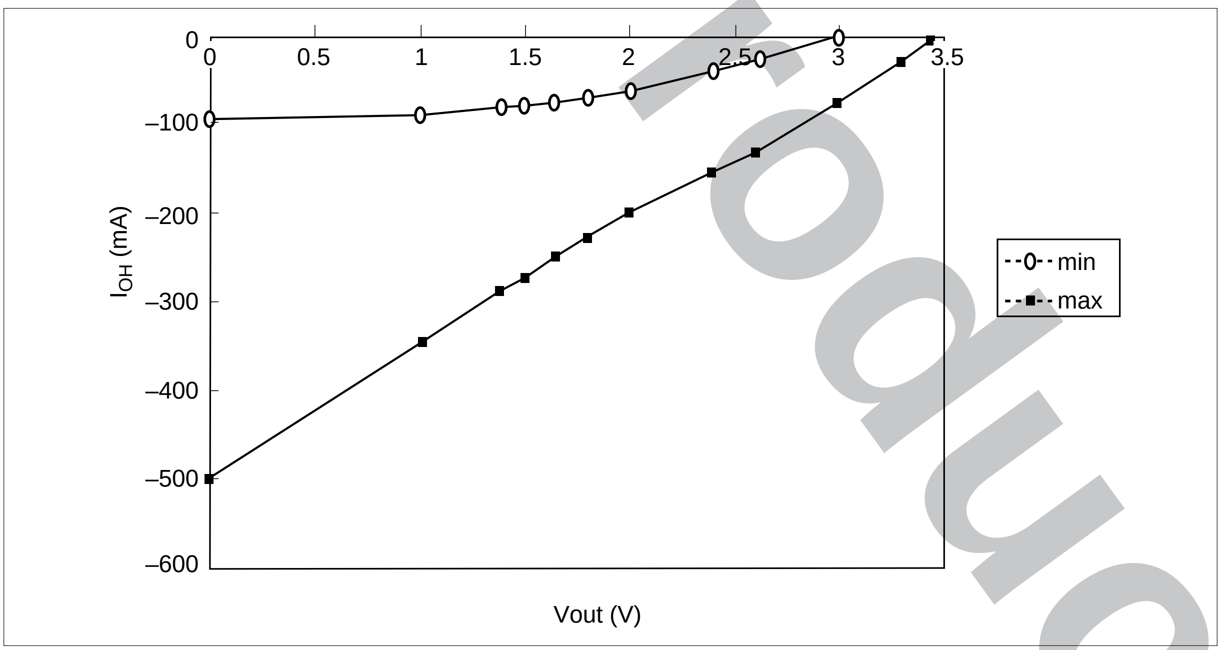
Output Low Current (I_{OL})

Vout (V)	I_{OL} Min (mA)	I_{OL} Max (mA)
0	0	0
0.4	27	71
0.65	41	108
0.85	51	134
1	58	151
1.4	70	188
1.5	72	194
1.65	75	203
1.8	77	209
1.95	77	212
3	80	220
3.45	81	223



Output High Current (I_{OH}) (Ta = 0 to 65˚C, V_{CC} = 3.0 V to 3.45 V, V_{SS} = 0 V)

Vout (V)	I_{OH} Min (mA)	I_{OH} Max (mA)
3.45	—	–3
3.3	—	–28
3	0	–75
2.6	–21	–130
2.4	–34	–154
2	–59	–197
1.8	–67	–227
1.65	–73	–248
1.5	–78	–270
1.4	–81	–285
1	–89	–345
0	–93	–503



DC Characteristics (Ta = 0 to 65°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

		HB52RD168GB				
		-A6F/B6F/A6FL/B6FL				
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	960	mA	Burst length = 1 t_{RC} = min	1, 2, 3
Standby current in power down	I_{CC2P}	—	24	mA	CKE0 = V_{IL}, t_{CK} = 12 ns	6
Standby current in power down (input signal stable)	I_{CC2PS}	—	16	mA	CKE0 = V_{IL}, t_{CK} = ∞	7
Standby current in non power down	I_{CC2N}	—	160	mA	CKE0, $\overline{S}$ = V_{IH}, t_{CK} = 12 ns	4
Active standby current in power down	I_{CC3P}	—	64	mA	CKE0, $\overline{S}$ = V_{IH}, t_{CK} = 12 ns	1, 2, 6
Active standby current in non power down	I_{CC3N}	—	288	mA	CKE0, $\overline{S}$ = V_{IH}, t_{CK} = 12 ns	1, 2, 4
Burst operating current	I_{CC4}	—	880	mA	t_{CK} = min, BL = 4	1, 2, 5
Refresh current	I_{CC5}	—	1760	mA	t_{RC} = min	3
Self refresh current	I_{CC6}	—	16	mA	V_{IH} ≥ V_{CC} – 0.2 V V_{IL} ≤ 0.2 V	8
Self refresh current (L-version)	I_{CC6}	—	9	mA		
Input leakage current	I_{LI}	–10	10	µA	0 ≤ Vin ≤ V_{CC}	
Output leakage current	I_{LO}	–10	10	µA	0 ≤ Vout ≤ V_{CC} DQ = disable	
Output high voltage	V_{OH}	2.4	—	V	I_{OH} = –4 mA	
Output low voltage	V_{OL}	—	0.4	V	I_{OL} = 4 mA	

Notes:
1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signals are changed once per one clock.
4. Input signals are changed once per two clocks.
5. Input signals are changed once per four clocks.
6. After power down mode, CK0/CK1 operating current.
7. After power down mode, no CK0/CK1 operating current.
8. After self refresh mode set, self refresh current.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V)

Parameter	Symbol	Max	Unit	Notes
Input capacitance (Address)	C_{IN}	90	pF	1, 2, 4
Input capacitance ($\overline{RE}$, $\overline{CE}$, $\overline{W}$, $\overline{S0}$, CKE0)	C_{IN}	90	pF	1, 2, 4
Input capacitance (CK0/CK1)	C_{IN}	60	pF	1, 2, 4
Input capacitance (DQMB0 to DQMB7)	C_{IN}	20	pF	1, 2, 4
Input/Output capacitance (DQ0 to DQ63)	$C_{I/O}$	20	pF	1, 2, 3, 4

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. Measurement condition: f = 1 MHz, 1.4 V bias, 200 mV swing.
3. DQMB = V_{IH} to disable Data-out.
4. This parameter is sampled and not 100% tested.

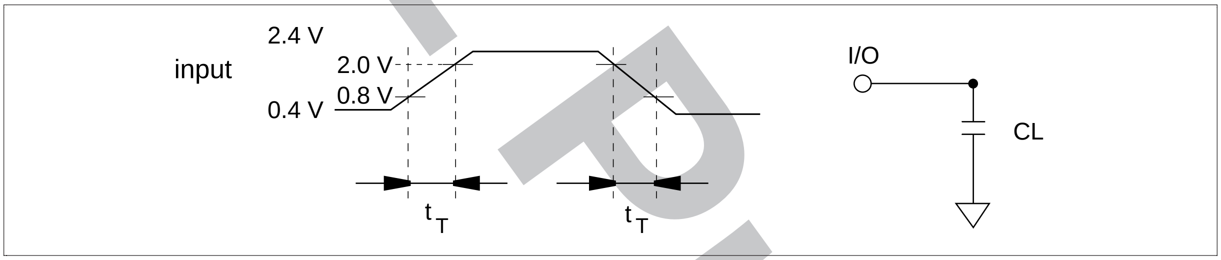
AC Characteristics (Ta = 0 to 65˚C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	PC100 Symbol	HB52RD168GB -A6F/A6FL Min	-A6F/A6FL Max	-B6F/B6FL Min	-B6F/B6FL Max	Unit	Notes
System clock cycle time ($\overline{CE}$ latency = 2)	t_{CK}	Tclk	10	—	15	—	ns	1
($\overline{CE}$ latency = 3)	t_{CK}	Tclk	10	—	10	—	ns	
CK high pulse width	t_{CKH}	Tch	3	—	3	—	ns	1
CK low pulse width	t_{CKL}	Tcl	3	—	3	—	ns	1
Access time from CK ($\overline{CE}$ latency = 2)	t_{AC}	Tac	—	6	—	8	ns	1, 2
($\overline{CE}$ latency = 3)	t_{AC}	Tac	—	6	—	6	ns	
Data-out hold time	t_{OH}	Toh	3	—	3	—	ns	1, 2
CK to Data-out low impedance	t_{LZ}		2	—	2	—	ns	1, 2, 3
CK to Data-out high impedance	t_{HZ}		—	6	—	6	ns	1, 4
Data-in setup time	t_{AS}, t_{CS}, t_{DS}, t_{CES}	Tsi	2	—	2	—	ns	1, 5, 6
CKE setup time for power down exit	t_{CESP}	Tpde	2	—	2	—	ns	1
Data-in hold time	t_{AH}, t_{CH}, t_{DH}, t_{CEH}	Thi	1	—	1	—	ns	1, 5
Ref/Active to Ref/Active command period	t_{RC}	Trc	70	—	70	—	ns	1
Active to Precharge command period	t_{RAS}	Tras	50	120000	50	120000	ns	1
Active command to column command (same bank)	t_{RCD}	Trcd	20	—	20	—	ns	1
Precharge to active command period	t_{RP}	Trp	20	—	20	—	ns	1
Write recovery or data-in to precharge lead time	t_{DPL}	Tdpl	10	—	10	—	ns	1
Active (a) to Active (b) command period	t_{RRD}	Trrd	20	—	20	—	ns	1
Transition time (rise and fall)	t_T		1	5	1	5	ns	
Refresh period	t_{REF}		—	64	—	64	ms	

Notes: 1. AC measurement assumes t_T = 1 ns. Reference level for timing of input signals is 1.5 V.
2. Access time is measured at 1.5 V. Load condition is CL = 50 pF.
3. t_{LZ} (min) defines the time at which the outputs achieves the low impedance state.
4. t_{HZ} (max) defines the time at which the outputs achieves the high impedance state.
5. t_{CES} define CKE setup time to CK rising edge except power down exit command.
6. t_{AS}/t_{AH}: Address, t_{CS}/t_{CH}: $\overline{S}$, $\overline{RE}$, $\overline{CE}$, $\overline{W}$, DQMB
t_{DS}/t_{DH}: Data-in, t_{CES}/t_{CEH}: CKE

Test Conditions

- Input and output timing reference levels: 1.5 V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency

Parameter			HB52RD168GB -A6F/A6FL/B6F/B6FL	
Frequency (MHz)			100	
t_{CK} (ns)	Symbol	PC100 Symbol	10	Notes
Active command to column command (same bank)	l_{RCD}		2	1
Active command to active command (same bank)	l_{RC}		7	= [l_{RAS}+ l_{RP}] 1
Active command to precharge command (same bank)	l_{RAS}		5	1
Precharge command to active command (same bank)	l_{RP}		2	1
Write recovery or data-in to precharge command (same bank)	l_{DPL}	Tdpl	1	1
Active command to active command (different bank)	l_{RRD}		2	1
Self refresh exit time	l_{SREX}	Tsrx	1	2
Last data in to active command (Auto precharge, same bank)	l_{APW}	Tdal	3	= [l_{DPL} + l_{RP}]
Self refresh exit to command input	l_{SEC}		7	= [l_{RC}] 3
Precharge command to high impedance ($\overline{CE}$ latency = 2)	l_{HZP}	Troh	2	
($\overline{CE}$ latency = 3)	l_{HZP}	Troh	3	
Last data out to active command (auto precharge) (same bank)	l_{APR}		1	
Last data out to precharge (early precharge) ($\overline{CE}$ latency = 2)	l_{EP}		–1	
($\overline{CE}$ latency = 3)	l_{EP}		–2	
Column command to column command	l_{CCD}	Tccd	1	
Write command to data in latency	l_{WCD}	Tdwd	0	
DQMB to data in	l_{DID}	Tdqm	0	
DQMB to data out	l_{DOD}	Tdqz	2	
CKE to CK disable	l_{CLE}	Tcke	1	
Register set to active command	l_{RSA}	Tmrd	1	

Parameter			HB52RD168GB -A6F/A6FL/B6F/B6FL	
Frequency (MHz)			100	
t_{CK} (ns)	Symbol	PC100 Symbol	10	Notes
$\overline{S}$ to command disable	l_{CDD}		0	
Power down exit to command input	l_{PEC}		1	
Burst stop to output valid data hold ($\overline{CE}$ latency = 2)	l_{BSR}		1	
($\overline{CE}$ latency = 3)	l_{BSR}		2	
Burst stop to output high impedance ($\overline{CE}$ latency = 2)	l_{BSH}		2	
($\overline{CE}$ latency = 3)	l_{BSH}		3	
Burst stop to write data ignore	l_{BSW}		0	

Notes: 1. l_{RCD} to l_{RRD} are recommended value.
2. Be valid [DSEL] or [NOP] at next command of self refresh exit.
3. Except [DSEL] and [NOP].

Pin Functions

CK0/CK1 (input pin): CK is the master clock input to this pin. The other input signals are referred at CK rising edge.

$\overline{\text{S0}}$ (input pin): When $\overline{\text{S}}$ is Low, the command input cycle becomes valid. When $\overline{\text{S}}$ is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

$\overline{\text{RE}}$, $\overline{\text{CE}}$ and $\overline{\text{W}}$ (input pins): Although these pin names are the same as those of conventional DRAM modules, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.

A0 to A11 (input pins): Row address (AX0 to AX11) is determined by A0 to A11 level at the bank active command cycle CK rising edge. Column address (AY0 to AY9) is determined by A0 to A9 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by A12/A13 (BA) is precharged.

A12/A13 (input pin): A12/A13 is a bank select signal (BA). The memory array is divided into bank0, bank1, bank2 and bank3. If A12 is Low and A13 is Low, bank0 is selected. If A12 is High and A13 is Low, bank1 is selected. If A12 is Low and A13 is High, bank2 is selected. If A12 is High and A13 is HIgh, bank3 is selected.

CKE0, CKE1 (input pin): This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.

DQMB0 to DQMB7 (input pins): Read operation: If DQMB is High, the output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z.

Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.

DQ0 to DQ63 (DQ pins): Data is input to and output from these pins.

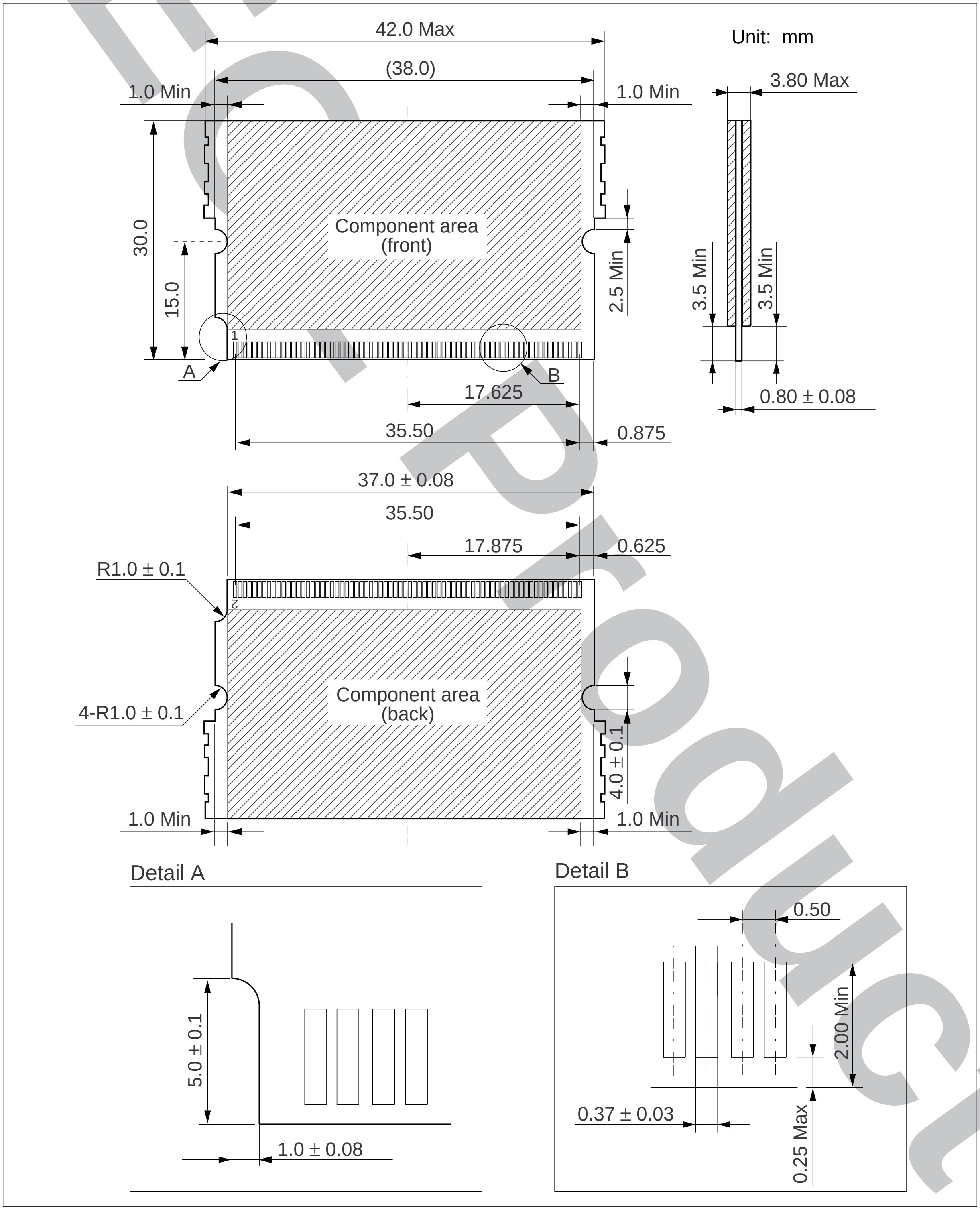
V_{CC} (power supply pins): 3.3 V is applied.

V_{SS} (power supply pins): Ground is connected.

Detailed Operation Part

Refer to the HM5264165F/HM5264805F/HM5264405F-75/A60/B60 datasheet.

Physical Outline



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