High Performance 128K×8 CMOS Flash EEPROM

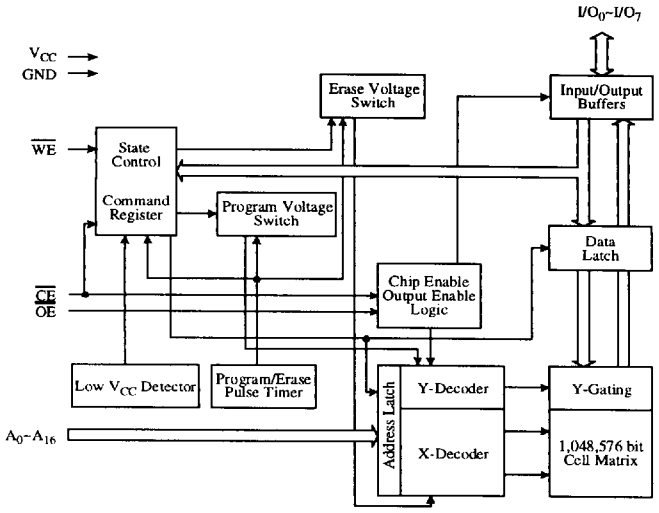
AS29F010
AS29F011

5V 128K×8 CMOS Flash Memory

FEATURES

- Organization:131,072 words × 8 bits
- Sector Erase architecture
  - Four 32K × 8 sectors
- Single 5.0±0.5V power supply
- High speed 70/90/120/150 ns address access time
- Low power consumption:
  - 30 mA maximum read current
  - 50 mA maximum program current
  - 1.5 mA maximum standby current
  - 1 mA maximum standby current (low power)
- Deep power-down: I_{CC} < 2μA (AS29F011 version)
- 10,000 write/erase cycle endurance
- JEDEC standard write cycle commands
  - protects data from accidental changes
- Program/erase cycle end signals:
  - $\overline{\text{Data}}$ polling
  - I/O6 toggle
- Low V_{CC} write lock-out below 3.2V
- JEDEC standard packages and pinouts:
  - 32-pin DIP
  - 32-pin PLCC
  - 32-pin TSOP

LOGIC BLOCK DIAGRAM



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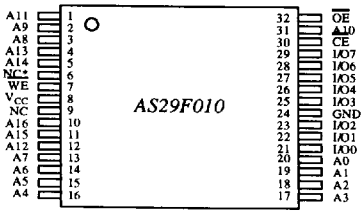
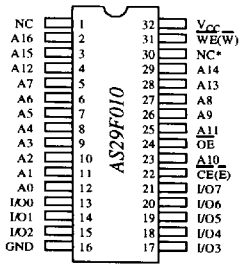
PIN ARRANGEMENT

TSOP



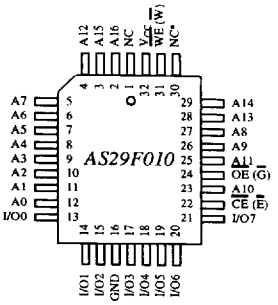
Pin	Description
A[16:0]	address inputs
I/O[7:1]	data input/output
$\overline{CE}$	chip enable
$\overline{OE}$	output enable
$\overline{WE}$	write enable
GND	device ground
V_{CC}	power supply
NC	no connect
RP	deep power down (AS29F011 only)

PDIP



*RP pin for AS29F011

PLCC



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SELECTION GUIDE

		29F010-70	29F010-90	29F010-120	29F010-150	Unit
Maximum access time	t_{AA}	70	90	120	150	ns
Chip enable access time	t_{CE}	70	90	120	150	ns
Output enable access time	t_{OE}	30	35	50	50	ns

FUNCTIONAL DESCRIPTION

The AS29F010 and AS29F011 are high performance 1 megabit byte wide Flash EEPROM memories. They are organized as 131,072 words × 8 bits, and divided into four sectors of 32K bytes each. Each sector is separately erased and programmed without affecting data in the other sectors. All program, erase, and verify operations are 5-volt only, and require no external 12V supply pin. All required features for in-system programmability are provided.

The AS29F010 and AS29F011 provide high performance with a maximum access time of 70, 90, 120, or 150 ns. Chip Enable ($\overline{CE}$), Output Enable ($\overline{OE}$), and Write Enable ($\overline{WE}$) pins allow easy interface with the system bus. The AS29F011 is functionally identical to the AS29F010 except for an additional input RP, which controls a deep power-down function. When the RP pin is pulled low (less than V_{IL}) the AS29F011 is disabled, reducing power consumption to virtually zero. The AS29F011 recovers in <2 µs when RP is pulled high.

Program, erase, and verify operations are controlled with an on-chip command register using a JEDEC standard Write State Machine approach to enter commands. Each command requires four write cycles to be executed. Address and data are latched internally during all write, erase, and verify operations, and an internal timer terminates each command. The chip has a typical timer period of 200 µs for all commands but Erase, which has a typical period of 800 ms. Under nominal conditions, a sector can be completely programmed and verified in less than 12 seconds. To program, erase, and verify a sector typically takes less than 18 seconds.

Data protection is provided by a low-V_{CC} lockout and by error checking in the Write State Machine. Data-bar polling and Toggle Bit modes are used to show that the chip is executing a command when the AS29F010 or AS29F011 is read during a write or erase operation. After Erase or Program commands, Verify-1 and Verify-0 command modes ensure sufficient margin for reliable operation. (See command summary on page 5.)

The AS29F010 and AS29F011 are packaged in 32-pin DIP, PLCC and TSOP packages with JEDEC standard pinouts for one megabit Flash memories.

ARRAY ARCHITECTURE AND DATA POLARITY

The array consists of 128K (131,072) bytes divided into four sectors of 32K bytes each. Addresses A15 and A16 select the four sectors:

Sector	Address Range
0	00000h–07FFFh
1	08000h–0FFFFh
2	10000h–17FFFh
3	18000h–1FFFFh

The AS29F010 and AS29F011 are shipped in the erased state with all bits set to 1. Programmed bits are set to 0. Data is programmed into the array one byte at a time. Within a programmed byte, any bit that remains set to 1 can be programmed to 0 later, but all programmed bits remain set to 0 until the sector is erased and verified using the Sector Erase and Verify algorithm. Erase returns all bytes in a 32K sector to the erased state FFh, or all bits set to 1. Each sector is erased individually with no effect on the other sectors.

Address Pins	Function
A0–A5	CA: Column addresses 00–3Fh
A6–A14	RA: Row addresses 000–1FFh
A15–A16	SA: Sector addresses 0–3h

OPERATING MODES

The AS29F010 and AS29F011 are controlled by a Write State Machine (WSM) that interprets and executes commands. At power-up the WSM is reset to normal mode, which allows the chip to operate as a ROM. Once a command is initiated by writing data into the I/O pins with the $\overline{WE}$ pin, the WSM enters the command mode and keeps the chip powered up until the command is finished. After the command is terminated by the internal timer, the WSM returns to the normal mode and the chip may be read as a ROM.

The RP pin of the AS29F011 overrides all other inputs. Any operation in progress is interrupted when the RP pin is pulled low.

MODE TABLE

Mode	RP†	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A9	I/O
Deep power down	L	X	X	X	X	X	HI-Z
Read	H	L	L	H	A0	A9	D_{OUT}
Output disable	H	L	H	H	X	X	HI-Z
Standby	H	H	H	H	X	X	HI-Z
Mfr. code	H	L	L	H	L	Vh	52h
Part code	H	L	L	H	H	Vh	03h
Write command	H	L	H	L	A0	A9	D_{IN}

†RP is used only on the AS29F011. **Key:** L =Low ($<V_{IL}$); H = High ($>V_{IH}$); Vh = 11.5–12.5V; X =Don't care

Deep power down: (AS29F011 only): RP low; all DC power disabled. This interrupts any command in progress.

Read mode: Selected with $\overline{CE}$ and $\overline{OE}$ low, $\overline{WE}$ high. Data is valid T_{aa} after addresses are stable, T_{CE} after $\overline{CE}$ is low and T_{OE} after $\overline{OE}$ is low.

Output disable: Part remains powered up; but outputs disabled with $\overline{OE}$ pulled high.

Standby: Part is powered down, and I_{CC} reduced to 1.5 mA for TTL input levels (<1.0 mA for CMOS input levels).

Mfr. (manufacturer) **code, Part code**: Selected by A9 = 11.5–12.5V per the JEDEC standard for non-volatile memories. When $\overline{CE}$ and $\overline{OE}$ are pulled low the outputs are enabled and a data byte is read out. When A0 is pulled low the output data = 52h, a unique Mfr. code for Alliance Semiconductor Flash products. When A0 is high D_{OUT} = 03h, the Alliance part code for the AS29F010.

Write command: Selected by $\overline{CE}$ and $\overline{WE}$ pulled low, $\overline{OE}$ pulled high. Initiates command mode in the WSM and latches addresses and data into the chip. Once a write command starts, the WSM stays in command mode until the command is completed or it times out. Addresses are latched on the falling edge of $\overline{WE}$ and $\overline{CE}$; data is latched on the rising edge. The $\overline{WE}$ signal is filtered to prevent spurious events from being detected as write commands.

COMMAND FORMAT

All commands require four bus write cycles to execute. After four write cycles the command executes until terminated by the internal timer. For verify commands a read operation after $Write_{[4]}$ in a write command bus cycle reads out the data from the array. For manufacturer and part code commands the ID code is read out. For other operations a read operation reads out a status byte on the outputs.

	ADDRESS IN	DATA IN
Bus $Write_{[1]}$	5555h	AAh
Bus $Write_{[2]}$	2AAAh	55h
Bus $Write_{[3]}$	5555h	Command code
Bus $Write_{[4]}$	Address in	Data in
Bus read	Address in	D_{OUT}

Command timeout: For each operation the address and data are latched at bus $Write_{[4]}$ and held until the operation completes and times-out. After time-out the WSM returns the AS29F010 to normal mode. Each individual operation requires the 4-cycle write command sequence to execute. The AS29F010 does not remain in command mode after time-out. When a command times-out only the error flag is not reset.

Errors and timeout: Any of the following conditions sets the error flag.

- Any write command which does not match the sequence above for $Write_{[1]}$, $Write_{[2]}$, and $Write_{[3]}$.
- Any write cycle that follows more than 150 µs after the previous write cycle.
- The command $Data_{[3]}$ in $Write_{[3]}$ has more than one bit set high. This indicates conflicting commands.
- V_{CC} drops below V_{LKO} during command execution.

Once the error flag is set, the AS29F010 times out and returns to normal mode. The error flag remains until it is cleared by a reset command. The error flag can be read by executing a status command and reading the status byte.

COMMAND CODES AND TIME-OUT

The Command Code table displays the bus cycles required for each command mode. Read delay is the minimum delay after $Write_{[4]}$ during a write command bus cycle before a valid read may be executed. Timeout indicates the maximum delay before the WSM returns the AS29F010 to normal mode. Erase has a longer timeout than the other modes. Status byte can be read almost immediately after a $Write_{[4]}$, but the verify commands require a 25 µs delay to read valid data.

COMMAND CODE TABLE

Mode	$D_{IN[3]}$ $Write_{[3]}$ Data	$A_{IN[4]}$ $Write_{[4]}$ Addr.	$D_{IN[4]}$ Data	Read Addr.	Read Data	Read Delay	Maximum Time Out
Reset	00h	x	x	0000h	Status	100 ns	250 µs
Status	01h	x	x	0000h	Status	100 ns	250 µs
Mfr. Code	02h	0000h	x	0000h	MCODE	100 ns	250 µs
		0001h	x	0001h	PCODE	100 ns	
Verify-0	04h	A_{IN}	x	A_{IN}	D_{OUT}	25 µs	250 µs
Verify-1	08h	A_{IN}	x	A_{IN}	D_{OUT}	25 µs	250 µs
Converge	10h	A_{IN}	00h	A_{IN}	Status	100 ns	250 µs
Program	40h	A_{IN}	D_{IN}	A_{IN}	Status	100 ns	250 µs
Erase	80h	A_{IN}	FFh	A_{IN}	Status	100 ns	1000 µs

Note: Code 02h is not used.

COMMAND ALGORITHMS

Individual write commands are used together in eight program and erase algorithms to guarantee the 29F010 operating margins for the life of the part. Refer to the AS29F010 Programming Specification for details on the algorithms for program and erase operations.

RECOMMENDED OPERATING CONDITIONS

(T_a = 0°C to +70°C)

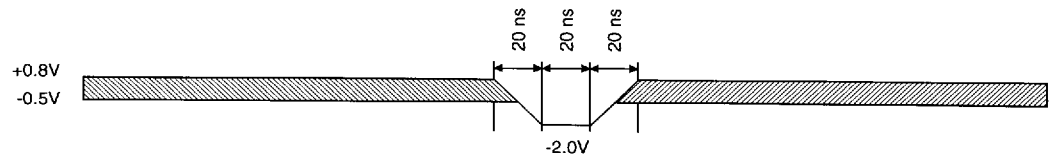
Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.0	-	V_{CC} + 1.0	V
	V_{IL}	–0.5	-	0.8	V

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Input Voltage (Input or I/O pin)	V_{IN}	–1.0	V_{CC} + 1.0	V
Input Voltage (A9 pin)	V_{IN}	–1.0	+13.0	V
Output Voltage	V_{OUT}	–1.0	V_{CC} + 1.0	V
Power Supply Voltage	V_{CC}	+4.5	+5.5	V
Operating Temperature	T_{OPR}	–55	+125	°C
Storage Temperature (Plastic)	T_{STG}	–65	+125	°C
Short Circuit Output Current	I_{OUT}	-	100	mA
Latch-up Current	I_{IN}	-	±100	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

MAXIMUM NEGATIVE OVERSHOOT WAVEFORM



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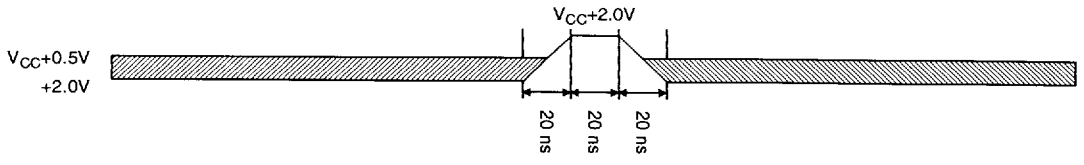
MAXIMUM POSITIVE OVERSHOOT WAVEFORM



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DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0±0.5V, GND = 0V, T_a = 0°C to +70°C

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input load current	I_{LI}		-	±1	µA
Output leakage current	I_{LO}		-	±1	µA
Output short circuit current	I_{OS}	V_{OUT} = 0.5V	-	100	mA
Active current, read @ 6MHz	I_{CC}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	-	30	mA
Active current, program/erase	I_{CCPRG}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	-	50	mA
I_{CC}	I_{SB1}	$\overline{CE}$ = V_{IH}	-	1.5	mA
	I_{SB2}	$\overline{CE}$ = V_{CC}	-	1.0	mA
	I_{CCPD}	$\overline{RP}$ = 0V	-	2	µA
Input: low level	V_{IL}		0.8	-	V
Input: high level	V_{IH}		-	2	V
Output low voltage	V_{OL}	I_{OL} = 12mA	-	0.45	V
Output high level	V_{OH1}	I_{OH} = -2.5 mA	2.4	-	V
	V_{OH2}	I_{OH} = -100 µA	V_{CC} - 0.4	-	V
Low V_{CC} lock out voltage	V_{LKO}		3.2	-	V
Input HV select voltage	V_{HH}		11.5	12.5	V

Notes:

- Not more than one output tested simultaneously. Duration of the short circuit must not be >1 second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. (This parameter is sampled and not 100% tested, but guaranteed by characterization.)
- The I_{CC} current listed includes both the DC operating current and the frequency dependent component (@ 6 MHz). The frequency component typically is less than 2 mA/MHz with $\overline{OE}$ at V_{IH}.
- I_{CC} active while program or erase operations are in progress.

AC PARAMETERS–READ CYCLE

(V_{CC} = 5.0±0.5V, GND = 0V, T_a = 0°C to +70°C)

JEDEC Symbol	Std Symbol	Parameter	-70 Min	-70 Max	-90 Min	-90 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
t_{AVAV}	t_{RC}	Read cycle time	70	-	90	-	120	-	150	-	ns
t_{AVQV}	t_{ACC}	Address to output delay	-	70	-	90	-	120	-	150	ns
t_{ELQV}	t_{CE}	Chip enable to output	-	70	-	90	-	120	-	150	ns
t_{GLQV}	t_{OE}	Output enable to output	-	30	-	35	-	50	-	50	ns
t_{EHQZ}	t_{DF}	Chip enable to output high-Z	-	20	-	20	-	30	-	30	ns
t_{GHQZ}	t_{DF}	Output enable to output high-Z	-	20	-	20	-	30	-	30	ns
t_{AXQX}	t_{OH}	Output hold time from addresses, first occurrence of $\overline{CE}$ or $\overline{OE}$	-	0	-	0	-	0	-	0	ns
	t_{PWH}	RP Power up recovery time†	-	1	-	1	-	1	-	1	µs

†Applies to version AS29F011 only.

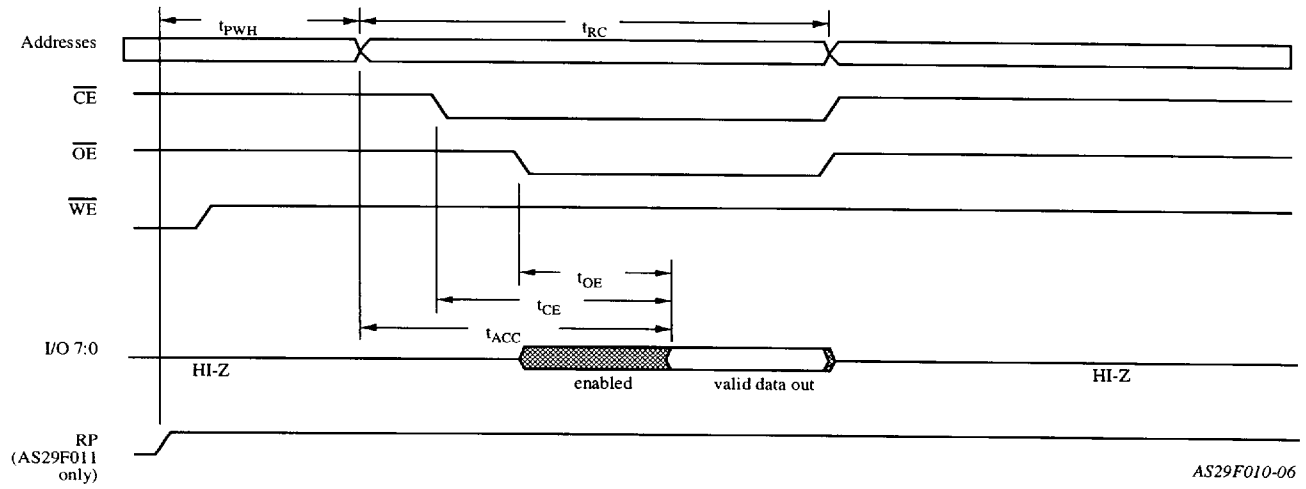
AC PARAMETERS–WRITE CYCLE

(V_{CC} = 5.0±0.5V, GND = 0V, T_a = 0°C to +70°C)

JEDEC Symbol	Std Symbol	Parameter	-70 Min	-70 Max	-90 Min	-90 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
t_{AVAV}	t_{WC}	Write cycle time	-	70	-	90	-	120	-	150	ns
t_{AVWL}	t_{AS}	Address setup time	-	0	-	0	-	0	-	0	ns
t_{WLAX}	t_{AH}	Address hold time	-	45	-	45	-	50	-	50	ns
t_{DVWH}	t_{DS}	Data setup time	-	30	-	45	-	50	-	50	ns
t_{WHDX}	t_{DH}	Data hold time	-	0	-	0	-	0	-	0	ns
	t_{OES}	Output enable setup time	-	0	-	0	-	0	-	0	ns
	t_{OEH}	Output enable hold time: Read	-	0	-	0	-	0	-	0	ns
		Output enable hold time: Toggle and data polling	-	10	-	10	-	10	-	10	ns
t_{GHWL}	t_{GHWL}	Read recover time before write	-	0	-	0	-	0	-	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ setup time	-	0	-	0	-	0	-	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ hold time	-	0	-	0	-	0	-	0	ns
t_{WLWH}	t_{WP}	Write pulse width	-	35	-	45	-	80	-	80	ns
t_{WHWL}	t_{WPH}	Write pulse width high	-	20	-	20	-	20	-	20	ns
t_{WHWH1}	t_{WHWH1}	Programming pulse time	-	250	-	250	-	250	-	250	µs
t_{WHWH2}	t_{WHWH2}	Erase pulse time	-	1000	-	1000	-	1000	-	1000	µs
	t_{VCS}	V_{CC} setup time	-	2	-	2	-	2	-	2	µs

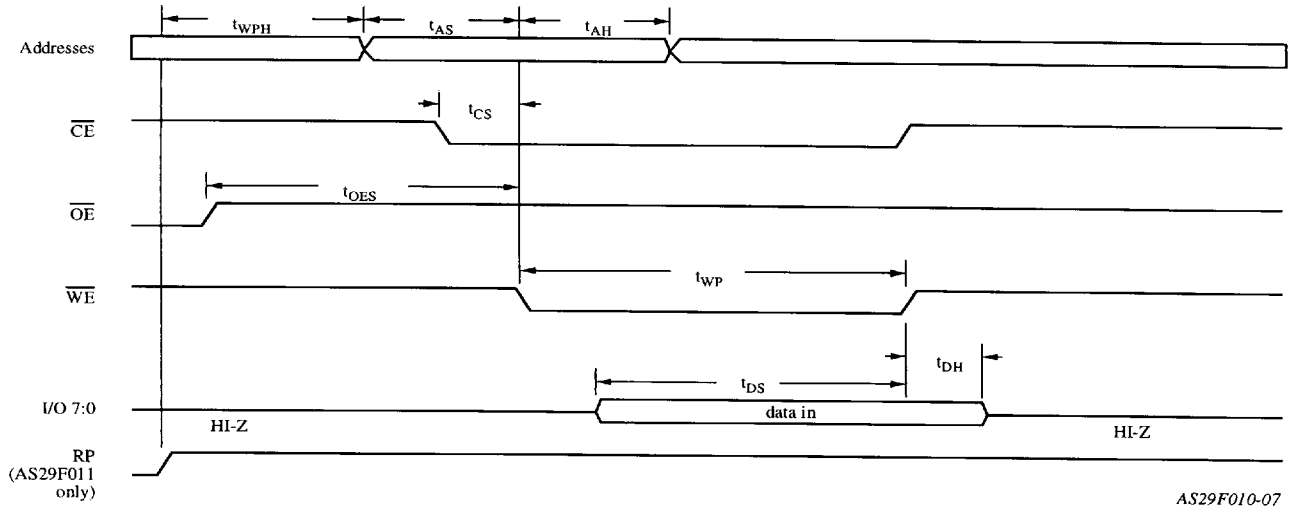
READ WAVEFORM

(V_{CC} = 5.0±0.5V, GND = 0V, T_a = 0°C to +70°C)



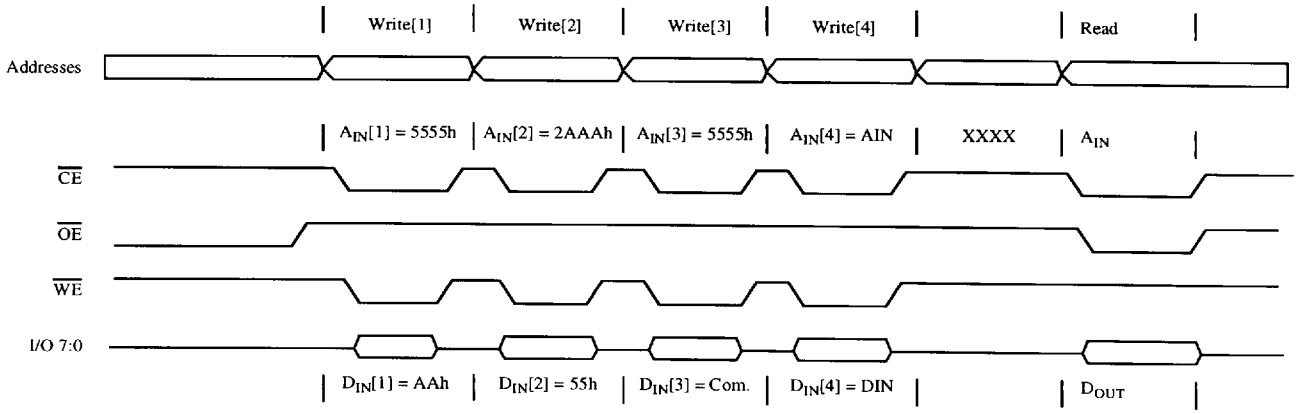
WRITE COMMAND WAVEFORM

(V_{CC} = 5.0±0.5V, GND = 0V, T_a = 0°C to +70°C)



WRITE COMMAND BUS CYCLE

(V_{CC} = 5.0±0.5V, GND = 0V, T_a = 0°C to +70°C)



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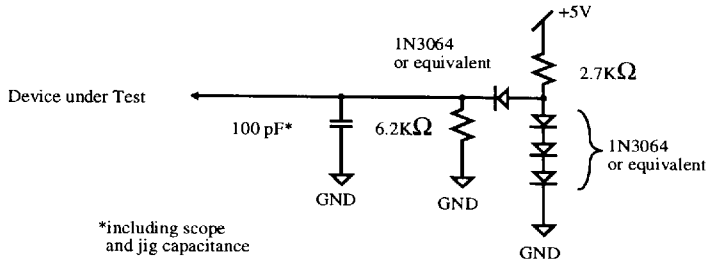
NOTES

- $A_{IN[4:1]}$, and $D_{IN[4:1]}$ = Address and Data for write cycles 1–4.
- D_{IN} = Data to be programmed at address A_{IN}.
- Com. = Command byte input on the I/O pins during $Write_{[3]}$.
- D_{OUT} = Status byte, Manufacturer ID code, or array data for verify.

AC TEST CONDITIONS



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LATCHUP CHARACTERISTICS

Parameter	Min	Max	Unit
Input voltage with respect to GND on pin A9	-1.0	+13.5	V
Input voltage with respect to GND (except I/O pins and A9)	-1.0	+10.0	V
Input voltage with respect to GND on all I/O pins	-1.0	V_{CC}+1.0	V
Current	-100	+100	mA

NOTE: Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0V, one pin at a time.

TSOP PIN CAPACITANCE

(f = 1 MHz, T_a = 25°C)

Symbol	Parameter	Test Setup	Typical	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control pin capacitance	V_{IN} = 0	7.5	9	µF

PLCC AND PDIP PIN CAPACITANCE

(f = 1 MHz, T_a = 25°C)

Symbol	Parameter	Test Setup	Typical	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0	4	6	pF
C_{OUT}	Output capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	Control pin capacitance	V_{IN} = 0	8	12	µF

DATA RETENTION

Parameter	Temperature	Min	Unit
Minimum pattern data retention time	150°	10	years
	125°	20	years

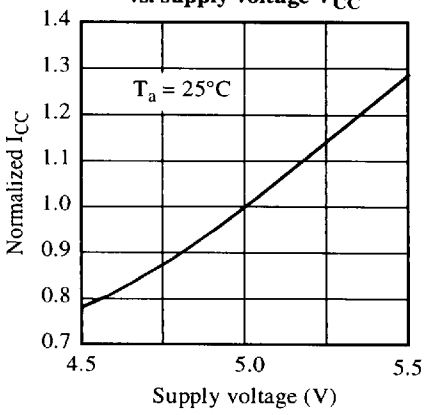
ERASE AND PROGRAMMING PERFORMANCE

(f = 1 MHz, T_a = Room Temperature, V_{CC} = 5V±10%)

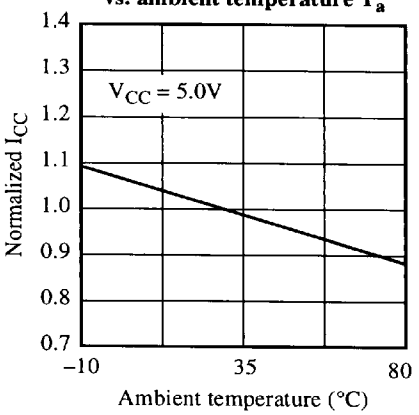
	Limits			
Parameter	Min	Typical	Max	Unit
Sector erase and Verify-1 time (excludes 00h programming prior to erase)	-	6.0	8.2	sec
Sector programming time	-	-	8.2	sec
Chip programming time	-	24	-	sec
Erase program cycles	10,000	-	-	cycles
Byte program time	-	200	250	µs
Bytc verify0 time	-	200	250	µs

PRELIMINARY DC AND AC CHARACTERISTICS

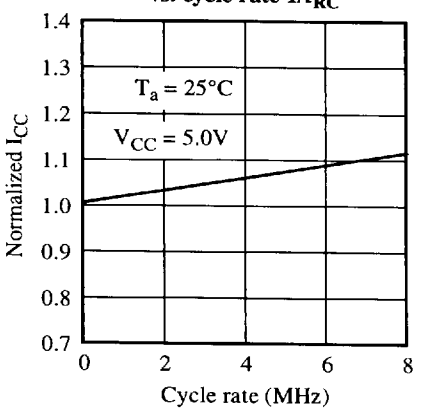
Normalized supply current I_{CC} vs. supply voltage V_{CC}



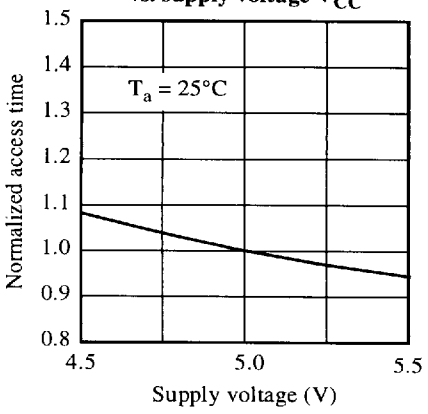
Normalized supply current I_{CC} vs. ambient temperature T_a



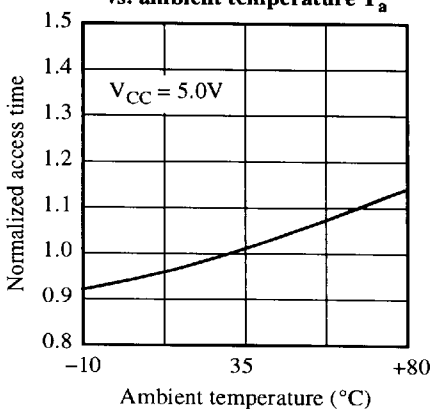
Normalized supply current I_{CC} vs. cycle rate $1/t_{RC}$



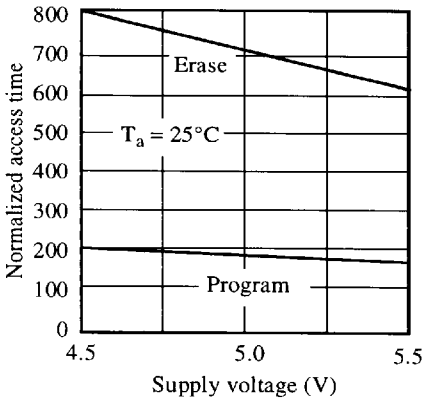
Normalized access time t_{AA} vs. supply voltage V_{CC}



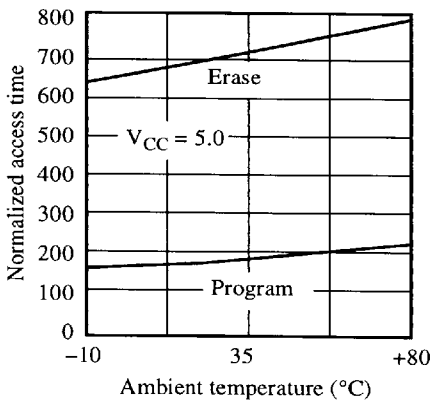
Normalized access time t_{AA} vs. ambient temperature T_a



Program/Erase time vs. V_{CC}



Program/Erase time vs. Temperature



AS29F010-11

ORDERING CODES

Package \ Access Time	70 ns	90 ns	120 ns	150 ns
Plastic DIP, 600 mil, 32-pin	AS29F010-70PC	AS29F010-90PC	AS29F010-120PC	AS29F010-150PC
PLCC, 32-pin	AS29F010-70LC	AS29F010-90LC	AS29F010-120LC	AS29F010-150LC
TSOP, 8×20 mm, 32-pin	AS29F010-70TC	AS29F010-90TC	AS29F010-120TC	AS29F010-150TC

PART NUMBERING SYSTEM

AS29F	010	–XX	X	C
Flash EEPROM Prefix	Device Number	Addr. Access Time	Package: P = PDIP 600 mil L = PLCC T = TSOP 8×20 mm	Commercial Temperature Range, 0°C to 70 °C

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