FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Univeral bus transceiver with D-type latches and D-type Flip-flops capabable of operating in transparant, latched or clocked mode.
- All inputs have bushold circuitry
- Output drive capability 50Ω transmission lines @ 85 °C
- 3-state non-inverting outputs for bus oriented applications

DESCRIPTION

The 74ALVC16601 is an 18-bit universal bus transceiver.
Data flow in each direction is controlled by output enable (OE_{AB}, $\overline{OE}_{BA}$), latch-enable (LE_{AB}, LE_{BA}) and clock inputs (CP_{AB}, CP_{BA}).
When LE_{AB} is HIGH, the A-B dataflow is transparant. When LE_{AB} is LOW, and CP_{AB} is held at LOW or HIGH, the A data is latched; on the LOW-to-HIGH transition of CP_{AB} the A-data is stored in the latch/flip-flop. The outputs are active when OE_{AB} is HIGH. When OE_{AB} is LOW the B-outputs are in 3-state.

Similarly, the LE_{BA}, $\overline{OE}_{BA}$ and CP_{BA} control the B-to-A dataflow. Please note that both output enables are complementary: OE_{AB} is active HIGH, $\overline{OE}_{BA}$ is active LOW.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n LE_{AB} to A_n	C_L = 50 pF V_{CC} = 3.3 V	3.0 3.2	ns
C_I	input capacitance		5.0	pF
$C_{I/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	22	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16601DL	56	SSOP56	plastic	SSOP56/SOT371
74ALVC16601DGG	56	TSSOP56	plastic	TSSOP56/SOT364

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_{AB}$	Output enable A-to-B
2	LE_{AB}	Latch enable A-to-B
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A_0 to A_{17}	'A' data inputs/outputs
4, 11, 18, 25, 29, 32, 39, 46, 53, 56	GND	ground (0 V)
7, 22, 35, 50	V_{CC}	positive supply voltage
27	$\overline{OE}_{BA}$	Output enable B-to-A
28	LE_{BA}	Latch enable B-to-A
30	CP_{BA}	Clock input B-to-A, HIGH-to-LOW
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B_0 to B_{17}	'B' data inputs/outputs
55	CP_{AB}	Clock input A-to-B, HIGH-to-LOW

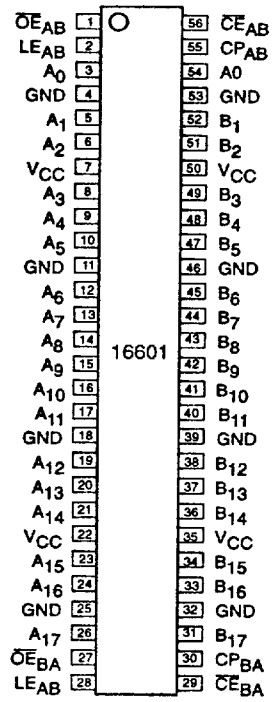


Fig.1 Pin configuration.

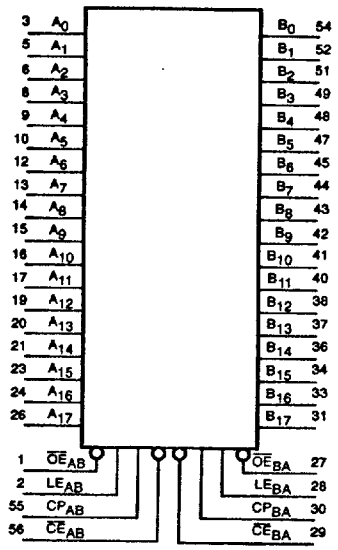


Fig.2 Logic symbol.

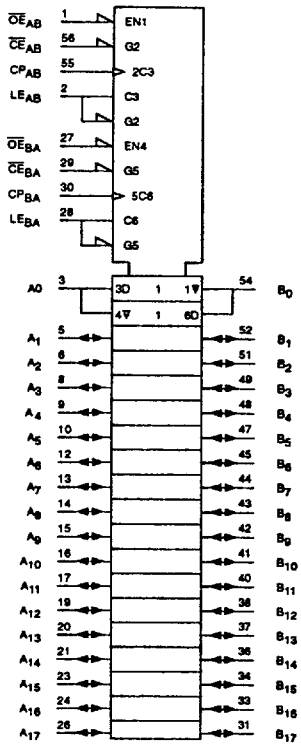


Fig.3 IEC Logic Symbol

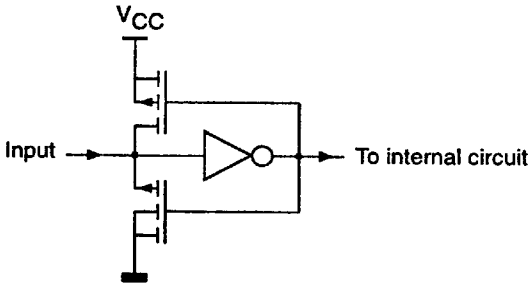


Fig.4 Bushold circuit

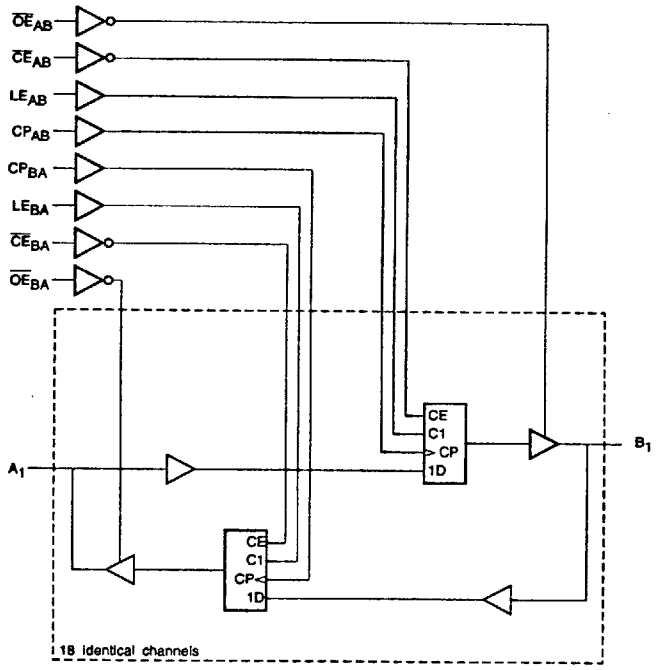


Fig.4 Logic diagram (one section)

FUNCTION TABLE

INPUTS					OUTPUTS	STATUS
$\overline{CE}_{xx}$	$\overline{OE}_{xx}$	LE_{xx}	CP_{xx}	DATA		
X	H	X	X	X	Z	Disabled
X X	L L	H H	X X	H L	H L	Transparant
H H	L L	L L	X X	X X	NC NC1	Hold
L L	L L	L L	↑ ↑	h l	Z Z	Disabled + latch
L L	L L	L L	↑ ↑	h l	H L	Latch + display
L L	L L	L L	L H	X X	NC NC1	Hold

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = High state must be present one setup time before the low-to-high transition of CP_{xx}
l = Low state must be present one setup time before the low-to-high transition of CP_{xx}
X = Don't care
↑ = LOW-to-HIGH level transition
NC = No change
NC1 = No change provided that CP_{xx} was LOW before LE_{xx} went low
Z = High impedance "off" state

DC CHARACTERISTICS FOR 74ALVC16601

For the DC characteristics see chapter "ALVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74ALVC16601

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 to +85				V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n, B_n to A_n	–	–	18.0	ns	1.2	Fig.6
		–	–	4.8		2.7	
		–	3.0*	4.4		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay LE_{BA} to A_n, LE_{AB} to B_n	–	–	20.0	ns	1.2	Fig.7
		–	–	6.0		2.7	
		–	3.2*	5.4		3.0 to 3.6	
t_{PHL}/t_{PLH}	propagation delay CP_{BA} to A_n, CP_{AB} to B_n	–	–	20.0	ns	1.2	
		–	–	6.0		2.7	
		–	3.2*	5.4		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to A_n, OE_{AB} to B_n	–	–	22.0	ns	1.2	Fig.8
		–	–	6.1		2.7	
		–	–	5.5		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{BA} to A_n, OE_{AB} to B_n	–	–	22.0	ns	1.2	
		–	–	6.1		2.7	
		–	–	5.5		3.0 to 3.6	

SYMBOL	PARAMETER		T_{amb} (°C)			UNIT	TEST CONDITIONS	
			−40 to +85				V_{CC} (V)	WAVEFORMS
			MIN.	TYP.	MAX.			
t_w	LE pulse width, LE_{AB} or LE_{BA} HIGH		–	–	–	ns	1.2	Fig.7
			2.5	–	–		2.7 to 3.6	
	LE pulse width, CP_{AB} or CP_{BA} HIGH or LOW		–	–	–		1.2	
			2.5	–	–		2.7 to 3.6	
t_{su}	set–up time, A_n before CP_{AB} ↓		–	–	–	ns	1.2	Fig.9
			3	–	–		2.7 to 3.6	
	set–up time, B_n before CP_{AB} ↓		–	–	–		1.2	
			3	–	–		2.7 to 3.6	
	set–up time, A_n before LE_{AB} ↓ or B_n before LE_{AB} ↓	CP high	–	–	–		1.2	
			1.5	–	–		2.7 to 3.6	
		CP low	–	–	–		1.2	
			1.5	–	–		2.7 to 3.6	
t_h	hold time, A_n after CP_{AB} ↓ or B_n before CP_{AB} ↓		–	–	–	ns	1.2	
			0	–	–		2.7 to 3.6	
	hold time, A_n after LE_{AB} ↓ or B_n before LE_{BA} ↓		–	–	–		1.2	
			1	–	–		2.7 to 3.6	

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

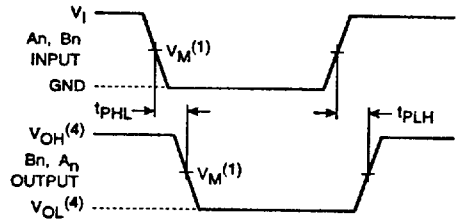


Fig.6 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays.

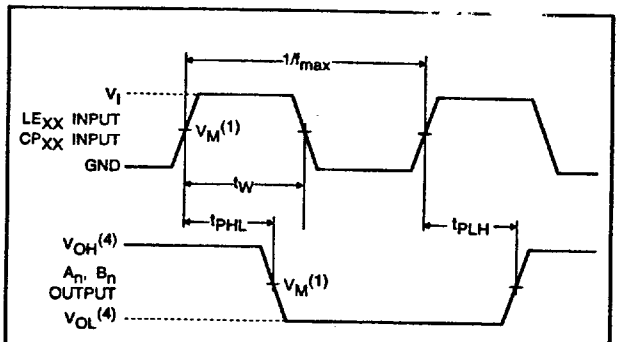


Fig.7 Waveforms showing the latch enable input (E_{AB}, LE_{BA}) and clock pulse input (CP_{AB}, CP_{BA}) to output propagation delays and their pulse width.

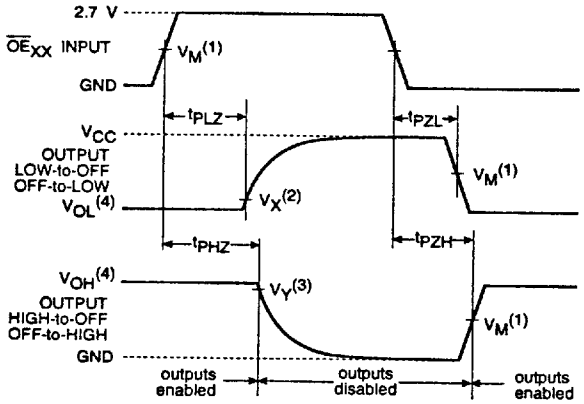


Fig.8 Waveforms showing the 3-state enable and disable times

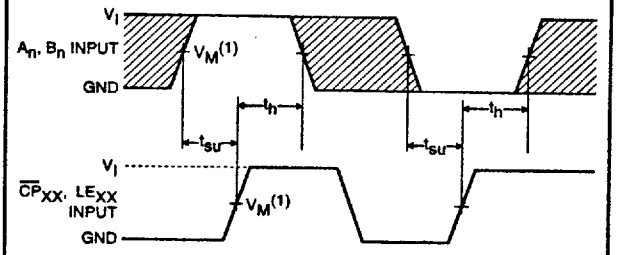
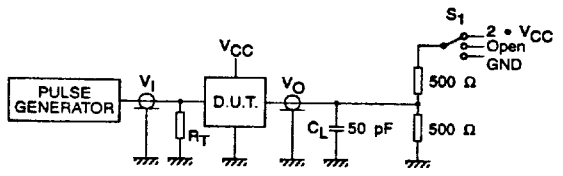


Fig.9 Waveforms showing the data set-up and hold times for the A_n and B_n inputs to the LE_{AB}, LE_{BA}, CP_{AB} and CP_{AB} inputs.
The shaded areas indicate when the input is permitted to change for predictable output performance.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.10 Load circuitry for switching times.

Notes:

(1) V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 · V_{CC} at V_{CC} < 2.7 V

(2) $V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V
$V_X = V_{OL}$ + 0.1 · V_{CC} at V_{CC} < 2.7 V

(3) $V_Y = V_{OH}$ − 0.3 V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH}$ − 0.1 · V_{CC} at V_{CC} < 2.7 V

(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.