REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make change to 1.2.4. In accordance with N.O.R. 5962-R086-96.	96-03-20	M.A. FRYE
B	Add device class N. Add case outline Y. Make editorial changes throughout. Redrawn.	96-08-16	R. MONNIN

REV																				
SHEET																				
REV	B	B	B	B	B	B	B	B	B	B	B	B	B							
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27							

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
RICK OFFICER

CHECKED BY
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APPROVED BY
MICHAEL FRYE

DRAWING APPROVAL DATE
96-01-12

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, LINEAR, 175 MHZ, 64-BIT, VIDEO INTERFACE PALETTE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-96758

SHEET 1 OF 27

DESC FORM 193
JUL 94

5962-E497-96

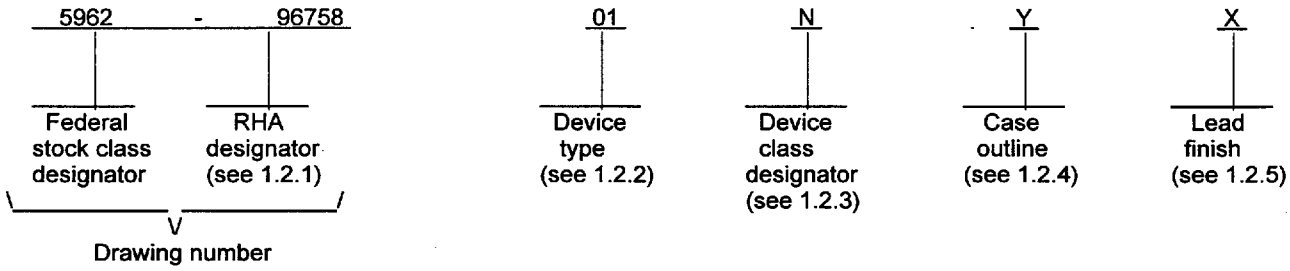
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0024100 958

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device classes Q and M), space application (device class V) and nontraditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN. For device class N, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes N, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TVP3026	175 MHz, 64-bit, video interface palette

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
N	Certification and qualification to MIL-PRF-38535 with a non traditional performance environment 1/
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CQCC2-F164	164	Quad ceramic flat pack with non-conductive tie bar
Y	See figure 1	160	Plastic quad flat pack

1/ Any device outside the traditional performance environment; e.g., an operating temperature range of -55°C to +125°C and which requires hermetic packaging.

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{DD})	+7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{DD} + 0.5 V dc 4/
Analog output short-circuit duration to any power supply or common ground	Unlimited
Storage temperature range (T_{STG})	-65°C to +150°C
Junction temperature (T_J)	+175°C
Case temperature for 10 seconds (HFG package)	+260°C
Lead temperature (1.6 mm (1/16 inch) from case for 10 seconds)	+260°C
Thermal resistance, junction to case (Θ_{JC}):	
Case outline X	0.84°C/W (heat slug)
Case outline Y	10.3°C/W
Thermal resistance, junction to ambient (Θ_{JA}):	
Case outline X	36°C/W
Case outline Y	41.4°C/W

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (AV_{DD}, DV_{DD})	+4.75 V dc to +5.25 V dc
Reference voltage,(V_{REF})	+1.1 V dc to +1.3 V dc
High level input voltage range (V_{IH})	+2.4 V dc to VDD + 0.5 V dc
Maximum low level input voltage (V_{IL})	+0.8 V
Ambient operating free-air temperature (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified V_{DD} range and ambient temperature range of -55°C to +125°C. Unused inputs must be held high or low.
4/ The input negative voltage rating may be exceeded provided that the input clamp current rating is observed.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Logic diagram(s). The logic diagram(s) shall be as specified on figure 4.

3.2.5 Switching waveform(s). The switching waveform(s) shall be as specified on figure 5.

3.2.6 Clock diagram. The clock diagram shall be as specified on figure 6.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. For class N devices only, the date code format may be modified as a traceable date code in lieu of the inspection lot date code for case outline Y.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes N, Q, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 110 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

TABLE I. Electrical performance characteristics.

Test and 1/ MIL-STD-883 test method	Symbol	Test conditions 2/ $-55°C \le T_A \le +125°C$ $+4.75\ V \le V_{DD} \le +5.25\ V$ unless otherwise specified		V_{CC}	Group A subgroups 3/	Limits		Unit
						Min	Max	
High level output voltage 3006	V_{OH}	For all inputs affecting output under test, I_{OH} = -800 µA		4.75 V to 5.25 V	1,2,3	2.4		V
Low level output voltage 3007	V_{OL}	For all inputs affecting output under test	D(7-0),GI/O(4-0),VCLK, RCLK,$\overline{SENSE}$, PCLKOUT, MCLK, I_{OL} = 3.2 mA	4.75 V to 5.25 V	1,2,3		0.4	V
			HSYNCOUT,VSYNCOUT I_{OL} = 15 mA				0.4	
			SCLK, I_{OL} = 18 mA				0.5	
Input current high 3010	I_{IH}	For input under test	TTL inputs, V_{IN} = 2.4 V	4.75 V to 5.25 V	1,2,3		10	µA
			ECL inputs, V_{IN} = 4.0 V				10	
Input current low 3009	I_{IL}	For input under test	TTL inputs, V_{IN} = 0.8 V	4.75 V to 5.25 V	1,2,3		-10	µA
			ECL inputs, V_{IN} = 0.4 V				-10	
Supply current	I_{DD}	Psuedo		4.75 V to 5.25 V	1,2,3		1.0	A
		True color					1.0	
		Direct					1.0	
High impedance-state output current 3021	I_{OZ}			4.75 V to 5.25 V	1,2,3		25	µA
Differential input voltage	V_{ID}	ECL inputs		4.75 V to 5.25 V	1,2,3	0.6	6.0	V
Common-mode input voltage	V_{IC}	ECL inputs		4.75 V to 5.25 V	1,2,3	2.85	V_{DD} - 0.5	V
End-point linearity error (each DAC)	E_L	8/$\overline{6}$ high		4.75 V to 5.25 V	1,2,3		1	LSB
		8/$\overline{6}$ low					0.25	
Differential linearity error (each DAC)	E_D	8/$\overline{6}$ high		4.75 V to 5.25 V	1,2,3		1	LSB
		8/$\overline{6}$ low					0.25	
Gray scale error	GSE			4.75 V to 5.25 V	1,2,3		5	%

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and 1/ MIL-STD-883 test method	Symbol	Test conditions 2/ $-55°C \le T_A \le +125°C$ $+4.75\ V \le V_{DD} \le +5.25\ V$ unless otherwise specified	V_{DD}	Group A subgroups 3/	Limits		Unit
					Min	Max	
Output current 4/	I_{OUT}	White level relative to blank	4.75 V to 5.25 V	1,2,3	17.69	20.4	mA
		White level relative to black (7.5 IRE only)			16.74	18.5	mA
		Black level relative to blank (7.5 IRE only)			0.95	1.9	mA
		Blank level on IOR, IOB			-50	50	µA
		Blank level on IOG (with SYNC enabled)			6.29	8.96	mA
		Sync level on IOG (with SYNC enabled)			-50	50	µA
DAC-to-DAC matching	DDM		4.75 V to 5.25 V	1,2,3		5	%
Output compliance voltage	V_{OC}		4.75 V to 5.25 V	1,2,3	0.4	1.2	V
Voltage reference output voltage	V_{REFO}		4.75 V to 5.25 V	1,2,3	1.1	3.0	V
Input capacitance	C_{IN}	See 4.4.1c, TTL inputs f = 1 MHz, V_{IN} = 2.4 V	4.75 V to 5.25 V	4		4.0	pF
		See 4.4.1c, ECL inputs f = 1 MHz, V_{IN} = 4 V				4.0	
Output capacitance	C_{OUT}	See 4.4.1c, f = 1 MHz, I_{OUT} = 0 mA	4.75 V to 5.25 V	4		13.0	pF
Functional test		See 4.4.1b	4.75 V to 5.25 V	7,8			
DOTCLK frequency	f_{DC}	5/	4.75 V to 5.25 V	9,10,11		175	MHz
Pixel clock PLL frequency	f_{PC}	Internal frequency 5/	4.75 V to 5.25 V	9,10,11		175	MHz
		PCLKOUT frequency 5/				110	
MCLK PLL frequency	f_M	5/	4.75 V to 5.25 V	9,10,11		100	MHz
VCO frequency, pixel clock PLL, MCLK PLL, and loop clock PLL	f_{VCO}	5/	4.75 V to 5.25 V	9,10,11	110	220	MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and 1/ MIL-STD-883 test method	Symbol	Test conditions 2/ $-55°C \le T_A \le +125°C$ $+4.75\ V \le V_{DD} \le +5.25\ V$ unless otherwise specified	V_{DD}	Group A subgroups 3/	Limits		Unit
					Min	Max	
CLK0 frequency for VGA mode 2	f_{VGA}	5/	4.75 V to 5.25 V	9,10,11		85	MHz
Clock cycle time	t_{cyc}	TTL 5/	4.75 V to 5.25 V	9,10,11	7.1		ns
		ECL 5/			5.7		
Delay time, RCLK to LCLK	t_{d4}	5/ 6/	4.75 V to 5.25 V	9,10,11		0.5	RCLK periods
Hold time, RS(3-0) valid before RD or WR↓	t_{su1}	5/	4.75 V to 5.25 V	9,10,11	10		ns
Hold time, RS(3-0) valid after RD or WR↓	t_{h1}	5/	4.75 V and 5.25 V	9,10,11	10		ns
Setup time, D(7-0) valid before WR↑	t_{su2}	5/	4.75 V and 5.25 V	9,10,11	35		ns
Hold time, D(7-0) valid after WR↑	t_{h2}	5/	4.75 V and 5.25 V	9,10,11	0		ns
Setup time, VGA(7-0) and VGAHS, VGAVS, and VGABL valid before CLK0↑	t_{su3}	5/	4.75 V and 5.25 V	9,10,11	5		ns
Hold time, VGA(7-0) and VGAHS, VGAVS, and VGABL valid After CLK0↑	t_{h3}	5/	4.75 V and 5.25 V	9,10,11	5		ns
Setup time, P(63-0), VGA(7-0), and PSEL valid before LCLK↑	t_{su4}	5/	4.75 V and 5.25 V	9,10,11	5		ns
Hold time, P(63-0), VGA(7-0), and PSEL valid after LCLK↑	t_{h4}	5/	4.75 V and 5.25 V	9,10,11	2		ns
Setup time, $\overline{SYSHS}$, $\overline{SYSVS}$, and OVS valid before LCLK↑	t_{su5}	5/	4.75 V and 5.25 V	9,10,11	5		ns
Hold time, $\overline{SYSHS}$, $\overline{SYSVS}$, and OVS valid after LCLK↑	t_{h5}	5/	4.75 V and 5.25 V	9,10,11	2		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and 1/ MIL-STD-883 test method	Symbol	Test conditions 2/ $-55°C \le T_A \le +125°C$ $+4.75\ V \le V_{DD} \le +5.25\ V$ unless otherwise specified	V_{DD}	Group A subgroups 3/	Limits		Unit
					Min	Max	
Setup time, $\overline{SYSBL}$ valid before LCLK↑	t_{su6}	5/	4.75 V and 5.25 V	9,10,11	5		ns
Hold time, $\overline{SYSBL}$ valid after LCLK↑	t_{h6}	5/	4.75 V and 5.25 V	9,10,11	2		ns
Pulse duration, $\overline{RD}$ or $\overline{WR}$ low	t_{w1}	5/	4.75 V and 5.25 V	9,10,11	50		ns
Pulse duration, $\overline{RD}$ or $\overline{WR}$ high	t_{w2}	5/	4.75 V and 5.25 V	9,10,11	30		ns
Pulse duration, clock high	t_{w3}	TTL 5/	4.75 V and 5.25 V	9,10,11	3		ns
		ECL 5/			2.5		
Pulse duration, clock low	t_{w4}	TTL 5/	4.75 V and 5.25 V	9,10,11	3		ns
		ECL 5/			2.5		
SCLK/RCLK 7/ frequency	f_{SR}		4.75 V and 5.25 V	9,10,11		85	MHz
VCLK frequency 7/	f_{VC}		4.75 V and 5.25 V	9,10,11		85	MHz
Enable time, $\overline{RD}$ low to D(7-0) valid	t_{en1}	See figure 5	4.75 V and 5.25 V	9,10,11		40	ns
Disable time, $\overline{RD}$ high to D(7-0) disabled	t_{dis1}	See figure 5	4.75 V and 5.25 V	9,10,11		17	ns
Valid time, D(7-0) valid after $\overline{RD}$ high	t_{v1}	See figure 5	4.75 V and 5.25 V	9,10,11	5		ns
Delay time, $\overline{RD}$ low to D(7-0) starting to turn on	t_{d1}	See figure 5	4.75 V and 5.25 V	9,10,11	5		ns
Delay time, SCLK high/low to RCLK high/low	t_{d3}	See figure 5 8/ 9/ 10/	4.75 V and 5.25 V	9,10,11	1	6	ns
Analog output skew	AOS		4.75 V and 5.25 V	9,10,11	0	2	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ For tests not listed in the referenced MIL-STD-883 (e.g. I_{DD}), utilize the general test procedure of MIL-STD-883 under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for the I_{DD} test, where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter. For input terminals not designated, V_{IN} = GND or $V_{IN} \geq 3.0$ V.

3/ For device class N only, all subgroup 3 (-55°C) test limits are guaranteed but not tested.

4/ Test conditions for RS343-A video signals (unless otherwise specified): recommended using external voltage reference V_{REF} = 1.235 V, R_{SET} = 523 Ω. When using the internal voltage reference, R_{SET} may need to be adjusted in order to meet these limits.

5/ Unless otherwise specified, TTL input signals are 0 V to 3 V with less than 3 ns rise/fall time between the 10% and 90% levels ECL input signals are V_{DD}-1.8 V to V_{DD}-0.8 V with less than 2 ns rise/fall time between the 20% and 80% levels. For input and output signals, timing reference points are at the 10% and 90% signal levels. Analog output loads are less than 10 pF. D(0-7) output loads are less than 50 pF. Unless otherwise specified, all other output loads are less than 50 pF. See figures 5 and 6.

6/ This parameter only applies when SCLK is used as the VRAM shift clock. When SCLK is not used, the delay may be as much as is required by system logic (assuming the loop clock PLL is used to compensate for the system delay).

7/ SCLK can drive an output capacitive load up to 60 pF. The worst-case transition time between the 10% and 90% levels is less than 4 ns (typical 3 ns). RCLK and VCLK can drive output capacitive loads up to 15 pF, with worst-case transition times between 10% and 90% levels less than 4 ns (typical 3 ns). See figure 6.

8/ The SCLK delay time to RCLK depends on the load that the signals drive. This parameter is measured with an VCLK = RCLK load of 15 pF and SCLK load of 60 pF.

9/ In SCLK mode, RCLK is delayed from SCLK in such a way that when RCLK is connected to LCLK.

10/ This parameter applies when SCLK is used.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

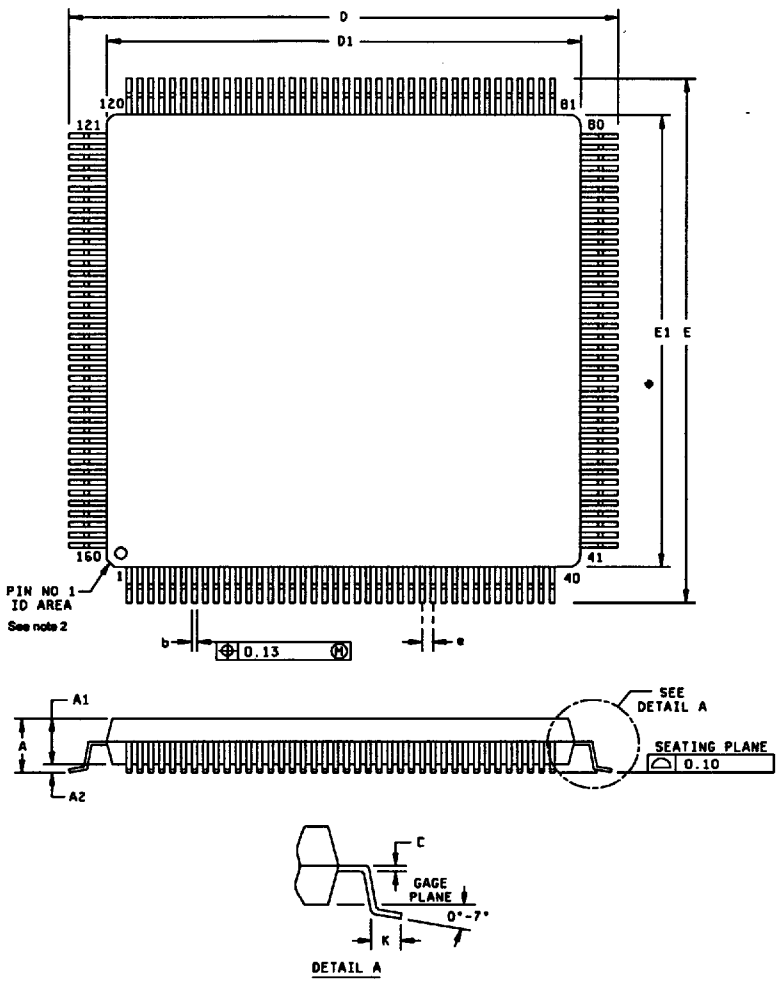


FIGURE 1. Case outline Y.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-96758
		REVISION LEVEL B	SHEET 11

Symbol	Dimensions		Notes
	Millimeters		
	Min	Max	
A	---	4.07	
A1	3.17	3.67	
A2	0.25	---	
b	0.30	---	
c	0.16	---	
D	30.95	31.45	
D1	27.90	28.10	
E	30.95	31.45	
E1	27.90	28.10	
e	0.65 BSC		
k	0.65	0.95	
N	160		3
Notes	1		

NOTES:

1. Controlling dimension: millimeter.
2. Index area: A notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as a pin one identification mark.
3. N is the maximum number of terminal positions.

FIGURE 1. Case outline Y - Continued.

Device type	01						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	PLLSEL0	42	GND	83	GND	124	MCLK
2	DV_{DD}	43	RS3	84	GND	125	ODD/EVEN
3	P33	44	$\overline{WR}$	85	GND	126	LCLK
4	P32	45	$\overline{RD}$	86	AV_{DD}	127	RCLK
5	P31	46	DV_{DD}	87	GND	128	VCLK
6	P30	47	GND	88	AV_{DD}	129	SCLK
7	P29	48	D7	89	AV_{DD}	130	P56
8	P28	49	D6	90	VGA0	131	P55
9	P27	50	D5	91	VGA1	132	P54
10	P26	51	D4	92	VGA2	133	P53
11	P25	52	D3	93	VGA3	134	P52
12	P24	53	D2	94	VGA4	135	P51
13	P23	54	D1	95	VGA5	136	P50
14	P22	55	D0	96	VGA6	137	P49
15	P21	56	RS0	97	VGA7	138	P48
16	P20	57	RS1	98	OVS	139	GND
17	GND	58	RS2	99	PSEL	140	DV_{DD}
18	DV_{DD}	59	GI/O0	100	$\overline{8/6}$	141	P47
19	P19	60	GI/O1	101	$\overline{SYSHS}$	142	P46
20	P18	61	GI/O2	102	SYSVS	143	P45
21	NC	62	NC	103	$\overline{NC}$	144	NC
22	P17	63	GI/O3	104	SYSBL	145	P44
23	P16	64	$\overline{GI/O4}$	105	VGAHS	146	PLLGND
24	P15	65	$\overline{RESET}$	106	$\overline{VGAVS}$	147	$PLLV_{DD}$
25	P14	66	$\overline{SENSE}$	107	VGABL	148	PCLKOUT
26	P13	67	DV_{DD}	108	SFLAG	149	NC
27	P12	68	GND	109	CLK0	150	$PLLV_{DD}$
28	P11	69	HSYNCOUT	110	CLK1	151	NC
29	P10	70	VSYNCOUT	111	CLK2	152	NC
30	P9	71	GND	112	$\overline{CLK2}$	153	P43
31	P8	72	IOR	113	P63	154	P42
32	P7	73	GND	114	P62	155	P41
33	P6	74	IOG	115	P61	156	P40
34	P5	75	GND	116	P60	157	P39
35	P4	76	IOB	117	P59	158	P38
36	P3	77	GND	118	P58	159	P37
37	P2	78	FS ADJUST	119	P57	160	P36
38	P1	79	COMP1	120	DV_{DD}	161	P35
39	P0	80	REF	121	GND	162	P34
40	VD_{DD}	81	COMP2	122	XTAL1	163	GND
41	VD_{DD}	82	AV_{DD}	123	XTAL2	164	PLLSEL1

FIGURE 2. Terminal connection.

Device type	01						
Case outline	Y						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	PLLSEL0	42	RS3	83	GND	124	RCLK
2	DV_{DD}	43	$\overline{WR}$	84	AV_{DD}	125	VCLK
3	P33	44	$\overline{RD}$	85	GND	126	SCLK
4	P32	45	DV_{DD}	86	AV_{DD}	127	P56
5	P31	46	GND	87	AV_{DD}	128	P55
6	P30	47	D7	88	VGA0	129	P54
7	P29	48	D6	89	VGA1	130	P53
8	P28	49	D5	90	VGA2	131	P52
9	P27	50	D4	91	VGA3	132	P51
10	P26	51	D3	92	VGA4	133	P50
11	P25	52	D2	93	VGA5	134	P49
12	P24	53	D1	94	VGA6	135	P48
13	P23	54	D0	95	VGA7	136	GND
14	P22	55	RS0	96	OVS	137	DV_{DD}
15	P21	56	RS1	97	PSEL	138	P47
16	P20	57	RS2	98	$\overline{8/6}$	139	P46
17	GND	58	GI/O0	99	$\overline{SYSHS}$	140	P45
18	DV_{DD}	59	GI/O1	100	$\overline{SYSVS}$	141	P44
19	P19	60	GI/O2	101	SYSBL	142	PLLGND
20	P18	61	GI/O3	102	VGAHS	143	$PLLV_{DD}$
21	P17	62	$\overline{GI/O4}$	103	$\overline{VGAVS}$	144	PCLKOUT
22	P16	63	$\overline{RESET}$	104	VGABL	145	NC
23	P15	64	SENSE	105	SFLAG	146	$PLLV_{DD}$
24	P14	65	DV_{DD}	106	CLK0	147	NC
25	P13	66	GND	107	CLK1	148	NC
26	P12	67	HSYNCOUT	108	$\overline{CLK2}$	149	P43
27	P11	68	VSYNCOUT	109	$\overline{CLK2}$	150	P42
28	P10	69	GND	110	P63	151	P41
29	P9	70	IOR	111	P62	152	P40
30	P8	71	GND	112	P61	153	P39
31	P7	72	IOG	113	P60	154	P38
32	P6	73	GND	114	P59	155	P37
33	P5	74	IOB	115	P58	156	P36
34	P4	75	GND	116	P57	157	P35
35	P3	76	FS ADJUST	117	DV_{DD}	158	P34
36	P2	77	COMP1	118	GND	159	GND
37	P1	78	REF	119	XTAL1	160	PLLSEL1
38	P0	79	COMP2	120	XTAL2		
39	VD_{DD}	80	AV_{DD}	121	$\overline{MCLK}$		
40	VD_{DD}	81	GND	122	ODD/EVEN		
41	GND	82	GND	123	LCLK		

FIGURE 2. Terminal connection - Continued.

Direct register map

RS 3	RS 2	RS 1	RS 0	Register addressed by MPU	R/W	Default (Hex)
0	0	0	0	Palette/cursor RAM write address/ index register	R/W	XX
0	0	0	1	Palette RAM data	R/W	XX
0	0	1	0	Pixel read-mask	R/W	FF
0	0	1	1	Palette/cursor RAM read address	R/W	XX
0	1	0	0	Cursor/overscan color write address	R/W	XX
0	1	0	1	Cursor/overscan color data	R/W	XX
0	1	1	0	Reserved		
0	1	1	1	Cursor/overscan color read address	R/W	XX
1	0	0	0	Reserved		
1	0	0	1	Direct cursor control	R/W	00
1	0	1	0	Indexes data	R/W	XX
1	0	1	1	Cursor RAM data	R/W	XX
1	1	0	0	Cursor-position X LSB	R/W	XX
1	1	0	1	Cursor-position X MSB	R/W	XX
1	1	1	0	Cursor-position Y LSB	R/W	XX
1	1	1	1	Cursor-position Y MSB	R/W	XX

FIGURE 3. Truth table.

Indirect register map (extended registers)

Index	R/W	Default	Register addressed by index register
0x00			Reserved
0x01	R	0x00 1/	Silicon revision
0x02-0x05			Reserved
0x06	R/W	0x00	Indirect cursor control
0x07-0x0E			Reserved
0x0F	R/W	0x06	Latch control
0x10-0x17			Reserved
0x18	R/W	0x80	True color control
0x19	R/W	0x98	Multiplex control
0x1A	R/W	0x07	Clock selection
0x1B			Reserved
0x1C	R/W	0x00	Palette page
0x1D	R/W	0x00	General control
0x1E	R/W	0x00	Miscellaneous control
0x1F-0x29			Reserved
0x2A	R/W	XX	General-purpose I/O control
0x2B	R/W	XX	General-purpose I/O data
0x2C	R/W	XX	PLL address
0x2D	R/W	XX	Pixel clock PLL data
0x2E	R/W	XX	Memory clock PLL data
0x2F	R/W	XX	Loop clock PLL data
0x30	R/W	XX	Color-key overlay low
0x31	R/W	XX	Color-key overlay high
0x32	R/W	XX	Color-key red low
0x33	R/W	XX	Color-key red high
0x34	R/W	XX	Color-key green low
0x35	R/W	XX	Color-key green high
0x36	R/W	XX	Color-key blue low
0x37	R/W	XX	Color-key blue high

FIGURE 3. Truth table - Continued.

Indirect register map (extended registers) - Continued

Index	R/W	Default	Register addressed by index register
0x38	R/W	0x00	Color-key control
0x39	R/W	0x18	MCLK/Loop clock control
0x3A	R/W	0x00	Sense test
0x3B	R	XX	Test mode data
0x3C	R	XX	CRC remainder LSB
0x3D	R	XX	CRC remainder MSB
0x3E	W	XX	CRC bit select
0x3F	R	0x26	ID
0xFF	W	XX	Software reset

FIGURE 3. Truth table - Continued.

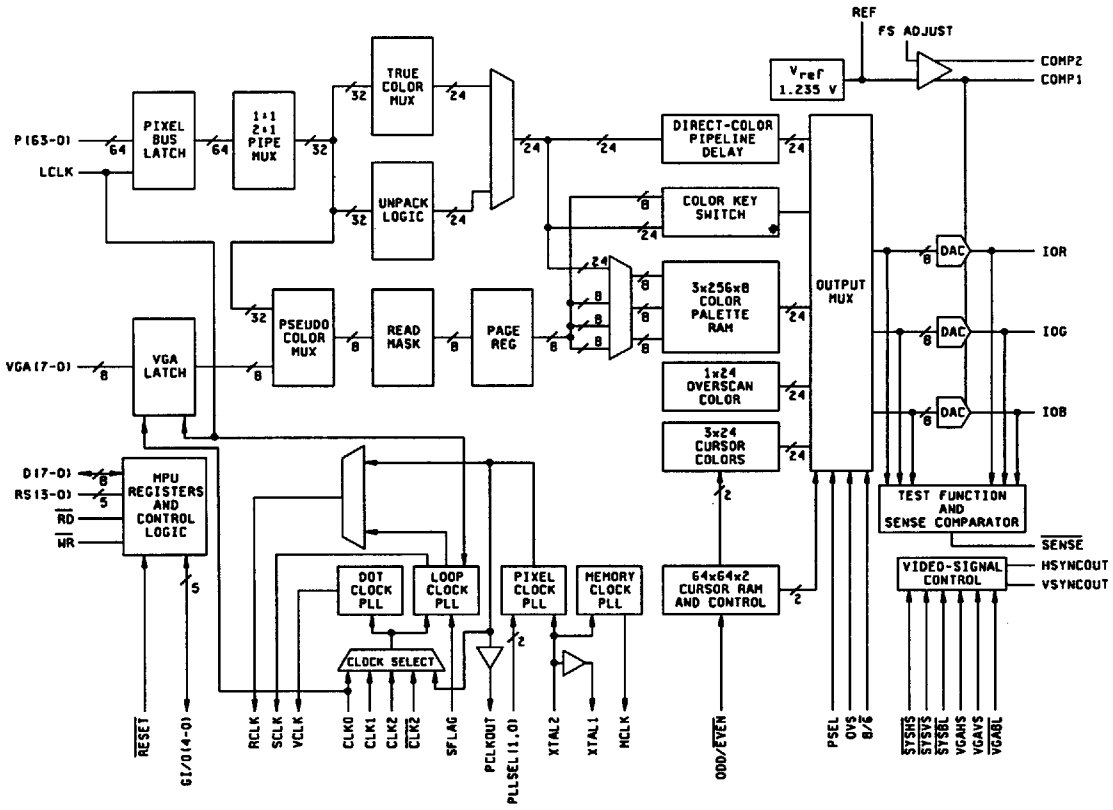


FIGURE 4. Logic diagram.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-96758
		REVISION LEVEL B	SHEET 18

DESC FORM 193A
JUL 94

9004708 0024117 151

MPU interface

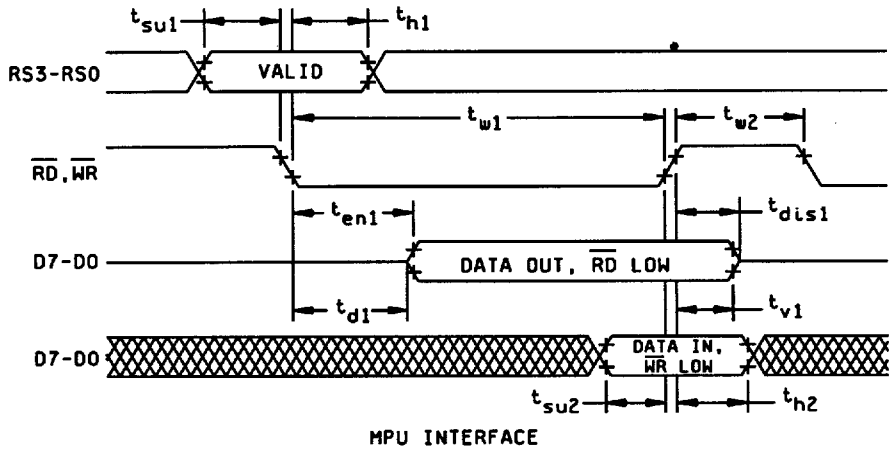
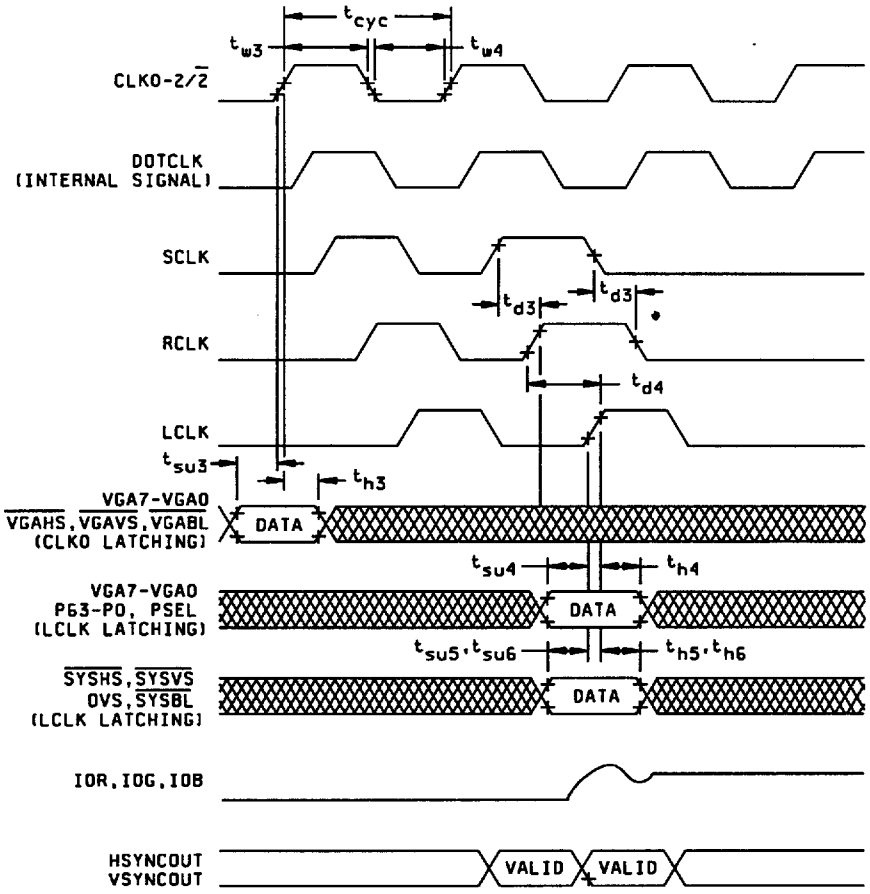


FIGURE 5. Switching waveforms.

Video input/output



VIDEO INPUT/OUTPUT

FIGURE 5. Switching waveforms - Continued.

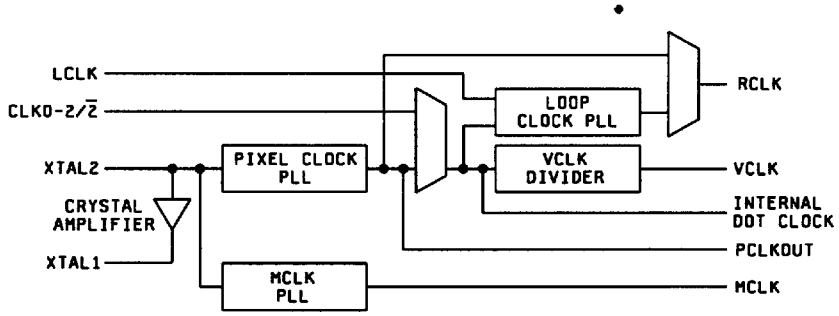


FIGURE 6. Clocking diagram.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 3 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3, herein. For device classes N, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} and C_{OUT} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and GND at a frequency of 1 MHz. This test may be performed at 10 MHz and guaranteed, if not tested, at 1 MHz. The DC bias for the pin under test (V_{BIAS}) = 2.5 V or 3.0 V. For C_{IN} and C_{OUT}, test all applicable pins on five devices with zero failures. For C_{IN} and C_{OUT}, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I, herein. The device manufacturer shall set a function group limit for the C_{IN} and C_{OUT} tests. The device manufacturer may then test one device functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and test conditions specified in table I, herein. The device manufacturers shall submit to DSCC-VA the device functions listed in each functional group and the test results for each device tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes N, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class M	Device class N	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---	1
Final electrical parameters (see 4.2)	1, 2, 3, 1/ 7, 8, 9, 10, 11	1,2,3 1/ 7,8,9,10,11	1, 2, 3, 1/ 7, 8, 9, 10, 11	1, 2, 3, 2/ 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1,2,3,4,7,8, 9,10,11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1	---*	1	1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1	---	1	1
Group E end-point electrical parameters (see 4.4)	1, 7, 9	---	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions.

Terminal symbol	I/O	Description
AV_{DD}		Analog power. All AV_{DD} terminals must be connected. A separate cutout in the DV_{DD} plane should be made for AV_{DD}. The DV_{DD} and AV_{DD} planes should be connected only at a single point through a ferrite bead close to where power enters the board.
CLK0	I	Dot clock 0 TTL input. CLK0 can be selected to drive the dot clock frequencies up to 140 MHz. When using the VGA port, the maximum frequency is 85 MHz. CLK0 can be selected as the latch clock for VGA and video controls. (power up default)
CLK1	I	Dot clock 1 TTL input. CLK1 can be selected to drive the dot clock at frequencies up to 140 MHz.
CLK2, $\overline{CLK2}$	I	Dual-mode dot clock input. These inputs are ECL-compatible inputs. Alternately, CLK2 and $\overline{CLK2}$ may be used as individual TTL clock inputs. Programming the clock selection register selects the chosen configuration. These inputs may be selected as the dot clock up to the device limit while in the ECL mode or up to 140 MHz in the TTL mode.
COMP1, COMP2	I	Compensation. COMP1 and COMP2 provide compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor is required between COMP1 and COMP2. This capacitor must be as close to the device as possible to avoid noise pickup.
DV_{DD}		Digital power. All DV_{DD} terminals must be connected to the digital power plane with sufficient decoupling capacitors near the device.
D7 - D0	I/O	MPU interface data bus. These terminals are used to transfer data in and out of the register map, palette RAM, and cursor RAM.
FS ADJUST	I	Full-scale adjustment. A resistor connected between this terminal and ground controls the full-scale range of the DAC's.
GND		Ground. All GND terminals must be connected. A common ground plane should be used.
HSYNCOUT, VSYNCOUT	O	Horizontal and vertical sync outputs. These outputs are pipeline delayed versions of the selected sync inputs. Output polarity inversion may be independently selected using general control register bits GCR(1,0).
IOR, IOG, IOB	O	Analog current outputs. These outputs can drive a 37.5 Ω load directly (doubly terminated 75 Ω line), thus eliminating the requirement for any external buffering

Terminal symbol	I/O	Description
LCLK	I	Latch clock input. LCLK is used to latch pixel-bus-input data and sytem video controls. VGA data may also be latched with LCLK if so selected. LCLK may be a deleayed version of RCLK provided that linear phase changes in RCLK cause corresponding linear phase changes in LCLK.
MCLK	O	Memory clock output. MCLK is the output of an independently programmable PLL frequency synthesizer. The frequency range is 14 - 100 MHz. The dot clock may be output on this terminal while the MCLK frquency is reprogrammed.
PCLKOUT	O	Pixel clock PLL output. PCLKOUT is a buffered version of the pixel clock PLL output and is mainly for test purposes. This output is independent of the dot clock source selected by the clock selection register.
PLLGND		Ground for PLL supplies. Decoupling capacitors should be connected between $PLLV_{DD}$ and PLLGND. PLLGND should be connected to the system ground through a ferrite bead.
$PLLV_{DD}$		PLL power supply. $PLLV_{DD}$ must be a well regulated 5 V power supply voltage. Decoupling capacitors should be connected between $PLLV_{DD}$ and PLLGND. Terminal 143 supplies power to the pixel clock PLL. Terminal 146 supplies power to the MCLK PLL and the loop clock PLL.
OVS	I	Overscan input. OVS is used to control the display of custom screen borders. If OVS is not used, it should be connected to GND.
ODD/$\overline{\text{EVEN}}$	I	Odd or even field disply. ODD/$\overline{\text{EVEN}}$ indicates odd or even field during interlaced display for cursor operation.
PLLSEL0, PLLSEL1	I	Pixel clock PLL frequency selection. Selects among two fixed frequencies and the programmed frequency of the pixel clock PLL.
PSEL	I	Port select. PSEL provides the capability of switching between direct color and true color or overlay. Multiple true color or overlay windows may be displayed using the PSEL control. Since PSEL is sampled with LCLK, the granularity for switching depends on the number of pixels loaded per LCLK. If PSEL is not used, it should be connected to GND.
P63-P0	I	Pixel input port. The port can be used in various modes. Unused terminals should not be allowed to float.
RCLK	O	Reference Clock output.
REF	I/O	Voltage reference for DACs. An internal voltage reference of nominally 1.235 V is provided, which requires an external 0.1 µF ceramic capacitor between REF and analog GND. However, the internal reference voltagecan be overdriven by an externally supplied reference voltage.
$\overline{\text{RESET}}$	I	Master reset. All the registers assume their default state after reset. The default state is VGA mode 2 (CLK0 latching of VGA data and video controls).
$\overline{\text{RD}}$	I	Read strobe input. A logic 0 on this terminal initiates a read from the register map. Read transfer data is enabled onto the D(7 - 0) bus when $\overline{\text{RD}}$ is low.

Terminal symbol	I/O	Description
RS3-RS0	I	Register select inputs. These terminals specify the location in the direct register map that is to be acessed.
SCLK	O	Shift clock output. SCLK is a gated version of the loop clock PLL output and is gated off during blank. SCLK may be used to drive the VRAM shift clock directly. This is intended for designs in which the graphics controller does not supply the VRAM shift clock.
$\overline{\text{SENSE}}$	O	Test mode DAC comparator output signal. This terminal is low if one or more of the DAC output analog levels is above the internal comparator reference of 350 mV ±50 mV.
SFLAG	I	Split shift register transfer flag. A high pulse on this terminal during blank is passed directly to the SCLK terminal. This operation is available to meet the special serial clocking requirements of some VRAM devices. If SFLAG is not used, SFLAG should be connected to GND.
$\overline{\text{SYSBL}}$	I	System blank input. $\overline{\text{SYSBL}}$ is active low. This should be selected for all modes other than VGA mode 2. This signal is pipeline delayed before being passed to the DACs.
$\overline{\text{SYSHS}}$, $\overline{\text{SYSVS}}$	I	System horizontal and vertical sync inputs. These signals should be selected for all modes other than VGA mode 2. These siganals are pipelined delayed and each may be inverted before being passed to the HSYNCOUT and VSYNCOUT terminals. General control register bits GCR(1,0) control the parity inversion. If used to generate the sync level on the green current, $\overline{\text{SYSHS}}$ and $\overline{\text{SYSVS}}$ must be active low at the input to the device.
VCLK	O	Progammable auxiliary clock output. VCLK is derived from the internal dot clock using a programmable divide ratio and does not utilize the loop clock PLL for synchronization. Since pixel data and video controls are always referenced to RCLK and LCLK (or CLK0), use of VCLK for the frame buffer interface or video timing is not recommended.
$\overline{\text{VGABL}}$	I	VGA blank input. $\overline{\text{VGABL}}$ is active low. This should be selected when in VGA mode 2 (CLK0 latching of VGA data and video controls). $\overline{\text{VGABL}}$ is pipeline delayed before being passed to the DACs.
VGAHS, VGAVS	I	VGA horizontal and vertical sync inputs. These signals should be used when in VGA mode 2 (CLK0 latching of VGA data and video controls). These signals are pipelined delayed and each may be inverted before being passed to the HSYNCOUT and VSYNCOUT terminals. General control register bits GCR(1,0) control the polarity inversion. If used to generate the sync level on the green current output, VGAHS and VGAVS must be active low at the input to the device.
VGA7 - VGA0	I	VGA port. This bus can be selected at the pixel input bus for VGA modes, but it does not allow for any mutiplexing.
$\overline{\text{WR}}$	I	Write strobe input. A logic 0 on this terminal initiates a write to the register map. Write transfer data is latched from the D(7-0) bus with the rising edge of $\overline{\text{WR}}$.
XTAL1, XTAL2	I/O	Connection for quartz crystal resonator as a reference for the frequency synthesis PLLs. XTA2 may be used as a TTL reference clock input, in which case XTAL1 is left unconnected.
8/$\overline{6}$	I	DC resolution selection. This terminal is used to select the data bus width (8 or 6 bits) for the DACs and is provided for VGA downward compatibility.

Terminal symbol	I/O	Description
GND		Ground zero voltage potential
I_{DD}		Quiescent supply current
I_{IL}		Input current low
I_{IH}		Input current high
T_A		Ambient temperature
V_{DD}		Positive supply voltage
C_{IN}		Input terminal to ground capacitance
C_{OUT}		Output terminal to ground capacitance
V_{IC}		Negative input clamp voltage

6.6 Sources of supply.

6.6.1 Sources of supply for device classes N, Q, and V. Sources of supply for device classes N, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 96-08-16

Approved sources of supply for SMD 5962-96758 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9675801NYB	01295	TVP3026-175MPCE
5962-9675801QXA	01295	TVP3026-175MHFGB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448

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