



MOTOROLA

Quad OR/NOR Gate

**ELECTRICALLY TESTED PER:
5962-8750301**

The 10H501 is a quad 2-input **OR/NOR** gate with one input from each gate common to pin 12.

This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

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- Propagation Delay, 1.0 ns Typical
- 40 mW Max/Gate (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

FUNCTION	PIN ASSIGNMENTS			BURN-IN (CONDITION C)
	DIL	FLATS	LCC	
VCC1	1	5	2	GND
AOUT	2	6	3	50 Ω to V _{TT}
BOUT	3	7	4	50 Ω to V _{TT}
A _{IN}	4	8	5	50 Ω to V _{TT}
AOUT	5	9	7	50 Ω to V _{TT}
BOUT	6	10	8	50 Ω to V _{TT}
B _{IN}	7	11	9	50 Ω to V _{TT}
VEE	8	12	10	VEE
DOUT	9	13	12	510 Ω to V _{TT}
C _{IN}	10	14	13	510 Ω to V _{TT}
COUT	11	15	14	510 Ω to V _{TT}
Common Input	12	16	15	OPEN
D _{IN}	13	1	17	50 Ω to V _{TT}
COUT	14	2	18	50 Ω to V _{TT}
DOUT	15	3	19	50 Ω to V _{TT}
VCC2	16	4	20	GND

BURN - IN CONDITIONS:

V_{TT} = - 2.0 V MAX/ - 2.2 V MIN

VEE = - 5.7 V MAX/ - 5.2 V MIN

Military 10H501

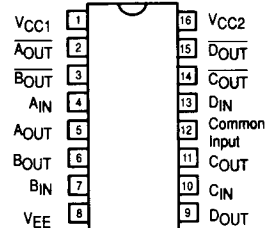


AVAILABLE AS

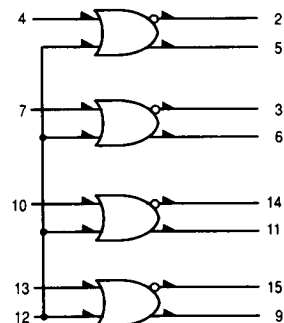
- 1) JAN: N/A
 - 2) SMD: 5962-8750301
 - 3) 883: 10H501/BXAJC
- X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM



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- ## NOTES

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10H501 QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	PS1	PS2	VEE1	VEE2
T _A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94
T _A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94
T _A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 0 V, Output Load = 100 Ω to - 2.0 V									
		Subgroup 1		Subgroup 2		Subgroup 3												
		Min	Max	Min	Max	Min	Max		V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	V _{EE1}	V _{EE2}	V _{CC}	P.U.T.		
V _{OH}	High Output Voltage	- 1.01	- 0.78	- 0.86	- 0.65	- 1.06	- 0.84	V	4, 7, 10 12, 13	4, 7, 10 12, 13			8		1, 16	2, 3, 5, 6, 9, 11, 14, 15		
V _{OL}	Low Output Voltage	- 1.95	- 1.58	- 1.95	- 1.565	- 1.95	- 1.61	V	4, 7, 10 12, 13	4, 7, 10 12, 13			8		1, 16	2, 3, 5, 6, 9, 11, 14, 15		
V _{OHA}	High Output Voltage	- 1.01	- 0.78	- 0.86	- 0.65	- 1.06	- 0.84	V			4, 7, 10 12, 13	4, 7, 10 12, 13	8	8	1, 16	2, 3, 5, 6, 9, 11, 14, 15		
V _{OLA}	Low Output Voltage	- 1.95	- 1.58	- 1.95	- 1.565	- 1.95	- 1.61	V			4, 7, 10 12, 13	4, 7, 10 12, 13	8	8	1, 16	2, 3, 5, 6, 9, 11, 14, 15		
I _{EE}	Power Supply Current	- 26	- 29	- 29		- 29		mA					8		1, 16	8		
I _{IH1}	Input Current High		265		425		425	μA	4, 7, 10, 13				8		1, 16	4, 7, 10, 13		
I _{I2}	Input Current High		535		850		850	μA	12				8		1, 16	12		
I _{IL}	Input Current Low	0.5		0.3		0.5		μA		4, 7, 10 12, 13				8	1, 16	4, 7, 10, 12, 13		

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Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max							VIN
tTLH	Rise Time (common)	0.4	1.65	0.4	1.7	0.4	1.65	ns	4	2, 5	1, 16	8	2	
tTHL	Fall time (common)	0.4	1.65	0.4	1.7	0.4	1.65	ns	7	3	1, 16	8	2, 5	
tPLH	Propagation Delay Low to High (common)	0.5	1.6	0.5	1.8	0.5	1.6	ns	12	5	1, 16	8	2	
tPHL	Propagation Delay High to Low (common)	0.5	1.6	0.5	1.8	0.5	1.6	ns	12	15	1, 16	8	2, 5	
tTLH	Rise Time (others)	0.4	1.6	0.4	1.6	0.4	1.6	ns	4	2, 5	1, 16	8	2	
tTHL	Fall time (others)	0.4	1.6	0.4	1.6	0.4	1.6	ns	7	3	1, 16	8	2, 5	
tPLH	Propagation Delay Low to High (others)	0.3	1.5	0.3	1.7	0.3	1.5	ns	12	5	1, 16	8	2	
tPHL	Propagation Delay High to Low (others)	0.3	1.5	0.3	1.7	0.3	1.5	ns	12	15	1, 16	8	2, 5	