PA19 • PA19A

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FEATURES

- VERY FAST SLEW RATE — 900 V/µs
- POWER MOS TECHNOLOGY — 4A peak rating
- LOW INTERNAL LOSSES — 2V at 2A
- PROTECTED OUTPUT STAGE — Thermal Shutoff
- WIDE SUPPLY RANGE — ±15V TO ±40V

8-PIN TO-3
PACKAGE STYLE CE

APPLICATIONS

- VIDEO DISTRIBUTION AND AMPLIFICATION
- HIGH SPEED DEFLECTION CIRCUITS
- POWER TRANSDUCERS UP TO 5 MHz
- MODULATION OF RF POWER STAGES
- POWER LED OR LASER DIODE EXCITATION

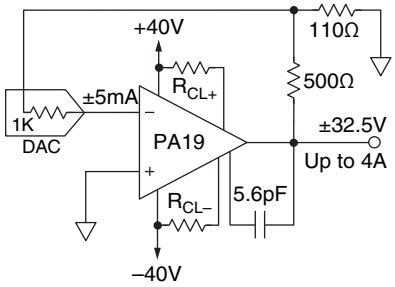
DESCRIPTION

The PA19 is a high voltage, high current operational amplifier optimized to drive a variety of loads from DC through the video frequency range. Excellent input accuracy is achieved with a dual monolithic FET input transistor which is cascoded by two high voltage transistors to provide outstanding common mode characteristics. All internal current and voltage levels are referenced to a zener diode biased on by a current source. As a result, the PA19 exhibits superior DC and AC stability over a wide supply and temperature range.

High speed and freedom from second breakdown is assured by a complementary power MOS output stage. For optimum linearity, especially at low levels, the power MOS transistors are biased in a class A/B mode. Thermal shutoff provides full protection against overheating and limits the heatsink requirements to dissipate the internal power losses under normal operating conditions. A built-in current limit of 0.5A can be increased with the addition of two external resistors. Transient inductive load kickback protection is provided by two internal clamping diodes. External phase compensation allows the user maximum flexibility in obtaining the optimum slew rate and gain bandwidth product at all gain settings. A heatsink of proper rating is recommended.

This hybrid circuit utilizes thick film (cermet) resistors, ceramic capacitors, and silicon semiconductor chips to maximize reliability, minimize size, and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically sealed. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

TYPICAL APPLICATION

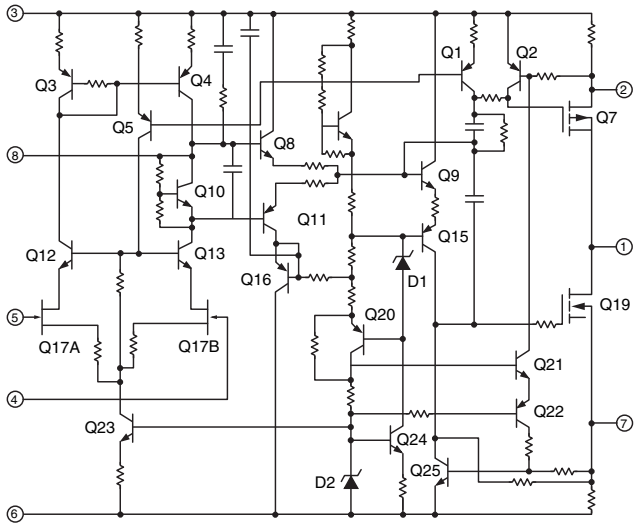


PA19 AS FAST POWER DRIVER

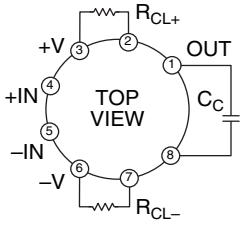
TYPICAL APPLICATION

This fast power driver utilizes the 900V/µs slew rate of the PA19 and provides a unique interface with a current output DAC. By using the DAC's internal 1KΩ feedback resistor, temperature drift errors are minimized, since the temperature drift coefficients of the internal current source and the internal feedback resistor of the DAC are closely matched. Gain of V_{OUT} to I_{IN} is –6.5/mA. The DAC's internal 1K resistor together with the external 500Ω and 110Ω form a "tee network" in the feedback path around the PA19. This effective resistance equals 6.5KΩ . Therefore the entire circuit can be modeled as 6.5KΩ feedback resistor from output to inverting input and a 5mA current source into the inverting input of the PA19. Now we see the familiar current to voltage conversion for a DAC where $V_{OUT} = -I_{IN} \times R_{FEEDBACK}$.

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



PHASE COMPENSATION

GAIN	C_C
1	330pF
10	22pF
100	2.2pF
1000	none

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	80V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal	78W
INPUT VOLTAGE, differential	40V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder — 10 sec	300°C
TEMPERATURE, junction[1]	150°C
TEMPERATURE, storage	–65 to 155°C
OPERATING TEMPERATURE RANGE, case	–55 to 125°C

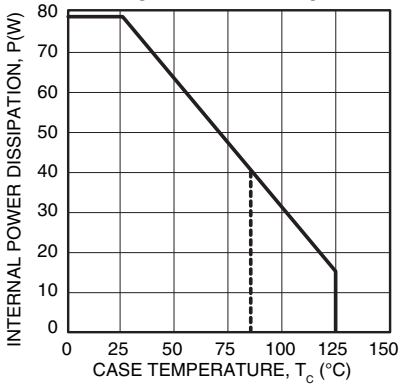
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	PA19 MIN	PA19 TYP	PA19 MAX	PA19A MIN	PA19A TYP	PA19A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±.5	±3		±.25	±.5	mV
OFFSET VOLTAGE, vs. temperature	T_C = 25°C to +85°C		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		10			*		µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C to +85°C		20			*		µV/W
BIAS CURRENT, initial	T_C = 25°C		10	200		5	50	pA
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		5	100		3	25	pA
INPUT IMPEDANCE, DC	T_C = 25°C		10^{11}			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		6			*		pF
COMMON MODE VOLTAGE RANGE[3]	T_C = 25°C to +85°C	$\pm V_S$–15	$\pm V_S$–12		*	*		V
COMMON MODE REJECTION, DC	T_C = 25°C to +85°C, V_{CM} = ±20V	70	104		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = 1KΩ		111			*		dB
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = 15Ω	74	78		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	T_C = 25°C, C_C = 2.2pF		100			*		MHz
POWER BANDWIDTH, A_V = 100	T_C = 25°C, C_C = 2.2pF		3.5			*		MHz
POWER BANDWIDTH, A_V = 1	T_C = 25°C, C_C = 330pF		250			*		kHz
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 4A	$\pm V_S$–5	$\pm V_S$–4		*	*		V
VOLTAGE SWING[3]	T_C = 25°C to +85°C, I_O = 2A	$\pm V_S$–3	$\pm V_S$–2		*	*		V
VOLTAGE SWING[3]	T_C = 25°C to +85°C, I_O = 78mA	$\pm V_S$–1	$\pm V_S$–.5		*	*		V
SETTLING TIME to .1%	T_C = 25°C, 2V step		.3			*		µs
SETTLING TIME to .01%	T_C = 25°C, 2V step		1.2			*		µs
SLEW RATE, A_V = 100	T_C = 25°C, C_C = 2.2pF	600	900		800	*		V/µs
SLEW RATE, A_V = 10	T_C = 25°C, C_C = 22pF		650			*		V/µs
POWER SUPPLY								
VOLTAGE	T_C = 25°C to +85°C	±15	±35	±40	*	*	*	V
CURRENT, quiescent	T_C = 25°C		100	120		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	T_C = 25°C to +85°C, F > 60Hz		1.2	1.3		*	*	°C/W
RESISTANCE, DC, junction to case	T_C = 25°C to +85°C, F < 60Hz		1.6	1.8		*	*	°C/W
RESISTANCE, junction to air	T_C = 25°C to +85°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	*		*	°C

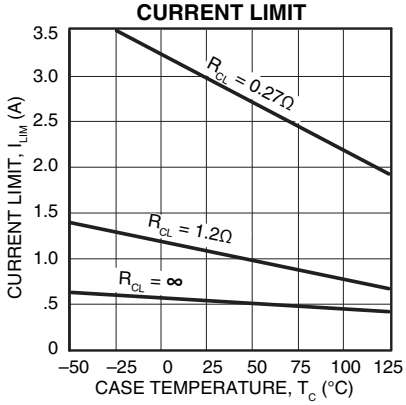
NOTES: * The specification of PA19A is identical to the specification for PA19 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

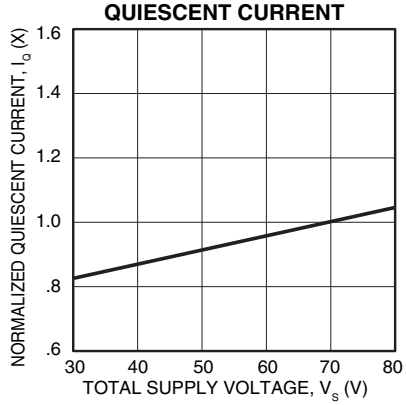
POWER DERATING



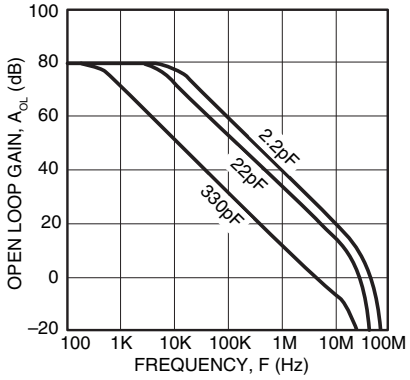
CURRENT LIMIT



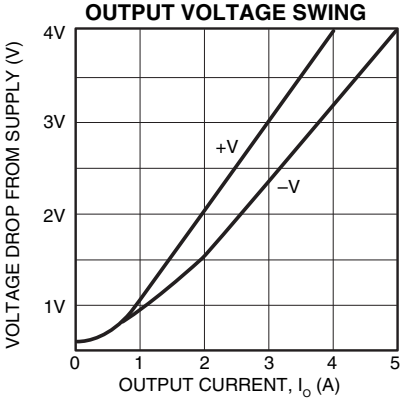
QUIESCENT CURRENT



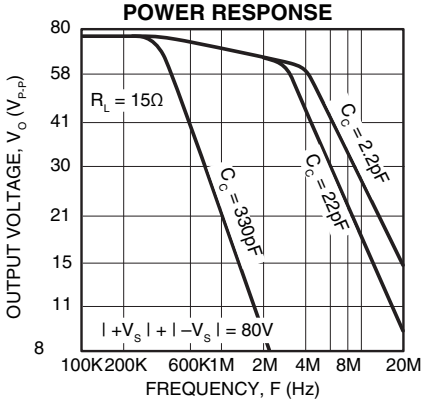
SMALL SIGNAL RESPONSE



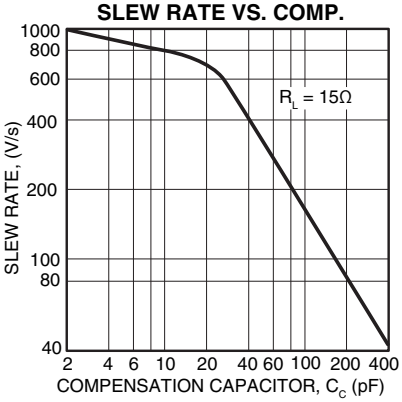
OUTPUT VOLTAGE SWING



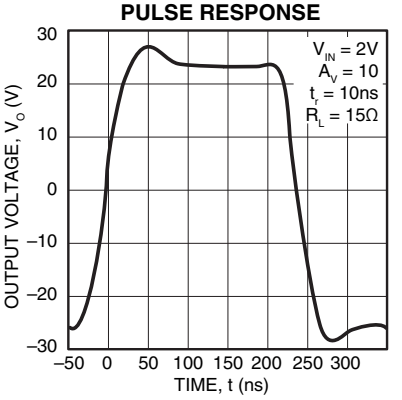
POWER RESPONSE



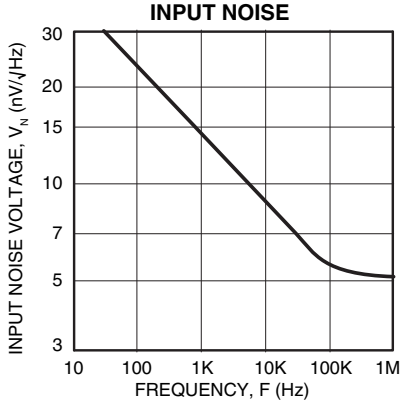
SLEW RATE VS. COMP.



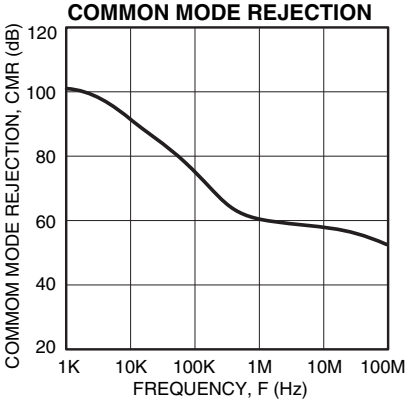
PULSE RESPONSE



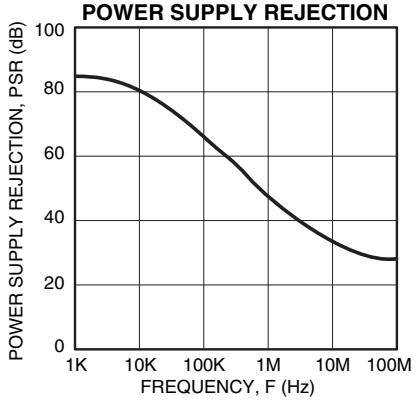
INPUT NOISE



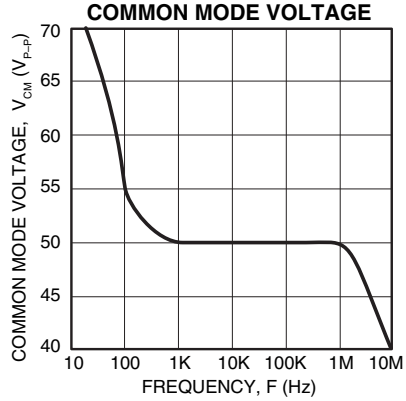
COMMON MODE REJECTION



POWER SUPPLY REJECTION



COMMON MODE VOLTAGE



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

Q2 (and Q25) limit output current by turning on and removing gate drive when voltage on pin 2 (pin 7) exceeds .65V differential from the positive (negative) supply rail. With internal resistors equal to 1.2Ω, current limits are approximately 0.5A with no external current limit resistors. With the addition of external resistors current limit will be:

$$I_{LIM} = \frac{.65V}{R_{CL}} + .54A$$

To determine values of external current limit resistors:

$$R_{CL} = \frac{.65V}{I_{CL} - .54A}$$

PHASE COMPENSATION

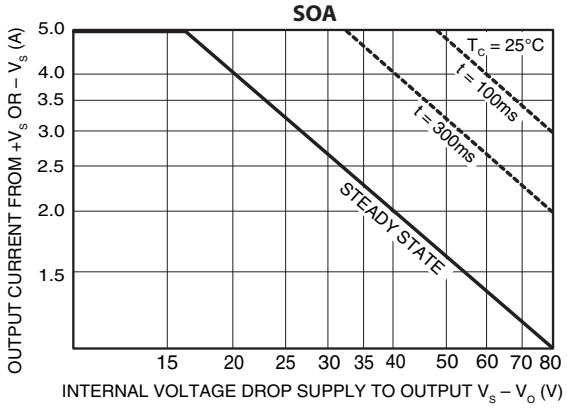
At low gain settings, an external compensation capacitor is required to insure stability. In addition to the resistive feedback network, roll off or integrating capacitors must also be considered when determining gain settings. The capacitance values listed in the external connection diagram, along with good high frequency layout practice, will insure stability. Interpolate values for intermediate gain settings.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

The SOA curves combine the effect of these limits and allow for internal thermal delays. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts:



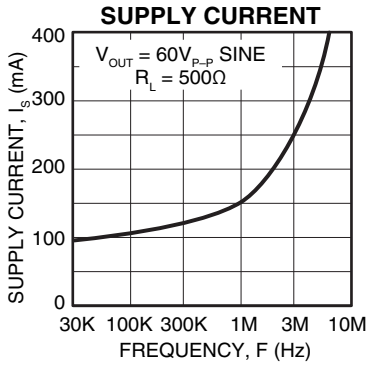
1. Capacitive and inductive loads up to the following maximums are safe:

±V_S	CAPACITIVE LOAD	INDUCTIVE LOAD
40V	.1µF	11mH
30V	500µF	24mH
20V	2500µF	75mH
15V	∞	100mH

2. Safe short circuit combinations of voltage and current are limited to a power level of 100W.
3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

SUPPLY CURRENT

The PA19 features a class A/B driver stage to charge and discharge gate capacitance of Q7 and Q19. As these currents approach 0.5A, the savings of quiescent current over that of a class A driver stage is considerable. However, supply current drawn by the PA19, even with no load, varies with slew rate of the output signal as shown below.



OUTPUT LEADS

Keep the output leads as short as possible. In the video frequency range, even a few inches of wire have significant inductances, raising the interconnection impedance and limiting the output current slew rate. Furthermore, the skin effect increases the resistance of heavy wires at high frequencies. Multistrand Litz Wire is recommended to carry large video currents with low losses.

THERMAL SHUTDOWN

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds approximately 150°C. This allows the heatsink selection to be based on normal operating conditions while protecting the amplifier against excessive junction temperature during temporary fault conditions.

Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the steady state boundary). It is designed to

protect against short-term fault conditions that result in high power dissipation within the amplifier. If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, destroy signal integrity, and reduce the reliability of the device.

STABILITY

Due to its large bandwidth, the PA19 is more likely to oscillate than lower bandwidth power operational amplifiers. To prevent oscillations a reasonable phrase margin must be maintained by:

1. Selection of the proper phase compensation capacitor. Use the values given in the table under external connections and interpolate if necessary. The phase margin can be increased by using a larger capacitor at the expense of slew rate. Total physical length (pins of the PA19, capacitor leads plus printed circuit traces) should be limited to a maximum of 3.5 inches.
2. Keep the external sumpoint stray capacitance to ground at a minimum and the sumpoint load resistance (input and feedback resistors in parallel) below 500Ω. Larger sumpoint load resistances can be used with increased phase compensation and/or by bypassing the feedback resistor.
3. Connect the case to any AC ground potential.

