# **LS7264**

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# FOUR PHASE BRUSHLESS DC MOTOR SPEED CONTROLLER

#### **FEATURES:**

- Drives 4 coils or 2 center tapped coils (two phase)
- Highly accurate speed regulation (±.1%) derived from XTL controlled time base.
- Rapid acceleration to speed with little overshoot
- Static braking
- 10V to 28V supply range
- Low speed detection output
- Internal overcurrent logic
- Power on reset
- Four outputs drive power switching transistors directly
- 16 pin dual-in-line package

#### **DESCRIPTION:**

The LS7264 is a monolithic, ion implanted MOS circuit designed to control the speed of a 4-phase, brushless, D.C. motor. This specific circuit is programmed for use in 3600 RPM applications. The circuit utilizes a 2.4576 MHz crystal to provide its accurate speed regulation time base. Overcurrent circuitry is provided to protect the windings, associated drivers and power supply. A static braking feature is provided to effect rapid deceleration.

Speed corrections are made by measuring the time between tachometer inputs and varying the on time of the drive signal applied to each winding. A sampling window is generated during which crystal derived clock pulses are accumulated. The contents of the accumulator provide the address of a look up table that has been derived from the physical characteristics of the motor and the load. The look up table output determines the amount of on time for each coil. Positive signals are applied sequentially to each winding driver through the output decoder/driver section.

A static type braking system shorts all winding together upon receipt of the brake input. This system creates an electrical load on the motor thus causing rapid deceleration. An overcurrent condition, when sensed at the overcurrent detection input, disables all four winding outputs. Outputs will be reenabled upon removal of the overcurrent condition.

LS DETECT OUTPUT 🔟	LSI	16) TACHOMETER INPUT
BRAKE INPUT 2		15 OVERCURRENT DETECT
OUTPUT 0 <sub>1</sub> 3		VDD (GND)
OUTPUT 024		33 FREQUENCY TEST POINT
OUTPUT 0 <sub>3</sub> 5		12) OSC OUT
OUTPUT 046		III OSC IN
VSS (+10 to +28 VDC) 7		10 FORWARD/REVERSE
S1 <b>8</b>		9 INPUT S2

TOP VIEW Figure 1

# INPUT/OUTPUT DESCRIPTION: LS DETECT OUTPUT (PIN 1)

This output provides a D.C. level which is high for speeds less than 1000 RPM.

#### **BRAKE INPUT (PIN 2):**

A high level applied to this input turns on all outputs, shorting the windings together. The brake input has priority over all other inputs. This feature may only be used when the center tap is connected to the positive supply through an external PNP transistor which is controlled by the brake signal. The brake input is provided with a pull-up resistor.

# INPUT/OUTPUT DESCRIPTION: (continued)

OUTPUTS 01, 02, 03, 04, (PINS 3-6)

These open drain outputs provide the base current (through external limiting resistors) to the base inputs of NPN drivers of the motor coils. They are enabled in the sequence described in Table 1 and for a duration as determined by the internal speed regulation data.

#### DESCRIPTION OF OUTPUT SIGNALS: (See Figures 1B)

Each output turns on at a change of commutator input state and remains on for a period of time determined by the rotational speed measured within the latest sampling window. The output pulse can be zero if speed is too high. If other than zero, the output width follows the formula Op $\psi$  (Clock Periods) = n x 384 x 4 ÷ No. of poles, where n varies from zero to 15. If the look up table indicates n is greater than 15, the pair remain on until the next commutation change.

#### VSS (PIN 7).

Supply voltage positive terminal, (+10 to +28 VDC).

#### \$1, \$2 INPUTS (PINS 8, 9)

These inputs provide control of the output commutation sequence as per Table 1. S1, S2 originate at the position sensors of the motor (see fig. 2). S1 and S2 are provided with a pull-up resistor.

#### FORWARD/REVERSE INPUT (PIN 10)

This Pin is used to control the motor's direction of rotation (see table I).

#### OSC IN (PIN 11).

This pin provides one of the two ports necessary for connecting a crystal. It may also be used to drive the circuit from an external clock.

#### OSC OUT (PIN 12).

This pin is used as the second connection when using a crystal for oscillation.

### FREQUENCY TEST POINT (PIN 13).

This test output provides the user with a point to measure the

oscillator frequency without loading the oscillator: It provides a signal which is one sixth of the oscillator frequency.

#### VDD (PIN 14).

Supply voltage negative terminal (ground).

#### OVER CURRENT DETECT (PIN 15).

The Overcurrent Detection Input provides the user a way of protecting the motor windings, drivers and power supply from an overload condition. The user provides a fractional ohm resistor between the positive supply and the positive side of the motor windings. This point is connected to a potentiometer (e.g. 100k ohm), the other end of which is connected to ground and the wiper connected to the overcurrent input. The wiper pickoff is adjusted so that the outputs  $0_1 - 0_4$  are off for currents greater than the limit.

An example of setting up the over current follows:

- Determine the fractional ohm resistance and the maximum current to determine the voltage drops across the resistor and call this V<sub>OC</sub>.
- Apply V<sub>SS</sub>-V<sub>OC</sub> to the fractional ohmage end of the potentiometer.
- 3. Hold S1 and S2 in a known state (e.g.00). This will enable 0<sub>1</sub>-0<sub>4</sub> outputs in accordance with Table 1.
- 4. Adjust the potentiometer until outputs  $0_1$ - $0_4$  are at ground.
- Remove the voltage from the potentiometer and connect the potentiometer to the winding end of the fractional ohm resistor.

# TACHOMETER INPUT (PIN 16).

The signal applied to the tachometer input originates at a motor position sensor (one of the commutation inputs may be used). Each negative edge of the tachometer input is synchronized by the one sixth oscillator frequency. The resulting signal 1) transfers new speed regulation data to the "on time" data storage latches, 2) resets the clock pulse accumulator and 3) originates a new sampling window. The tachometer input is provided with a pull-up resistor.

#### **MAXIMUM RATINGS:**

PARAMETER Storage Temperature Operating Temperature	SYMBOL T <sub>stg</sub>	VALUE -65 to +150	UNITS °C
1. Plastic 2. Ceramic	Т <sub>ар</sub> Т <sub>ас</sub>	-25 to +70 -55 to +125	°C °C
Voltage (any pin to V <sub>SS</sub> )	V <sub>max</sub>	-30  to  +0.5	VOLTS

#### DC ELECTRICAL CHARACTERISTICS: (+10 to +28 VDC)

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SUPPLY CURRENT	SYMBOL	MIN.	MAX.	UNITS
(Excluding Outputs)	100	_	22	mA

# **INPUT SPECIFICATIONS:**

Brake, commuting and tachometer (Pins 2, 10, 11, 12, 18)

INPUT VOLTAGE	MIN.	MAX.	UNITS
Logic "1"	V <sub>SS</sub> -2.5	$V_{SS}$	VOLTS
Logic "O"	0	$V_{SS}$ -5	VOLTS

#### INPUT CURRENT

Each of the five inputs provides an internal constant current source to  $V_{SS}$  of 200 to 400 ua (typically 300ua)

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# **OVERCURRENT DETECTION INPUT (PIN 15)**

INPUT VOLTAGE	MIN.	MAX.	UNITS
Logic "1"	$(V_{SS} \div 2) + .25$	$V_{SS}$	VOLTS
Logic "0"	0	$(V_{ss} \div 2)25$	VOLTS

Theoretical switching point for the Overcurrent Detection Input is one half of the power supply. Manufacturing tolerances cause the switching point to vary plus or minus .25 volts. After manufacture, the switching point remains fixed within 10mv over time and temperature. The input switching sensitivity is a maximum of 50mV. There is no hysteresis on the overcurrent detection input.

OSCILLATOR INPUT (PIN 11). (When driven from external source.)

	MIN.	MAX.	UNITS
Logic "1"	V <sub>SS</sub> -1	$V_{SS}$	VOLTS
Logic "0"	0	$V_{SS}$ -6	VOLTS

#### **OUTPUT SPECIFICATIONS**

#### 410 KHz TEST (PIN 13)

Designer for  $10M\Omega$ , 20 pF scope probe.

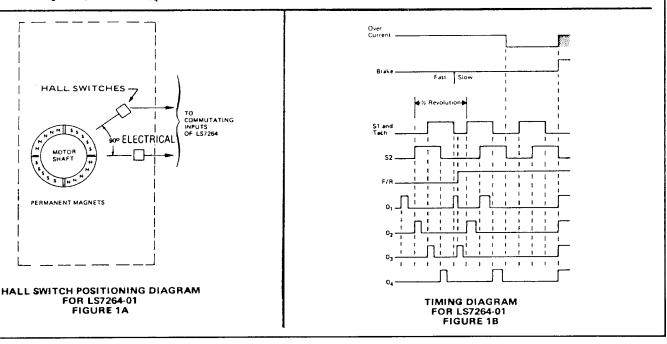
# LS DETECT OUTPUT (PIN 1)

	MIN.	MAX.	UNITS	CONDITIONS
Isource	1.0		mA	Output short circuit to V <sub>DD</sub>
ISINK	10.0		ua	Output at .5V

# 0<sub>1</sub>-0<sub>4</sub> (PINS 3-6)

0<sub>1</sub>-0<sub>4</sub> are current sources (Base current limiting resistors are required)

TABLE 1					
F/R	<b>S</b> 1	<b>S2</b>	OUTPUT S ENABLED		
0	0	0	01		
0	0	1	02		
0	1	1	$0_{3}^{-}$		
0	1	0	04		
1	0	0	03		
1	1	0	02		
1	1	1	01		
1	0	1	04		



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